A Low SINR Synchronization System for Direct-Sequence Spread-Spectrum Communications: Radio Prototype, Verification Testbed and Experimental Results

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ABSTRACT

Ability to receive signals at low signal to interference and noise ratio (SINR) improves the spatial range and reliability of wireless networks. However, it is difficult to design a communication system that operates correctly in this type of environment. Our system uses a high spreading gain in the direct-sequence spread-spectrum (DSSS) modulation to combat the problems associated with low SINR. Undoubtedly, *synchronization* is a severe bottleneck for low SINR reception in DSSS.

In this paper, we present a prototype hardware implementation of a DSSS synchronization system, which was proposed in [1], a testbed, and experimental results. The synchronization system is implemented on a reconfigurable radio prototyping platform and verified on a hardware testbed. Controlled experiments are performed in the laboratory to calibrate its performance. Finally, over-the-air experiments are conducted at two outdoor test sites and the results are presented.

Categories and Subject Descriptors

C.2.1 [**Computer-Communication Networks**]: Network Architecture and Design—*wireless communication*;
C.3 [**Special-purpose and Application-based Systems**]: Signal Processing Systems;
C.5.4 [**Computer System Implementation**]: VLSI Systems

General Terms

Design, Experimentation, Measurement, Performance

Keywords

synchronization, direct-sequence spread-spectrum, radio prototype, asynchronous communication, wireless testbed

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1. INTRODUCTION

Recent advances in wireless communications and VLSI technology have led to a tremendous increase in the usage of wireless devices in everyday life. A majority of these devices depends upon an asynchronous packet-based mode of communication which leads to fast deployment of these devices in a wireless network. Asynchronous reception requires synchronization to be performed per packet. For example, in the popular 802.11 standard [2] based networks, the preamble and header fields are appended to the start of the payload in each packet to aid the synchronization process. On the other hand, cellular communications typically rely upon a pilot signal which is always available for synchronization. It requires a network infrastructure that is expensive to set up and unsuitable for fast deployment. In this paper, we will focus upon asynchronous packet-based communication.

Wireless communications in the low signal to interference and noise ratio (SINR) environment are becoming increasingly important although the low SINR makes communications difficult. Low SINR is caused by long distance between transmitter and receiver, the communication channel being *in fade*, or interference from adjacent wireless transmissions over the same frequency spectrum. Furthermore, there is a growing interest in low SINR operation for improving the throughput in wireless networks [3].

Low SINR can be countered by employing a high spreading gain in the direct-sequence spread-spectrum (DSSS) modulation at the cost of lowering the data rate [1, 4]. This will lead to a gradual reduction in throughput with decreasing SINR, rather than an abrupt disconnect. The DSSS modulation is also used to tackle frequency-selective fading and is highly resistant to interference and jamming [5]. Moreover, it has a low probability of intercept and can also be used for random access of the wireless spectrum by multiple users using the unique properties of its spreading code [5]. However, the ability to synchronize over a short period of time limits the performance of the DSSS receiver at low SINR.

Synchronization in a DSSS receiver involves code acquisition, code tracking, carrier recovery, multipath detection and frame synchronization [5, 6, 7] as shown in Figure 2. Code acquisition [8] ensures correct despreading operation in the receiver by aligning the spreading code in the incoming packet with a local copy of the spreading code at the receiver. Once the acquisition is achieved, tracking [9, 10] *maintains* the alignment of the local spreading code with the received signal over the reception of the entire packet. Car-

rier recovery [11] is performed in the coherent demodulation schemes for correctly estimating the carrier frequency and phase from the incoming signal. Multipath detection estimates the multipath delay profile of the channel for the subsequent RAKE combining [5, 7] operation. Finally, frame synchronization [12] finds the start of the payload in the received packet.

A system for reliable synchronization at low SINR has been presented in [1]. For this paper, we implemented the system on a radio prototype. We verified the implementation on a hardware testbed, capable of emulating wireless channels. After the verification, we calibrated the system performance using controlled experiments in the laboratory. Finally, we conducted experiments at two outdoor test sites to observe the performance of the system over real wireless channels.

The remainder of the paper is organized as follows. Section 2 describes the synchronization system. Section 3 describes the radio prototype and Section 4 the hardware verification testbed. Section 5 presents the experimental setup and results. Finally, we draw conclusions in Section 6.

2. SYSTEM DESCRIPTION

2.1 Packet Format

Figure 1 shows the packet format used by the transmitter in the proposed DSSS system [1]. Each packet is divided into 3 fields: preamble, start frame delimiter (SFD), and payload. The preamble is used for achieving symbol-level synchronization at the receiver. It consists of 67 repeating symbols of ones, each of which is spread by a short psuedo-random (PN) sequence [13]. The SFD field consists of 31 binary symbols, each of which is spread using one of two orthogonal Kasami sequences, depending on its polarity. Kasami sequences have good autocorrelation and crosscorelation properties and can be used for non-coherent detection of the symbols [14]. The PN and the Kasami sequences used for spreading the packet symbols consist of 63 chips each. Finally, the binary symbols in the SFD field form a 31-bit PN code to improve frame synchronization using a correlation-based method. The payload contains the actual information to be transmitted and is encoded exactly like the SFD field.

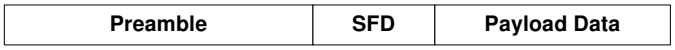

Figure 1: Packet format.

2.2 Synchronization Block

Figure 2 shows the block diagram of the synchronization system (also referred to as the synchronization block (SB) in the rest of the paper). Symbol decoding is performed using non-coherent detection. Thus the carrier recovery block (needed for coherent communication) is not included for this implementation; however, it can easily be integrated into the system with a minor redesign of the non-coherent SB.

The down-converted and digitized baseband I and Q signals from the analog front-end of the receiver are fed to the inputs of the SB. During the reception of the preamble, the SB performs a post-detection integration (PDI) based parallel code acquisition [4, 6, 8] operation for fast synchronization at low SINR. Parallel code acquisition, which leads to

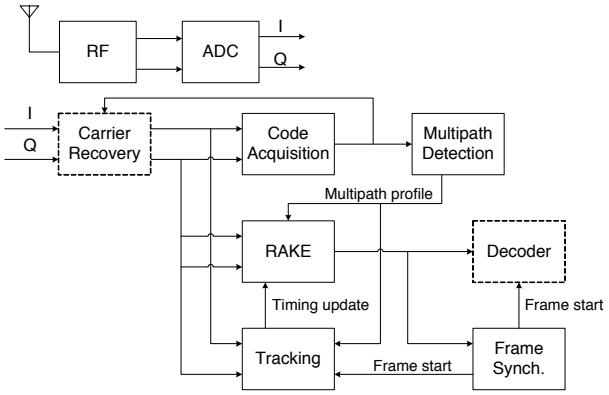

Figure 2: Synchronization block.

fast acquisition, involves simultaneous testing of all hypotheses for correct alignment of the incoming received signal and the locally generated spreading code for accurate despreading operation. The PDI operation involves summing the energy over multiple symbol periods for improving the acquisition performance. Once the acquisition is completed, the multipath detection is performed to resolve all the multipaths for subsequent RAKE combining operation, which is needed for frame synchronization and decoding of payload symbols. After the multipath search, the frame synchronization block searches for the SFD field in the incoming packet by correlating the raw received symbols with a locally generated 31-bit PN code used in the SFD field. The location of the peak of this correlation output determines the start of the payload — the following symbols are sent to the decoder for post-processing. Code tracking operation maintains the synchronization over the reception of the entire payload.

The perfomance of the SB is analyzed via simulations in [1]. Figure 6, as presented in [1], shows the probability of correct synchronization under the additive white Gaussian noise (AWGN). Note that the SINR is calculated after the despreading operation which includes the spreading gain of approximately 18 dB (for a spreading ratio of 63). We observe that the SB accurately synchronizes more than 90% of the received packets at a post-despreading SINR of 3 dB.

Figure 7 shows the probability of correct synchronization in a multipath environment. The small-scale fading for each discrete multipath is modeled by the Rayleigh distribution and the average power by an exponentially decaying multipath intensity profile [15]:

$$\Omega_l = \Omega_1 \; e^{-\tau_l / \tau_{max}}, \quad l = 1, 2, 3, ..., L_p$$

where Ω_l is the average power of the l^{th} path and τ_{max} represents the maximum delay spread.

The SINR under the multipath Rayleigh fading conditions is calculated from the signal power Ω_1, the strongest average multipath signal. Note that it does not denote the SINR based on the combined strength of all the paths in the multipath profile.

The specific delay profile is:

$$\{\tau_l\}_{l=1}^{L_P} = \{0,\ 3.88,\ 10.63,\ 15.75,\ 19.75,\ 22.13,\ 26.5\} \quad (1)$$

where the unit is a chip period T_c. Therefore, for a spreading ratio of 63, the maximum delay spread is 0.42 times a bit period. We observe that the SB accurately synchronizes

more than 90% of the received packets at an average post-despreading SINR of 3 dB for the strongest multipath signal.

3. RADIO PROTOTYPE

The synchronization block is implemented on a radio prototyping platform to demonstrate the feasibility of its implementation.

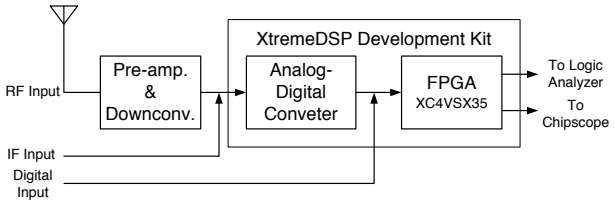

Figure 3: Block diagram of the radio prototyping platform.

Figure 3 shows a block diagram of the radio prototyping platform. The RF receiver front-end is implemented using a National Instruments preamplifier (PXI-5690) [16] and downconverter (PXI-5600) [17] which are housed in a NI PXI chassis (PXI-1045) [18]. The digital baseband component of the SB is implemented on a Xilinx Virtex-4 (XC4VSX35) FPGA [19]. This FPGA is part of a Xilinx XtremeDSP Development Kit for Virtex-4 [20] which also hosts a Analog Devices AD6645 [21] 14-bit ADC with a maximum sampling rate of 105 MSPS. The FPGA is interfaced to the PC using a JTAG cable for conducting real-time measurments using the Chipscope [22] software logic analyzer provided by Xilinx.

The PXI-5690 RF preamplifier has gain and noise figure characteristics that optimize the dynamic range and sensitivity of the NI PXI-5600 RF downconverter. The typical noise figure of the preamplifier is 5 dB [23]. The National Instruments PXI-5600 downconverts a RF signal up to 2.7 GHz to a low intermediate frequency (IF) of 15 MHz. The noise density of the PXI-5690 and PXI-5600 combination ranges from -162 dBm/Hz to -164 dBm/Hz, depending on the frequency range [23]. The downconverted IF signal is first digitized at 80 MSPS by the ADC and then digitally downconverted to baseband before being processed by the baseband section of the SB.

The following parameters were used for designing the VLSI architecture of the digital baseband section:

- Chipping rate = 10 Mchips/sec
- Sampling rate = 80 Msamples/sec
- Oversampling ratio (N_s) = 8
- Spreading ratio (N_c) = 63
- Symbol rate = 158.73 Kbits/sec
- Length of PDI operation = 32 symbol periods
- Number of RAKE fingers (N_{FINGER}) = 4

The area utilized on the FPGA was *directly proportional* to the number of symbols used in the postdetection integration operation for code acquisition and the spreading ratio. A brief summary of the FPGA implementation is shown in Table 1. For better understanding of these parameters, one can refer to the Virtex-4 documentation [19].

Logic Distribution	Used	Avail.	Utilized
Number of 4-Input LUTs	25298	30720	82%
Number of BRAMs	157	192	81%
Number of DSP48s	18	192	9%

Table 1: FPGA implementation details.

4. VERIFICATION TESTBED

The SB implementation is verified using the hardware test setups available on the testbed. The verification consists of two steps:

- *Digital Baseband Test*: The baseband test vectors used for simulations are fed to the SB implementation on the FPGA as digital input for verification of the digital hardware. Note that the signals used for the simulations and digital hardware verification are *exactly identical* including the noise characteristic.
- *RF Test*: The baseband test vectors used for simulations (without the noise) are upconverted to RF and fed as input to the SB. This tests the RF downconversion and analog-to-digital conversion components of the prototype.

4.1 Digital Baseband Test Setup

Figure 4 shows a block diagram of the digital baseband test setup. The baseband test vectors are replayed as a digital stimulus to test the digital subsystem of the SB. This is achieved by using a combination of the Agilent Baseband Studio N5110B [24] and N5102A [25] modules. N5110B Baseband Studio for Waveform Capture and Playback allows playback of custom digital IQ test vectors of up to 512 million samples. Agilent N5102A Baseband Studio Digital Signal Interface module provides an easily controllable digital interface to connect to the digital subsystem. An Agilent logic analyser is used for monitoring and calibrating the performance of the digital logic inside the FPGA. The Agilent logic analyzer consists of a 16901A Logic Analysis System [26] and 16950B measurement module [27]. The 16901A is a 2-slot logic analysis mainframe and the 16950B is a 68-channel 4 GHz timing, 667 MHz state logic analysis measurement module.

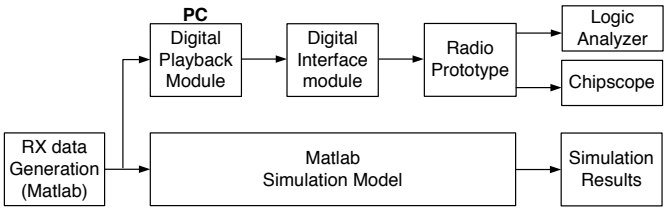

Figure 4: Digital Baseband Test Setup

4.2 RF Test Setup

Figure 5 shows a block diagram of the RF test setup. In this setup, the baseband test vectors are up-converted to 2.4 GHz by an Agilent ESG 4438C [28] signal generator which serves as a RF transmitter. The transmission bandwidth is set to 20 MHz, for a chipping rate of 10 Mchips/sec, similar to that used in WLANs [2]. The transmitter output is connected to the radio prototype input via a variable

attenuator. This setup emulates a single line-of-sight link between the transmitter and receiver. The received signal level can be adjusted using the variable attenuator. The logic analyzer in this setup helps in real-time monitoring of the SB performance. It is also used for calculating the received SINR for accurate calibration of test results.

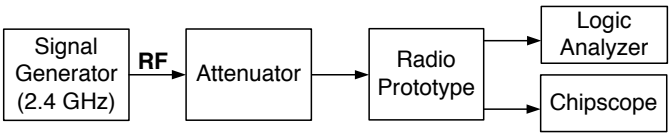

Figure 5: RF Test Setup

4.3 Hardware Test Results

Figure 6 shows the probability of correct synchronization for the SB at various SINR under additive white Gaussian noise (AWGN) environment. As mentioned earlier in Section 2.2, the SINR is calculated after the despreading operation which includes the spreading gain of approximately 18 dB (for a spreading ratio of 63). In Figure 6, we observe that the digital verification results closely match the simulation results and thus verify the accuracy of the digital implementation. We also observe that the controlled RF verification tests, using the setup described in Section 4.2, accurately match the simulation and digital verification results.

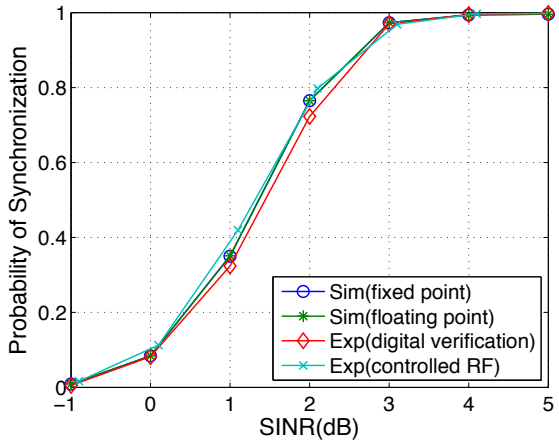

Figure 6: Simulation and verification results under AWGN.

Figure 7 shows that digital verification results for the multipath Rayleigh fading channel described in Section 2.2 accurately match the simulation results. RF verification tests, similar to the experiments conducted for the AWGN channel, could not be conducted due to the difficulty in emulating a specific multipath environment in the laboratory. From Figures 6 and 7, we conclude that the implementation of the SB on the prototyping testbed faithfully translates the SB design into real hardware.

5. EXPERIMENTAL RESULTS

The performance of the SB prototype is calibrated in a controlled lab setup. After calibration, the SB prototype is evaluated at two outdoor test sites using over-the-air packet receptions in highly scattering multipath environments.

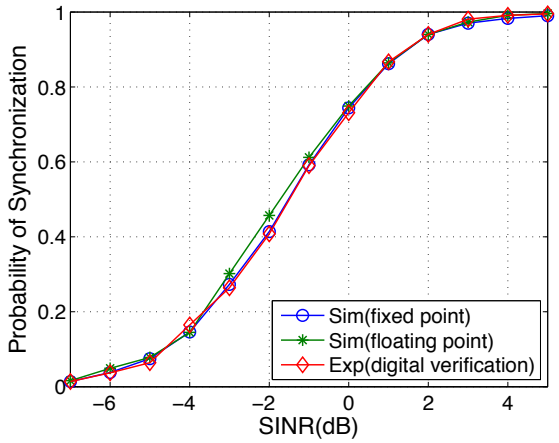

Figure 7: Simulation and verification results for multipath environment.

5.1 Lab Experiment

The ability of the SB to receive low SINR signals has already been established via simulations and hardware tests in Sections 2 and 4, respectively. Experiments were also conducted to calculate the sensitivity of the SB prototype. Sensitivity is the minimum signal level required for reliable operation of the SB. We use a 95% synchronization rate as the yardstick for reliable operation of the SB. The RF test setup described in Section 4.2 is used for conducting the sensitivity experiment. It is equivalent to an unfaded AWGN channel without multipath. The received signal level is controlled using an attenuator between the Tx RF output and the Rx RF input.

Receiver sensitivity is used as a figure of merit for calibrating the performance of wireless receivers. For example, according to the 802.11 standard [2], the receiver sensitivity is the minimum input signal level for which the frame error ratio shall be less than 8% at a payload length of 1024 bytes encoded using 2 Mbps DQPSK modulation. The sensitivity for commercial 802.11a/b/g wireless receivers vary from vendor to vendor and also depends on the data rates and modulation used. −94 dBm is the lowest sensitivity level we have encountered in literature [29].

From Figure 8, we observe that we are able to synchronize reliably at low signal levels at the RF input of the receiver. For example, we are able to synchronize 99.37% of the received packets when the signal level is −101.7 dBm. The sensitivity of the SB is observed to be at least −102 dBm since we correctly synchronize more than 95% of the received packets at that signal level. Since we have not developed a complete packet receiver, we are unable to compare the SB sensitivity to the receiver sensitivity of the commercial 802.11a/b/g receivers.

5.2 Outdoor Experiments

The setup for the outdoor experiments is similar to the RF test setup described in Section 4.2 with the attenuator replaced by commercial off-the-shelf omnidirectional antennas. The antennas are placed at a height of one meter while

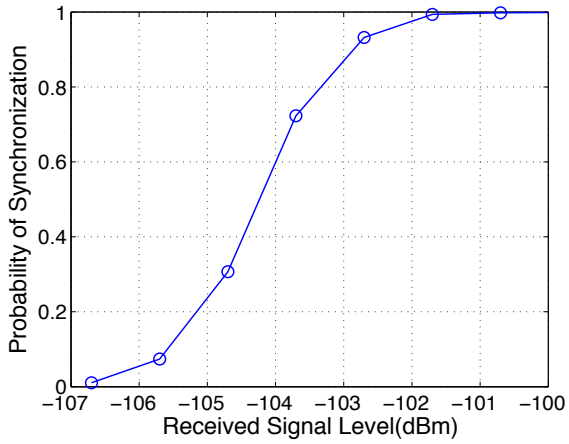

Figure 8: Sensitivity experiment results.

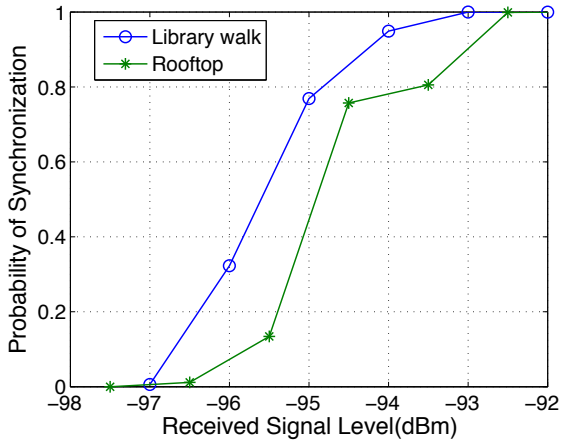

Figure 10: SB performance at the two outdoor test sites.

conducting the tests. The received signal power is controlled by varying the transmit power. The average received signal power is measured using the spectrum analyzer placed at the receiver. The multipath delay profile and fading characteristics of the channel were not measured or characterized during the experiment. As a part of our future research, we plan to perform channel characterization to gain further insights from our outdoor experiments.

The rooftop of Atkinson Hall building at University of California, San Diego was used as the first test site. Figure 9 shows the layout of the test site. The transmitter (Tx) and the receiver (Rx) are separated by 54 meters. Although there is a line-of-sight between Tx and Rx, the proximity of the Tx and Rx to metal walls, vents, and other structures causes multipath propagations. The multipath intensity profile can be assumed to be constant over time since Tx, Rx, and scatterers are stationary.

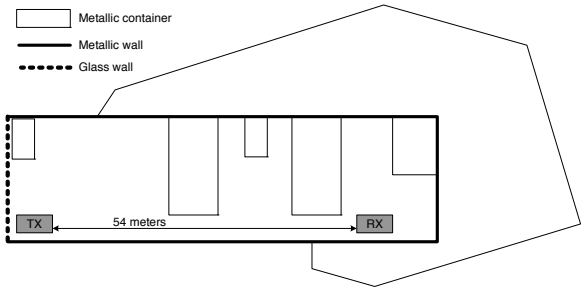

Figure 9: Rooftop layout.

Figure 10 shows the performance of the SB on the rooftop averaged over 50,000 packet transmissions. We observe that almost all the packets are correctly received at a signal level of −92.5 dBm and above. The received signal level of −92.5 dBm corresponds to −27.4 dBm of transmit power.

The second test site is a long pathway in front of the Geisel Library at University of California, San Diego — also known as the Library Walk. We placed the transmitter and receiver at a distance of 137 meters and performed the experiment. Apart from the line-of-sight component, we also had multipaths coming into the receiver due to trees, surrounding buildings, and people walking past the experimental setup.

Unlike the first outdoor experiment, the multipath intensity profile at this test site cannot be assumed to be constant over time as the scatterers are mobile and change positions over time. The layout of the library walk is given in Figure 11.

Figure 11: Library walk layout.

Figure 10 shows the performance of the SB on the library walk averaged over 50,000 packet transmissions. We observe that almost all the packets are correctly received at a signal level of −93 dBm and above. The −93 dBm received signal level corresponds to −13.4 dBm of transmit power.

The results from the rooftop experiments show that the SB is able to synchronize reliably over 54 meters in a rich multipath environment at a transmit power of −27.4 dBm. The results from the library walk show that the SB is able to synchronize reliably over 137 meters in an urban line-of-sight setting at a transmit power of −13.4 dBm. Note that 30 dBm is the maximum transmit power limit with omnidirectional directional antennas over the 2.4 GHz unlicensed ISM band in the United States [30] (other countries have similar limits). Hence, we can further improve the spatial range by transmitting at a higher transmit power compared to the experimental setups. For example, a 6 dB increase in transmit power can double the spatial range in free space [31].

6. CONCLUSIONS

We have implemented a synchronization system for low SINR operation in asynchronous packet-based DSSS communications on a reconfigurable radio prototyping platform. The prototype is verified on a hardware testbed, and controlled lab experiments are carried out to calibrate its performance. Finally, experiments are conducted at two outdoor test sites to evaluate its performance over real wireless

channels. Experimental results show that the prototype has a lower receiver sensitivity compared to commercial 802.11 receivers. It also performs reliably over long distances in outdoor environments.

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