A Biosensor Readout Circuit with 3fF Resolution and Broad Configurable Range

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***Abstract*— Capacitance to digital conversion is often used for biosensor readout circuits based on charge sensitive amplifier Front Ends. Absolute capacitance can be measured by the time it takes to discharge a capacitance through a current source. Higher precision is obtained, if the difference between the unknown capacitance and a reference one is estimated but this is difficult to be achieved if the range of the biosensor capacitance is broad. In this paper, an absolute capacitance readout circuit appropriate for use with capacitive biosensors is presented. It can cover a capacitance range of 180pF with an experimentally measured capacitance accuracy of 3fF, close to the 2.44fF theoretical resolution (Integral Non Linearity-INL<1 LSB). This mixed signal readout circuit has been implemented and successfully tested in 90nm TSMC CMOS technology occupying 0.04mm^2 of die area. This system is extended for a range of 640pF based on a method that digitally configures an appropriate external reference capacitance close to the unknown capacitance value. The 3fF resolution is achieved by using a 12-bit instead of 18-bit ADC that would be required to measure an absolute capacitance value with the same accuracy.**

Keywords- Biosensors, Readout, Capacitance Measurement

I. INTRODUCTION

The capacitive biosensor operation is based on chemical reactions that influence their capacitance and can be used for example in DNA analysis [1]. On the membrane surface, probe molecules are immobilized and upon interaction with the corresponding targets, the membrane deflects due to surface stress variation. The deflection is translated into charge in capacitance between the flexible electrode and substrate. The development of miniaturized capacitance arrays on silicon is of crucial importance for the successful use of these microsystems in practical biological applications.

The variation in the biosensor capacitance values during a chemical process that is called hybridization is usually slow and requires several minutes or even hours to complete. Although there is no need for fast digitization, several biosensors (e.g., 64 or 256) have to be measured in a specific time interval and a high A/D Converter (ADC) resolution is required to observe small capacitance changes of a few fF starting from an arbitrary high initial value. The scientists in such applications are more interested in accurately monitoring how the biosensor capacitance changes rather than be aware of absolute capacitance values. The integrated microsystem which can be achieved through Si-based biosensors make them most suitable for point of care diagnostic systems. Nevertheless, such Si-based biosensors usually suffer from low selectivity, higher detection limits compared to label based techniques and the elements that have to be accommodated are considerably lower than what may be achieved with traditional optical scanning techniques and labeled micro arrays.

Capacitive sensors are also used for measuring humidity [2] and pressure [3]. Analogue integrators called Charge Sensitive Amplifiers (CSA) [1] or Switched Capacitance Interface (SCI) [4] are used to map an input capacitance to a voltage level or a pulse with appropriate duration. In the first case, an ADC like the one presented by the authors in [5] can be connected at the CSA output while in the second case the duration of a pulse can be measured using a counter [1]. The difference, between a reference capacitor and the unknown one can be measured by circuits like the one presented in [4] where a configurable on-chip reference capacitor has been used. In [6] a configurable reference capacitor has also been proposed where 6 input sensors are multiplexed and 3 capacitors are combined to form a reference value between 250fF to 15pF in steps of 250fF. The correlation between a Direct Charge Measurement (DCM) and the classic LCR method followed by commercial capacitance-meters is examined in [7] and finally, a very accurate capacitance measurement is performed in [8] based on a delta-sigma converter and a high precision calibration step.

The Capacitance to Digital (CTD) measurement is performed here by discharging the unknown capacitance through a small current source. This solution has been selected as more suitable compared to a CSA (integrator) input, since it can accommodate a broader range of biosensor capacitance values without facing overload or oscillation effects. The time it takes for the capacitance to be discharged is measured by a 16-bit counter driven by a fast clock that is generated by a robust low complexity frequency multiplier. The output of the counter is captured at the end of the measurement interval by a 16-bit Parallel In-Serial Out register that enables the reading of the counter value through a 2-wire serial interface.

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An extended version of the implemented readout circuit is also described and this version is capable of measuring the difference between the unknown biosensor and a configurable reference capacitor with a theoretical 2.44fF accuracy. This circuit connects in parallel an appropriate combination of external capacitors that can provide a reference value between 0 and 630pF in steps of 10pF.

The implemented biosensor array readout system is presented in detail in Section II. Simulation and experimental results are presented in Section III. Finally, the readout system with configurable external reference capacitor is described in Section IV.

II. ARCHITECTURE OF THE IMPLEMENTED IC

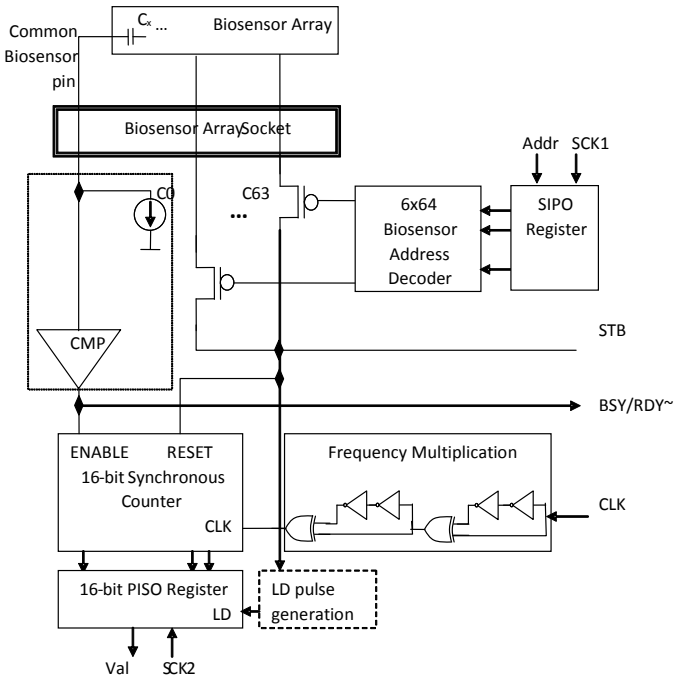


Figure 1. The implemented readout circuit based on CTD.

The architecture of the implemented solution is presented in Fig. 1. The address of the selected biosensor is fed through a 2-wire serial interface (lines: *Addr*, *SCK1*). One of the outputs of a 6x64 NOR address decoder is activated connecting one of the 64 biosensors to the strobe signal *STB* that charges the selected biosensor capacitance. All the biosensors share a common pin connected to a current source and the input of an operational amplifier with very high input resistance so that the leakage current in this path is negligible.

The current source and the comparator of the dotted square of Fig. 1 are shown in more detail in Fig. 2. The current source is comprised of the transistors *M1* to *M4* and the resistors *R1* and *R2*. The dimensions of the transistors *M3* and *M4* are chosen so as to achieve the required constant current, while the degeneration resistors increase the output resistance of the current source.

The shape of the *M2* voltage drain is a sawtooth and its duration is proportional to the measured capacitance. The *CMP* operational amplifier converts the sawtooth to a rectangular pulse with equal duration.

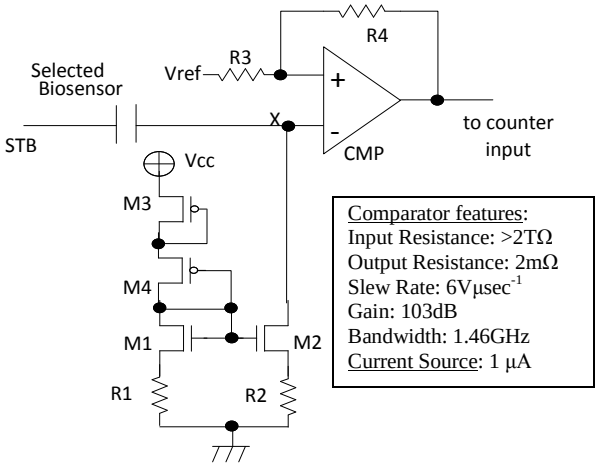


Figure 2. The discharge circuit of the biosensor capacitance (CTD)

The comparator buffers the sensitive node *X* and remains low for as long as the sensor capacitance discharges. Consequently, high input resistance and high slew rate are required by the operational amplifier that implements the comparison operation as shown in see Fig. 2. The use of the resistors *R1* and *R2* adds hysteresis, to stabilize the output under all conditions.

Taking the parasitic input capacitance of the operational amplifier (C_p) into consideration, the voltage at node *X* when the strobe pulse is applied is:

$$V_x = V_{stb}\ C_s/(C_s + C_p) \tag{1}$$

where V_{stb} is the strobe voltage and C_s is the sensor capacitance. The absolute value of the sensor's charge Q_s that the current source draws in a single conversion is $Q_s = C_s(V_x - V_{tl})$. The voltage V_{tl} is the threshold of the comparator for a low-to-high transition. Similarly, for the parasitic capacitance C_p: $Q_p = C_p(V_x - V_{tl})$. Taking into account the finite output resistance *R* of the current source, the extra amount of charge Q_m drawn by the current source is:

$$Q_m = t \cdot I_m = t(V_x + V_{th1})/(2R) \tag{2}$$

where the average value of the current I_m has been used, while *t* is the duration of the output pulse. If the constant current of the current source is I_s, the duration of the output pulse is estimated by dividing the total charge with I_s. The total charge is the sum of Q_s, Q_p and Q_m. The duration *t* of the output pulse can be expressed as:

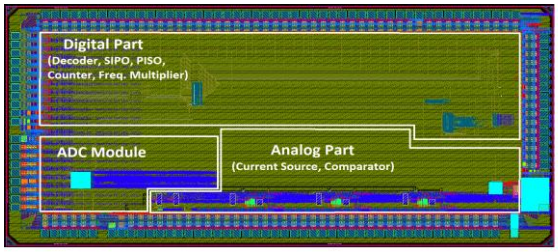
$$t = \frac{2R(C_s + C_p)(V_x - V_{tl})}{2RI_s + (V_x + V_{tl})} \tag{3}$$

It becomes evident from equation (3) that both the finite output resistance of the current source and the parasitic input

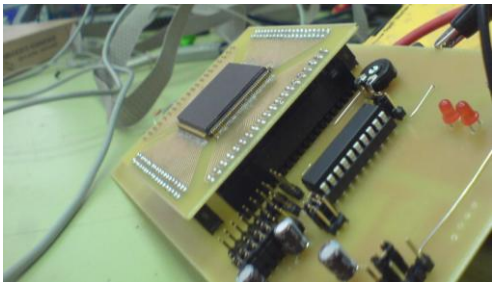
capacitance of the operational amplifier affect the time to be measured, the first changing the gain of the setup and the second adding an offset, proportional to C_p. For a perfect current source and operational amplifier (R infinite, $C_p=0$), equation (3) is reduced to $t=Q_s/I_s$, as expected.

The operation of the 16-bit synchronous counter is enabled as long as the *CMP* output is active (low). The counter speed has to be high in order to achieve higher measurement accuracy. A low complexity internal frequency multiplier is used to generate the high frequency clock required by the counter. The input of this frequency multiplier can be an external clock, with up to 100MHz frequency, that is multiplied by 4 to get the internal 400MHz frequency used by the counter. The frequency multiplication is implemented by the use of high speed XOR gates with inputs that have different delay and are driven by the previous stage output (or the external clock in the first stage). Although the duty cycle of the output pulses of such a frequency multiplier is not stable, Monte Carlo simulations showed that there were no missing pulses and the correct counter operation is guaranteed.

The output of the 16-bit counter is captured by the a 16-bit Parallel-In Serial-Out (PISO) register at the end of the CMP pulse. The output of the PISO register is read serially through the data pin *Val* and the clock *SCK2*. The layout of the IC developed in TSMC90nm technology as well as the development board for the evaluation of this IC is shown in Fig. 3. The pure die area of the various blocks and the total power consumption is 0.04mm^2 and 5mW respectively.



(a)



(b)

Figure 3. The layout (a) and development board (b) of the biosensor readout IC (4mmX2mm).

III. Simulation and Experimental Results

In Fig. 4, the discharge (sawtooth) of a 20pF and an 180pF sensor is shown, alongside with the respective output pulse of the comparator. Fig. 5 demonstrates the linearity of the system, by measuring a number of distinct capacitance values. As can be seen from Fig. 5, it would not be accurate to approximate the whole capacitance range with a single line but an estimation error around 3fF (INL<1LSB) can be achieved using piecewise linear approximation and sample averaging for the suppression of the noise effect. These operations can be performed by the low cost microcontroller incorporated in the development board. The maximum conversion time T_{max} can be estimated as $T_{\max} = 2^b / F_{clk}$, where F_{clk} and b are the clock frequency and the resolution of the counter, respectively. T_{max} is approximately 164 usec here.

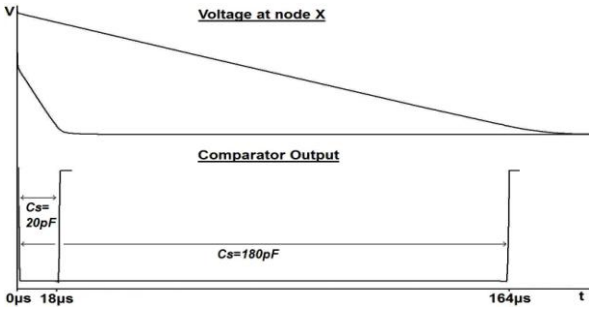


Figure 4. V_x and comparator output at 20pF and 180pF.

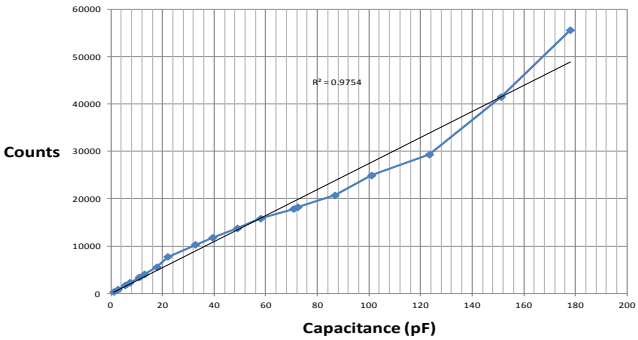
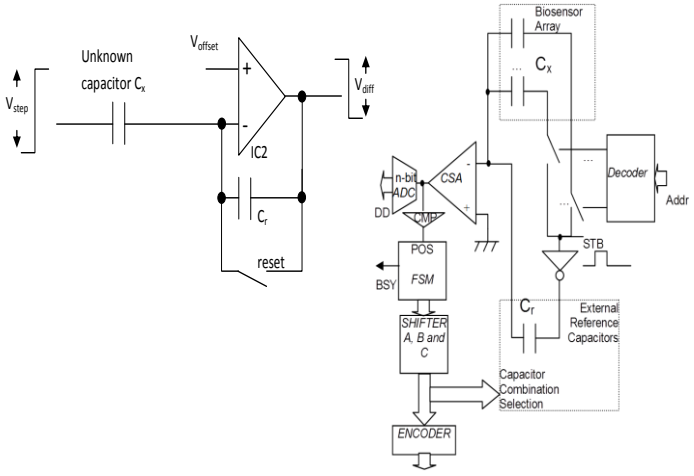


Figure 5. Linearity in the capacitance range covered.

IV. Extension of the Capacitance Range



(a) (b)

Figure 6. Direct Charge Measurement [7] (a) and the biosensor readout system with extended capacitance range

The unknown capacitance C_x can be estimated by its difference or ratio with a known reference capacitor C_r as shown for example in Fig. 6a [4][7]. The capacitance range covered by the architecture described in Section II can be extended if the block architecture shown in Fig. 6b is used. The C_x in Fig. 6a can be measured as (see [7]): $C_x = -V_{diff} C_r / V_{step}$. In this case higher linearity can be achieved if the unknown capacitor C_x is close to C_r and thus, the covered capacitance range depends on the C_r value.

The digital way to form a configurable external reference capacitor C_r in the context of the circuit shown in Fig. 6b, is briefly described in this section. If an input capacitance range of 640pF is adequate and C_r should not have a difference higher than 10pF from C_x, the C_r value can be selected as a multiple of 10pF between 0 and 630pF. These C_r values can be expressed in a radix-4 numerical system representation with 3 digits as:

$$C_r = (b_2 4^2 + b_1 4^1 + b_0 4^0) \cdot 10\,pF \qquad (4)$$

The digits b_2, b_1 and b_0 can be 0, 1, 2 or 3 and represent the reference capacitors of 4^2x10pF, 4^1x10pF and 4^0x10pF respectively that are connected in parallel by three Serial In Parallel Out shift registers (SHIFTER A, B and C of Fig. 6b). The A, B and C capacitor sets comprise of 3 identical capacitors each, with values 10, 40 and 160pF respectively. Numerical representations with different radix can also be defined to cover different input ranges.

TABLE I. RESOLUTION COMPARISON

Reference	**Resolution**	**Range**	**Conversion Time**	**Power Cons.**	**Area / process**
This Work (CTD)	Experimental= 3fF	20pF.. 180pF	1us to 163.84us	5 mW	0.04 mm^2 / 90nm
This Work (DCM)	3fF	640pF	(1 to 11) x (1us to 163.84us)		
[1]	0.01%	10nF.. 50nF	Several ms		
[6]	1fF	10pF	100ms	2.2 mW	10 mm^2 /3um
[7]	0.5-6fF	5pF	176us		
[8]	65aF	10pF	20us	14.85 mW	2.6 mm^2 / 35nm

The potential gaps in the covered range stemming from the deviation of the external capacitor values from their typical ones, can be compensated using one additional capacitor in the A and B sets. Although the reference capacitance is still described in a radix-4 numerical system (see equation (4)), the digits b_1 and b_0 can now have 5 potential values (0-4) allowing the connection of up to 4 identical capacitors in parallel. In this way, a reference capacitance may have more than one representation (24 of the 64 reference values can be derived by more than one combination).

An 8-state Finite State Machine (FSM) evaluated on the Altera Cyclone III FPGA of a DK-Start3C25N development kit, can connect in parallel the appropriate external capacitors as follows: initially, all 160pF capacitors of the set C are connected in parallel (SHIFTER C output is preset to "111") and gradually disconnected (a '0' is shifted in SHIFTER C) until the unknown input capacitance C_x is found higher than the present C_r value. Then, all the 40pF capacitors of the set B are connected in parallel with the ones of the previous step and gradually disconnected until $C_x > C_r$. The same procedure is repeated for the 10pF capacitors of the set A.

The worst case delay introduced for the configuration of the reference C_r is 11 shifts. An 18-bit resolution is needed for 2.5fF accuracy by measuring the absolute capacitance while using the approach suggested in this section a 12-bit resolution is sufficient.

Table I compares the features of the proposed solutions with the referenced ones. As can be seen from this table the proposed solutions can cover a broad range of capacitance (only [1] has broader but it has a much worse resolution) with an absolute error (3fF) very close to the error that appears in approaches with much narrower range. Moreover, the area of the implemented solution is extremely low allowing the embedding of the presented readout circuit to other systems.

V. CONCLUSION

A biosensor readout system requiring only 0.04mm^2 of die area was implemented in CMOS TSMC 90 nm, capable of measuring 64 biosensors with an error below 3fF. The biosensor capacitance range is 180pF extendable to 640pF if a configurable reference capacitance scheme is adopted. A very good linearity (below 1 LSB) was achieved by applying averaging and piecewise linear approximation.

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