$\Sigma\Delta$ ADC with Fractional Sample Rate Conversion for Software Defined Radio Receiver

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***Abstract*—An analog-to-digital converter (ADC) in a software defined radio (SDR) receiver must be able to support the specifications of various wireless standards. It should also work with the low power supply voltage of CMOS circuits. A $\Sigma\Delta$ ADC is one of the solutions for the SDR receiver. However, the power consumption of the circuits, such as a lowpass filter (LPF) and a decimator after the $\Sigma\Delta$ modulator is large due to the high sampling speed.**

On the other hand, since a different wireless communication standard has a different master clock rate, it is necessary to provide the clock rate suitable for each standard. As a solution for the problem, direct insertion/deletion based sample rate conversion (SRC) has been proposed. Nevertheless, in order to apply this method to the $\Sigma\Delta$ ADC, the problem of the high clock speed in the circuits of the LPF after $\Sigma\Delta$ modulator remains.

In this paper, a novel $\Sigma\Delta$ ADC with fractional SRC is proposed. In the proposed scheme, SRC and filtering are combined. By filtering and decimating the output of the $\Sigma\Delta$ modulator in parallel with Q transversal filters the clock speed of the circuits of the SRC and the LPF can be reduced P times for Q/P SRC.

***Index Terms*—$\Sigma\Delta$ ADC, SDR, Fractional SRC, Direct Insertion/Deletion**

I. Introduction

Wireless telecommunication systems such as cellular phones, wireless LANs, or wireless broadband access systems have been developed rapidly, and various communication standards coexist in recent years. Under such circumstances, the demand for a receiver that can support multiple wireless communication standards with one terminal has been growing. One of the solutions is a software-defined radio (SDR) technology. The SDR allows a single terminal to support various kinds of wireless systems by changing software or hardware configurations [1–3].

An analog-to-digital converter (ADC) in the SDR receiver must be able to support the various requirements of the standards. From a viewpoint of silicon process development in recent years, the ADC for the SDR receiver should work with the low power supply voltage of CMOS circuits and, in response, the limited maximum input range as well. Because of the reduction of the input range, the input signal is more affected by noise generated in inner circuits. In order to reduce the noise in band, a $\Sigma\Delta$ modulator is one of the solutions for the SDR receiver [4–6]. The $\Sigma\Delta$ modulator has higher resolution than the other types of the ADC since it can remove the quantization noise in band through its noise shaping effect. In this architecture, by changing the oversampling rate (OSR), the bandwidth and the dynamic range of the ADC can be easily selected. However, the power consumption of the circuits, such as the lowpass filter and the decimator after the $\Sigma\Delta$ modulator is proportional to the OSR [7].

On the other hand, since a different wireless communication standard has a different master clock rate, it is necessary to provide the clock rate suitable for each standard. To resolve this issue with hardware, a complex analog circuit is inevitable. A solution to this problem is to provide different clock rates virtually by means of digital sample rate conversion (SRC) [8]. Especially, how to realize the fractional SRC is very important for the implementation of the SDR technology. Several methods for realizing fractional SRC has been proposed [9–12]. However, those methods have the problem of the high intermediate sample rate or very complex circuits. As a method that the high intermediate frequency is unnecessary and has low power consumption, direct insertion/deletion based SRC has been proposed in [13]. Nevertheless, in order to apply this method to the $\Sigma\Delta$ ADC, the problem of the high clock speed in the circuits of the lowpass filter (LPF) after $\Sigma\Delta$ modulator remains significant.

In this paper, a novel $\Sigma\Delta$ ADC with fractional SRC is proposed. In the proposed scheme, SRC and filtering are combined. By filtering and decimating the output of the $\Sigma\Delta$ modulator in parallel with Q transversal filters the clock speed of the circuits of the SRC and the LPF can be reduced P times for Q/P SRC.

This paper is organized as follows. Section II describes the conventional SRC scheme, and the proposed SRC scheme is presented in Section III. Numerical results through computer simulation are shown in Section IV. Finally, conclusions are presented in Section V.

II. Conventional System

Figure 1 shows a block diagram of a conventional system. The RF signal is converted to the 1 bit sequence in the $\Sigma\Delta$ modulator block at the clock speed of F. The output of the $\Sigma\Delta$ modulator is then put into the LPF for noise shaping. Suppose $x[n]$ is the nth output of the $\Sigma\Delta$ modulator and h_l is the lth coefficient of the LPF, the vector form of the $\Sigma\Delta$ modulator and the LPF coefficients are given as

$$\mathbf{x}[n] = [x[L-1+n]\ x[L-2+n]\ \cdots\ x[n]]^T, \qquad (1)$$

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and in a matrix form as

$$\mathbf{X}[n] = \begin{bmatrix} x[L-1+n] & x[L+n] & \cdots \\ x[L-2+n] & x[L-1+n] & \cdots \\ \vdots & \vdots & \vdots \\ x[n] & x[n+1] & \cdots \end{bmatrix}$$

$$= [\mathbf{x}[n]\ \mathbf{x}[n+1]\ \cdots]. \tag{2}$$

The coefficient of the filter is given as

$$\mathbf{h} = [h_0\ h_1\ h_2\ \cdots\ h_{L-1}]^T. \tag{3}$$

The output of the LPF is then calculated as

$$\begin{aligned} &\mathbf{Y}_c \\ &= [y[n]\ y[n+1]\ y[n+2]\ \cdots] \qquad (4) \\ &= \mathbf{h}\mathbf{X}[n] \\ &= [h_0\ h_1\ h_2\ \cdots\ h_{L-1}] \begin{bmatrix} x[L-1+n] & x[L+n] & x[L+1+n] & \cdots \\ x[L-2+n] & x[L-1+n] & x[L+n] & \cdots \\ \vdots & \vdots & \vdots & \cdots \\ x[0] & x[1] & x[2] & \cdots \end{bmatrix} \qquad (5) \end{aligned}$$

where $y[n]$ is the nth output of the LPF.

The conventional structure of the LPF is shown in Fig. 2. The input sample of the filter is put into the 1 bit shift register. Since the output of the $\Sigma\Delta$ modulator is either 0 or 1 and it selects one of the coefficient $\{+h_l\ or\ -h_l\}$ [14]. Therefore, no multiplication is required in this filter. The filtered signal of Eq. (5) is put into the SRC block. The output signal after $(N+\alpha)/N$ direct insertion SRC is given as

$$z[k] = y\left[\left\lfloor \frac{kN+\alpha R}{N+\alpha} \right\rfloor\right] \tag{6}$$

where k is an integer as the index of $z[k]$, $\lfloor\gamma\rfloor$ denotes the maximum integer that does not exceed γ.

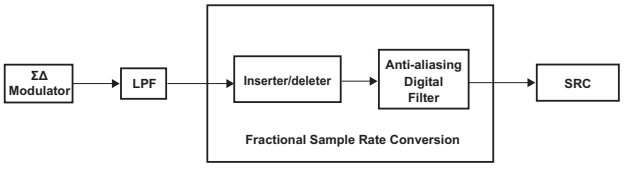

Fig. 1. Conventional system with separated $\Sigma\Delta$ ADC and SRC.

III. Proposed System

Figure 3 shows the structure of the proposed $\Sigma\Delta$ ADC. The input signal is converted to a 1 bit sequence at a high OSR, and the noise shaping and SRC are carried out at the same time. For instance, in the case of the decimation from 300 MHz to 40 MHz, the sample rate is converted with the rate of 2/15. In order to decimate with the conversion rate of Q/P, $(P-Q)$ samples are eliminated every P samples of the LPF outputs. The interval between the Q remaining samples should be maximized in order to minimize the noise caused by direct deletion [15]. The decimated samples are then represented as the following equation.

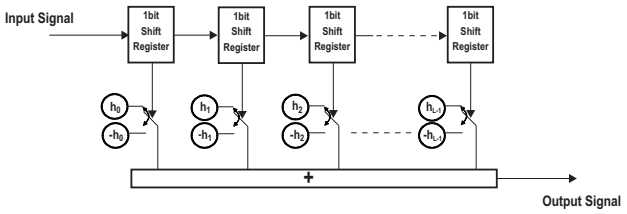

Fig. 2. Structure of conventional LPF.

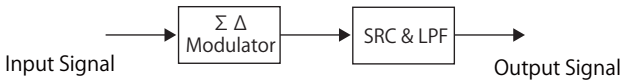

Fig. 3. Block diagram of proposed system with combined $\Sigma\Delta$ ADC and SRC.

$$\mathbf{Y}_p = \left[\mathbf{y}_p^T[0]\ \mathbf{y}_p^T[P]\ \mathbf{y}_p^T[2P]\ \cdots\right] \tag{7}$$

where

$$\mathbf{y}_p[iP] = \left[y[iP]\ y[iP+\lfloor P/Q\rfloor]\ \cdots\ y[iP+\lfloor (Q-1)P/Q\rfloor]\right]^T \tag{8}$$

for an integer i. $\mathbf{Y}_p$ is rearranged as

$$\begin{aligned} &\mathbf{Y}'_p \\ &= \left[\mathbf{y}_p[0]\ \mathbf{y}_p[P]\ \mathbf{y}_p[2P]\ \cdots\right] \qquad (9) \\ &= [\mathbf{H}]^T \begin{bmatrix} \mathbf{x}[0] & \mathbf{x}[P] & \cdots & \mathbf{x}[iP] & \cdots \\ \mathbf{x}[\lfloor P/Q\rfloor] & \mathbf{x}[\lfloor P/Q\rfloor+P] & \cdots & \mathbf{x}[\lfloor P/Q\rfloor+iP] & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \mathbf{x}[\lfloor (Q-1)P/Q\rfloor] & \mathbf{x}[\lfloor (Q-1)P/Q\rfloor+P] & \cdots & \mathbf{x}[\lfloor (Q-1)P/Q\rfloor+iP] & \cdots \end{bmatrix} \qquad (10) \end{aligned}$$

where $\mathbf{H}$ is the $1 \times LQ$ vector given as

TABLE I
OPERATION COST OF LPF AND SRC

	Proposed scheme	Conventional scheme
Number of multipliers	0	0
Clock speed of multipliers	-	-
Number of adders	$Q(L-1)$	$(L-1)$
Clock speed of adders	F/P MHz	F MHz

$$\mathbf{H} = \left[\mathbf{h}^T\ \mathbf{h}^T\ \cdots\ \mathbf{h}^T\right]^T. \tag{11}$$

Figure 4 shows the details of the filter structure for SRC. The binary samples are fed into Q branches. On each branch $\lfloor iP/Q \rfloor$ samples delay is added where i is an integer with the condition of $1 \leq i \leq Q-1$ and stored in the P bit shift register. The samples in the P bit shift register is transferred to the P bit latch circuit in every F/P clocks. Thus, the coefficients of the filter on each branch is selected and summed every F/P clocks. The selector at the outputs of the filters sequentially selects the branches at every F/P clocks. Therefore, the sample rate is converted to Q/P.

No multiplier is required in the proposed structure while switches are required to select the filter coefficients. However, the clock speed of the filters can be reduced P times as compared to the conventional filter structure. The difference of the calculation cost between the conventional and proposed schemes is listed in Table I.

IV. Numerical Results

A. MSE characteristics

Based on the simulation model shown in Fig. 5, the MSE performance of the conventional and proposed converters is obtained. In the simulation, the MSE is obtained by calculating the difference between the direct samples of the input sinusoidal wave and the converted samples. The simulation conditions with the sinusoidal signal are shown in Table II. Figure 5(a) shows the simulation model of the conventional system, which has the second-order $\Sigma\Delta$ modulator. The input signal is sampled at 300 MHz and modulated by the $\Sigma\Delta$ modulator. The output of the modulator is put into the LPF for noise shaping. The output of the LPF is then upsampled from 300 MHz to 360 MHz by direct insertion with the conversion rate of 6/5 and decimated to 40 MHz [13]. Figure 5(b) shows the simulation model of the proposed system. The input signal is sampled and modulated by the $\Sigma\Delta$ modulator at 300 MHz, and decimated to 40 MHz by the proposed SRC. The input of the system is sinusoidal signals from 0 MHz to 10 MHz. The LPF is a root cosine rolloff filter with the 20 MHz signal bandwidth and the rolloff factor of 0. The MSE is calculated between the converted signal and the sinusoidal signal sampled at 40 MHz. The MSE performance is shown in Fig. 6. Figure 6 shows that both the conventional and proposed converters achieve almost the same MSE regardless of the input signal frequency.

B. BER Performance

For bit error rate (BER) evaluation of the proposed scheme an OFDM signal is employed. The simulation conditions for the OFDM signal are shown in Table III. The BER vs. E_b/N_o is calculated with QPSK-OFDM and 64QAM-OFDM signals. The number of subcarriers is 64 and the bandwidth is 20 MHz. The BER curves are shown in Figs. 7 and 8. Both of the BER curves with QPSK and 64QAM are close to the theoretical performance.

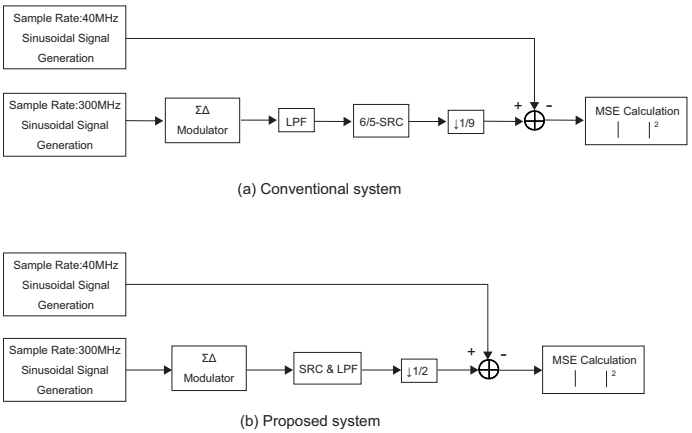

Fig. 5. MSE simulation model ((a)Conventional system,(b)Proposed system).

TABLE II
MSE SIMULATION CONDITIONS

Number of bits of the $\Sigma\Delta$ modulator	1
Order of the $\Sigma\Delta$ modulator	2
Output after D/A conversion in the $\Sigma\Delta$ modulator	$\pm$ 1
Input signal	Sinusoidal wave
Amplitude of input signal	$\pm$ 0.5 max.
Input signal frequency [MHz]	0-10
Sample rate of the $\Sigma\Delta$ modulator [MHz]	300
Sample rate after SRC [MHz]	40
LPF	Root cosine
Rolloff factor	0
Bandwidth [MHz]	20
Order of LPF	91

V. Conclusions

In this paper, the novel $\Sigma\Delta$ ADC with fractional SRC has been proposed. In the proposed scheme, SRC and filtering are combined. By filtering and decimating the output of the $\Sigma\Delta$ modulator in parallel with Q transversal filters the clock speed of the circuits of the SRC and the LPF can be reduced P times for Q/P SRC. The numerical results through computer simulation have shown that the proposed scheme achieves

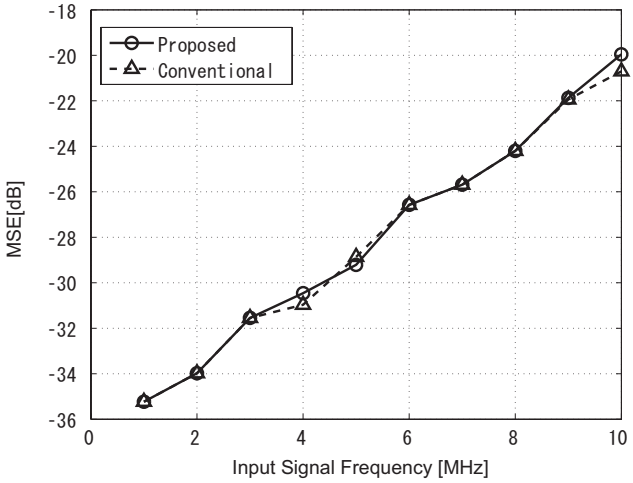

Fig. 6. MSE vs. input signal frequency.

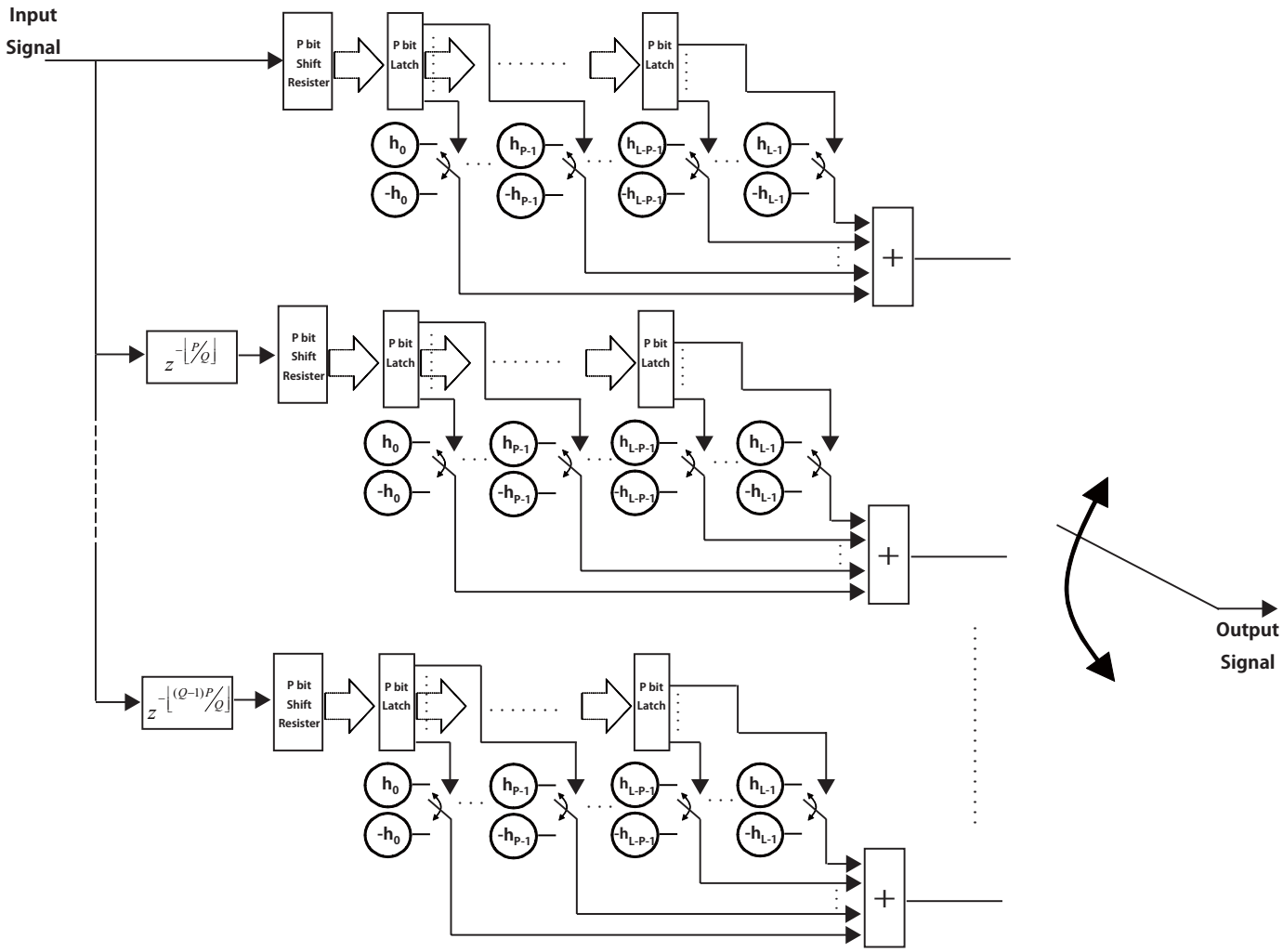

Fig. 4. Proposed SRC and LPF structure.

TABLE III
BER SIMULATION CONDITIONS

Input signal	QPSK-OFDM, 64QAM-OFDM
Number of bits of the $\Sigma\Delta$ modulator	1
Order of the $\Sigma\Delta$ modulator	2
Output after D/A conversion in the $\Sigma\Delta$ modulator	$\pm$ 1
Number of DFT points	64
Number of subcarriers	64
Number of data subcarriers	48
Bandwidth [MHz]	20
Sample rate of the $\Sigma\Delta$ modulator [MHz]	300
Sample rate after SRC [MHz]	40
LPF	Root cosine
Rolloff factor	0
Bandwidth [MHz]	20
Filter length	91
Number of trials [OFDM symbols]	10000

almost the same performance as the conventional scheme with the lower clock speed in the SRC and LPF circuits.

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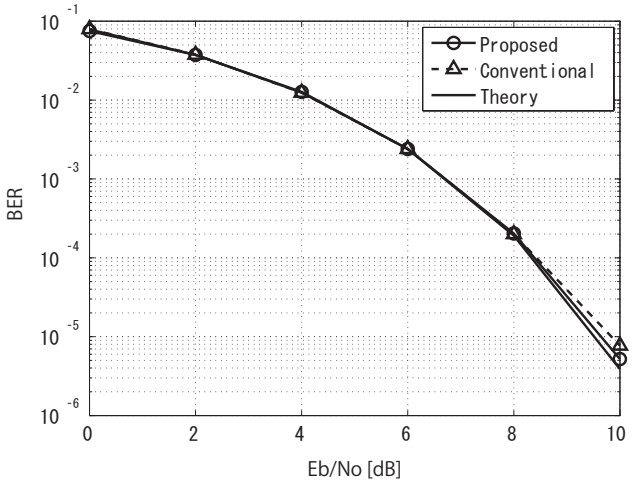

Fig. 7. BER vs. E_b/N_o (QPSK-OFDM).

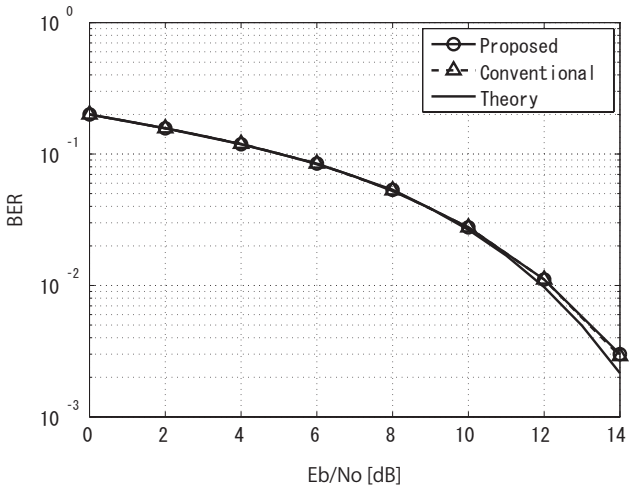

Fig. 8. BER vs. E_b/N_o (64QAM-OFDM).

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