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Seven Level Symmetric Cascaded H-Bridge Multilevel Inverter for Solar Photovoltaic System

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Abstract

Among different types of Non-Conventional Energy Sources, Solar Power has become highly prominent with exhausting suitable to innovation in Power Electronic Systems. The primary intention of the advised performance must limit the number of switches to enhance the output waveforms with a preferred harmonic profile. This topology moderates the estimate about switches, isolated DC origin, expenditure, and intensity of the circuit substantially as correlated to other topologies. The proposed method uses the MPPT approach to exploit the maximum energy from solar photovoltaic to load entirely. The Proposed method provides almost sinusoidal output waveforms by developing a few power switches. The SPV arrangement was simulated and constitution through SPV arrays, a DC-DC buck converter, and a sliding mode MPPT regulation. Based on the cascaded H-Bridge multilevel converters, The strong constraint enforced confined DC voltage sources considering separately Cascaded H-Bridge. This constitution converter worth along with diminishing the constancy based on the system. The system gives boosting voltages with improves the harmonic profile. Performance of the arrangement demonstrated in MATLAB SIMULINK as well as PROTEUS.

Keywords: Cascaded H-Bridge (CHB) Inverter, Multilevel Inverter (MLI), Bidirectional Switches, Pulse Width Modulation (PWM), Fuzzy Controller, Non-Conventional Energy.

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1. Introduction

In current years, countries everywhere the globe carry their awareness against globalization. One of the origins persists traditional fossil fuel-based power reproducing sources and acquires to turn into severe consideration [1]. With the use of non-conventional power supplies related to wind, solar, geothermal, etc., solar photovoltaic (SPV) arrangements persist as a highly significant power resource [2]. Also, it retains collected enough consideration appropriate to the analysis with progress in the invention of SPV cells [3]. Power electronic converter equipment is essential for generating PV supply, which diminishes the expenditure and upgrades the system competence [4].

Multilevel Inverter (MLI) carries vast superiority over traditional inverters in behalf of reduced switching losses, lower voltage stress crosswise along lower Electromagnetic Interference (EMI) [5]. Mainly, there persist three fundamental categorize of Multilevel Inverter: Neutral point Clamped MLI, Flying Capacitor MLI, and CHBMLI [6]. Figure 1 appearance the arrangement made from the Multilevel Inverter [7]. Neutral point Clamped MLI subsist like clamping diodes that boost the voltage levels. The capacitor is associated in sequence as voltage compensatory [8]. The indicated produces an enormous complication for the appliance. In Flying Capacitor MLI, extended clamping capacitors (CC) remain associated, so the voltage compensatory is complicated [9]. Cascaded H-Bridge MLI is appropriate for immense voltage operation, being separate H-bridge subsist of four switches and one DC source. CC, as well as diodes, are never used here [10]. Cascaded H-Bridge MLI Topology conditional simultaneous DC resource subsist of Single DC supply and Multiple DC supply [11]. In Single DC supply, the Cascaded H-Bridge MLI persist associated in parallel as a consequence, through the production containing separate CHB, the subsided frequency transformer is coupled [12]. Through expanding the 'n' statistic of levels, the Transformer is diluted, being various H-bridge inverters [13]. Such that every ability based on arrangement power inclines less. The Cascaded H-Bridge MLI in numerous DC Sources is associated in series [14]. The considerable H-bridge with DC source amplifies the 'n' amount of output voltage levels [15]. To condense the switches in that topology, the Symmetrical and Asymmetrical Cascaded H-Bridge MLI are tested [16].

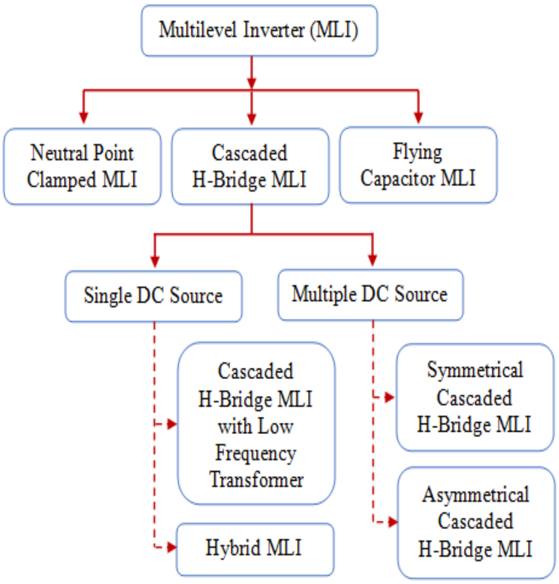


Figure 1. Arrangement of Multilevel Inverter (MLI)

MLI has been stimulating in the modern generation in considering academicians and corporations in the contemporary existence used for medium and high voltage utilization [17]. The MLI carry acquired significant concern for their competence with high power appliances [18]. The recognition of MLI is immense power quality, lesser order harmonic, reduced switching losses, along with enhanced electromagnetic interference [19]. These MLI produce a stepped inverter waveform through several input voltages connection in the input process with a suitable layout of power semiconductor devices [20]. The foremost intention of MLI is to preserve nearly sinusoidal output waveforms along with sustaining the power quality [21].

The MLI is not alone reaches a high power standard, although facilitating the acceptance of non-conventional power systems [22]. In non-conventional power sources acting as solar, wind, and fuel cell can incorporating into an MLI method for high power appliances. A lot of MLI topologies has-been developed [23]. The introductory approach of an MLI is to produce a power quality directed toward adopting a severe of power semiconductor switches among considerably reduced voltage DC supply toward achieving the potential transformation through staircase voltage waveforms [24].

The MLI achieves high voltages among low harmonic distortion without adopting transformers [25]. The numeral of voltage level expansion simultaneously harmonic content based on the output voltage waveform contraction substantially [26]. MLIs are more extravagant expected to a higher number of capacitors, and extra clamping diodes are mandatory when the level is immense, and the enormous number of DC sources are essential [27]. To conquer these raised obstacles worn by modified H-bridge inverter for medium and high power appliances [28].

2. Solar Photovoltaic Cell
2.1 Solar PV Modelling

Sunlight intensity is one of the necessary sustainable continuity supplies that is absolute, inexhaustible, and hygienic. Solar PV production is operating away to be continuously crucial in their no fuel worth, not contaminating less conservation. It is correspondingly an apprehensive source based on effort. Therefore its most supervision point depends on the temperature and irradiance [29]. The erection segment of solar photovoltaic performance is necessarily a 'p-n semiconductor' junction with it V-I aspect is inclined through,

$$"I = I_{sc} - I_0\left\{exp\left(\frac{q(v+R_sI)}{nKT_k}\right)-1\right\}\frac{v+R_sI}{R_{sh}}"$$

"Where,
V, I is Output Voltage and Current of Solar PV Cell
R_s, R_{sh} is series and shunt resistance of PV Cell
q is Electronic Charge
I_{sc} is light generated current
I_0 is Reverse Saturation current
n is a dimensionless factor
k is Boltzmann constant
T_k is the temperature in ^{0}K"

The circuit representation attributed to the SPV unit as illustrated in figure 2

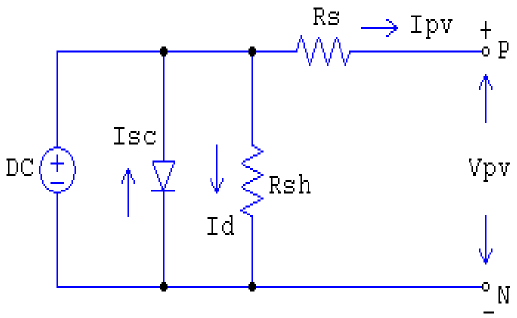


Figure 2. The Symbolic layout of solar PV Cell

2.2 Effect of Variation of Photovoltaic Irradiation

A solar PV cell's P-V and I-V tendency is highly vulnerable on the photovoltaic irradiation character, as illustrated in figures 3 & 4. The photovoltaic irradiation in the process of a decision of the environmental variation possess on fluctuating, although supervision appliance is accessible a particular track this conversion also be able to vary the functioning of the photovoltaic cell to appropriate the prescribed load demands [30]. Higher is the photovoltaic irradiation, and the open-circuit voltage is elevated, which is expected to be inflation of photovoltaic irradiation. This is compensation to the certainty that, when enhanced sunshine circumstance on the Photovoltaic cell, the electrons are providing for greater excitation power, with rising the electron mobility, better energy is produced.

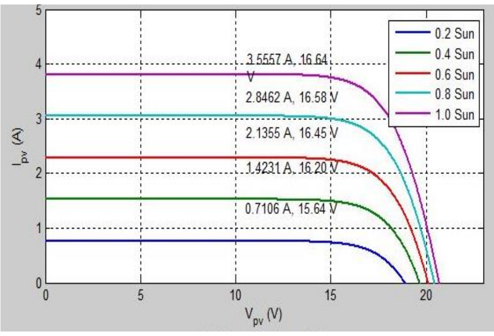


Figure 3. I-V Characteristics of SPV System

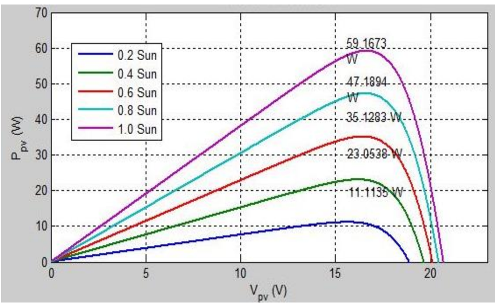


Figure 4. P-V Characteristics of SPV System

2.3 Maximum Power Point Tracking

Maximum Power Point Tracking (MPPT) obtain the most acceptable approach toward achieving valuable probable effectiveness products considering automatic alteration related to the solar PV system. There is a steady switch in surface elements, such as temperature and irradiance, that compose the constant alternation containing V-I curvation, this one upward or else downward. Modification in temperature at variance correlatively to the output voltage with variation in irradiance power impact output current. MPPT carries various approaches related to Fuzzy logic as a consequence of neural networks other off contingents that if an essential power execution structure is needed, the best scenario is to be adopted Fuzzy rule base and Perturb and Observe (P&O).

2.4 MPPT Based Fuzzy Logic Controller

Fuzzy logic is effortless with vigorous than a traditional PI controller. It is the proper stand-in considering the typical controller. The fuzzy logic controller (FLC) subsists fuzzification, inference, and defuzzification. The voltage with various modern voltage based on the suggested arrangement has been input with duty cycle being the boost converter stand investigated in the process of output. The fuzzy rule base has been worked in the process of exposure within the table position row performs voltage with column produce varies in voltage. The rule base subsists of 7-membership functions as both inputs together with output. Altogether forty-nine rules worked toward acquiring the enhanced duty cycle for the alternation in the information, as illustrated in table 1.

Table 1. Rule Table of Fuzzy Logic

E → / Δe ↓	NB	NS	Z	PS	PB
NB	Z	Z	NB	NB	NS
NS	Z	Z	NS	NS	NS
Z	NS	Z	Z	Z	PS
PS	PS	PS	Z	Z	Z
PB	PB	PB	PB	Z	Z

3. Proposed Technology

The extension consisting of the designed MLI expands the levels, including exploiting a specific fewer count of switches, reduced capacitors, lower sources with fewer diodes for developing the power quality. The boost converters (DC to DC) are interdependent among PV arrays with loads.

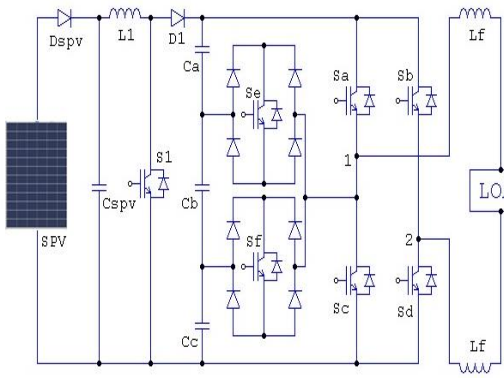


Figure 5. Proposed 1Ø Seven Level Cascaded H-Bridge MLI for SPV system

MPPT subsist of power electronic components with its conduct situated on duty cycles. The boost converters develop immense voltages from Photovoltaic Panel producing a low voltage in solar PV panel than the load voltage. Huge voltages persist significantly to inspire a specific solar PV array to load power, appropriate for the proposed inverters with filters. The suggested complex subsist of a 1∅ traditional CHB inverter, two bi-directional switches, and capacitor voltage divider worked through C_a, C_b, and C_c in the exposure process in figure 5. The hybrid inverter topology effectively obtains uniquely one DC source with lower power switches, limited capacitors, and lower power diodes than the MLI comparatively diode clamped, flying capacitors & cascaded inverter.

The SPV panel is associated with load over boost converter can build up the voltages in altered MLI without transformer and decline the total harmonic distortion (THD). Require switching concerning the MLI can supply 7-output voltage levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, 0*, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$).

4. Modes of Performance

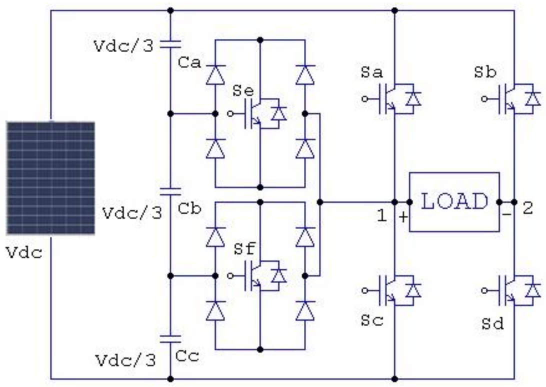


Figure 6. Seven Level MLI for Switching Performance

Single-phase (1∅) proposed Cascaded H–Bridge 7-level inverter subsist of two bidirectional switches with a capacitor is voltage divider worked through C_a, C_b and C_c being presented in figure 6. The proposed topology typically promises functions by MLI corresponding as fewer power switches, biased diodes, and reduced capacitors considering the equivalent representation of levels. Solar PV systems are associated with compound inverters over bidirectional switches. Solar PV combination is commencing lesser voltages with it enhance the voltages through boost converter without adopting of auxiliary apparatus. This inverter progresses the power and power factor is conveyed to load. Accurate switching from the inverter can generate 7-output voltage levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, 0^*, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$) against DC supply voltage.

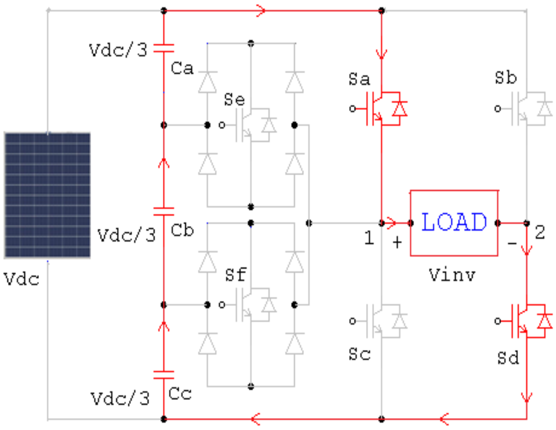
The seven-level inverter process can obtain split within 7-switching states in the process of presented in figure 7 (i), (ii), (iii), (iv), (v), (vi), (vii) & (viii). Imperative of 7-level output voltages were induced as follows.

1) *Maximum positive(+Ve) output Voltage (V_{dc}):* The electrical energy diagonal by capacitance C_a, C_b & C_c is V_{dc} with the power adopted toward the load is V_{dc}. The contribution energy V_{dc} is linked among load '1' +Ve terminal whereas IGBT composed switch S_a is turned ON along with the load '2' -Ve terminal persists associated with the ground at IGBT Controlled switch S_d is turned ON along with resting IGBT Controlled switches stand in OFF position, figure 7 (i) indicate the behavior of current discharge in the layout through influential phase position.
2) *Two-Third +Ve output Voltage ($2V_{dc}/3$):* The electrical energy diagonal by capacitance C_b and C_c is $2V_{dc}/3$, with the power adopted toward the load being $2V_{dc}/3$. The contribution energy $2V_{dc}/3$ is linked with load '1' +Ve terminal whereas bidirectional IGBT controlled switch S_e is turned ON such that the current discharge over diode D_a and D_d with the load '2' negative terminal is associated by the ground at IGBT controlled switch S_d is turned ON along with resting IGBT controlled switches stand in OFF circumstance, figure 7 (ii) indicate the behavior of current discharge in the layout through influential phase position.
3) *One-Third +Ve output Voltage ($V_{dc}/3$):* The electrical energy diagonal by capacitance C_c is $V_{dc}/3$, with the power adopted toward the load being $V_{dc}/3$. The contribution energy $V_{dc}/3$ is linked with load '1' +Ve terminal whereas bidirectional IGBT controlled switch S_f is turned ON such that the current discharge over diode D_e and D_h with the load '2' -Ve terminal is associated with the ground at IGBT controlled switch S_d is turned ON along with resting IGBT controlled switches stand in OFF circumstance, figure 7 (iii) indicates the behavior of current discharge in the layout through influential phase position.
4) *Zero output Voltage (0 & 0*):* The zero output electrical energy level is made through turning ON IGBT controlled switch S_c, S_d either by turning ON IGBT controlled switch S_a, S_b with uninterrupted controlled switches as well as diodes stand in OFF position. When IGBT controlled switch S_c, S_d has turned ON, the current discharge over the load is a short circuit. The output energy by '1' and '2' terminal power is zero. Figures 7 (iv) & (v) indicate the behavior of current discharge in the circuit through influential phase position.
5) *One-Third negative (-Ve) output Voltage (– $V_{dc}/3$):* The electrical energy diagonal by capacitance C_a is $V_{dc}/3$. The input energy $V_{dc}/3$ act linked with load '2' -Ve terminal whereas IBGT controlled switch S_b is turned ON with the load '1' +Ve terminal is linked whereas bi-directional IGBT controlled switch S_e is turned

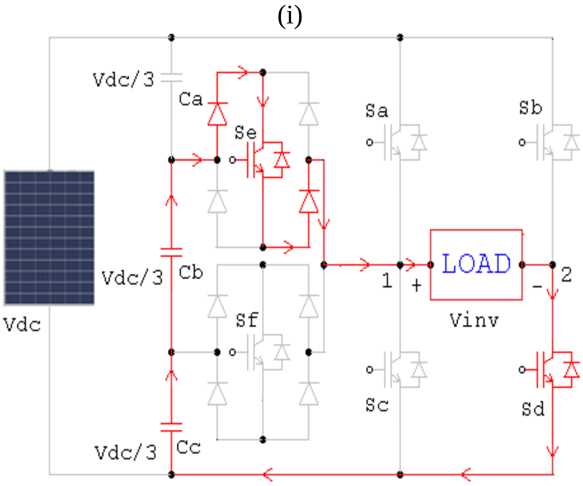
ON such that the current discharge over Diode D_c along with D_b and resting IGBT controlled switches are in OFF position, figure 7 (vi) indicates the behavior of current discharge in the layout through influential phase position.

6) *Two-Third -Ve output Voltage ($-2V_{dc}/3$):* The electrical energy diagonal by capacitance C_a and C_b is $2V_{dc}/3$. The input energy $2V_{dc}/3$ is linked by load '2' -Ve terminal. In contrast, IGBT controlled switch S_b turned ON with the load '1' +Ve terminal act combined whereas bi-directional IGBT controlled switch S_f is turned ON such that the current discharge over diode D_g and D_f and resting IGBT managed switches are in OFF position, figure 7 (vii) indicates the behavior regarding current release in the layout through influential phase position.

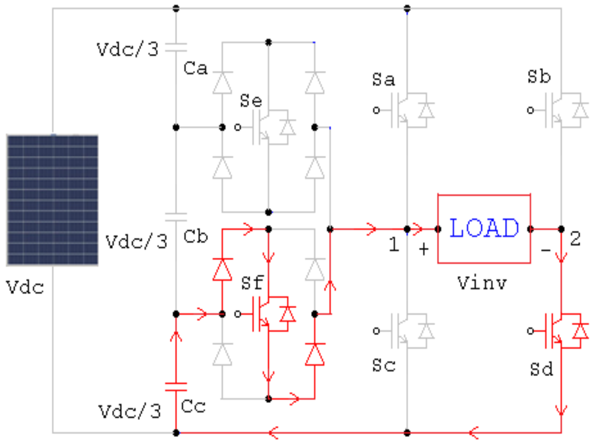
7) *Maximum -Ve output Voltage ($-V_{dc}$):* The electrical energy diagonal by capacitance C_a, C_b & C_c is V_{dc}. The input energy V_{dc} is linked through load '2' -Ve terminal when IGBT controlled switch S_b turned ON with the load '1' +Ve terminal is associated by IGBT controlled switch S_c is turned ON also resting IGBT switches are in OFF position, figure 7 (viii) indicates the behavior regarding current discharge in the layout through influential phase position.



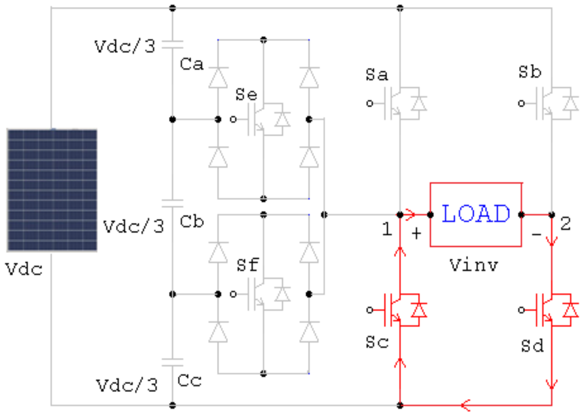
(i)



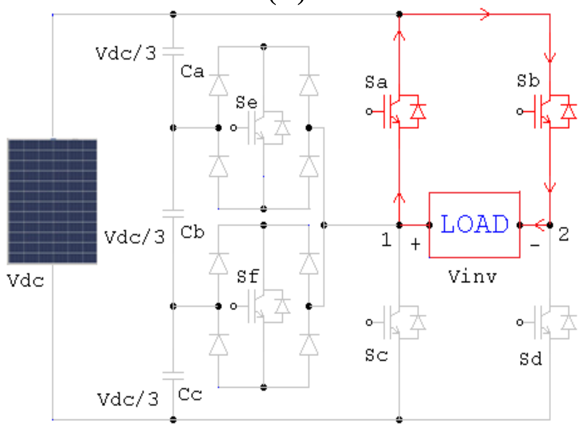
(ii)



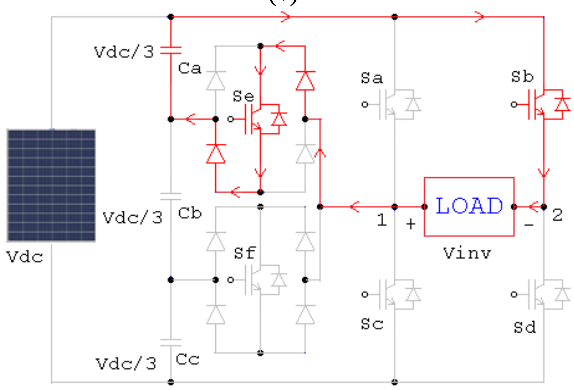
(iii)



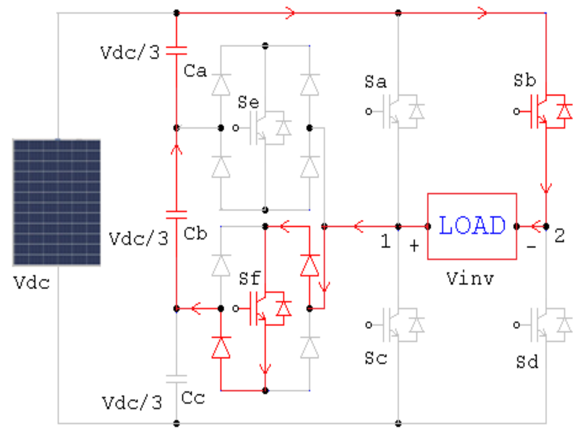
(iv)



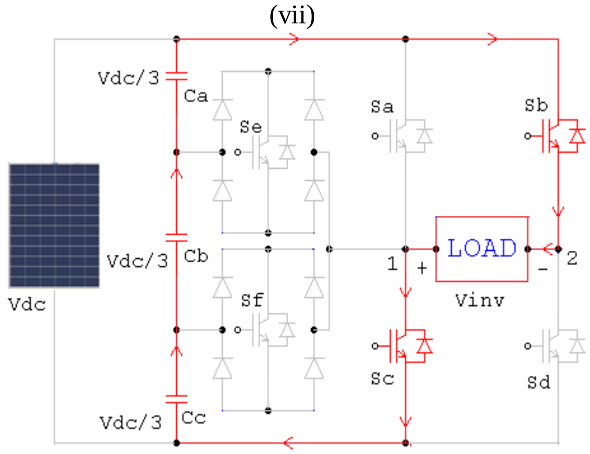
(v)



(vi)



(vii)



(viii)

Figure 7. Switch sequence appropriate to achieve the output voltage (V_{12}) (i) $V_{12} = V_{dc}$ (ii) $V_{12} = 2V_{dc}/3$ (iii) $V_{12} = V_{dc}/3$ (iv) $V_{12} = 0$ (v) $V_{12} = 0^*$ (vi) $V_{12} = -V_{dc}/3$ (vii) $V_{12} = -2V_{dc}/3$ (viii) $V_{12} = -V_{dc}$

Table 2. Output Voltage corresponding through the Switches ON-OFF mode

V_0	S_a	S_b	S_c	S_d	S_e	S_f
V_{dc}	√	-	-	√	-	-
$2V_{dc}/3$	-	-	-	√	√	-
$V_{dc}/3$	-	-	-	√	-	√
0	-	-	√	√	-	-
0^*	√	√	-	-	-	-
$-V_{dc}/3$	-	√	-	-	√	-
$-2V_{dc}/3$	-	√	-	-	-	√
$-V_{dc}$	-	√	√	-	-	-

Where,
√ indicates the Switch is ON
- indicates the Switch is OFF

Table 2 occurrence the switching sequence produced the seven-level output voltages (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, 0^*, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$) for switching arrangement for 1∅ CHB seven-level inverter in the process of exposed in figure 8.

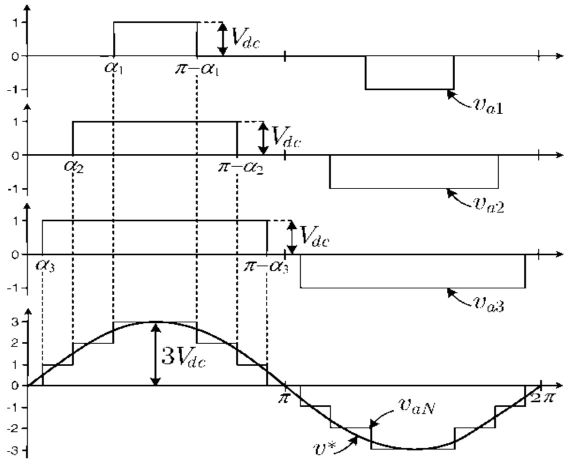


Figure 8. Switching sequence of 1∅ Modified 7-Level Inverter

5. Closed Loop Control Scheme

The closed-loop scheme contains MPP tracking, fuzzy controller, with inverter controller as presented in figure 9. The behaviour of MPPT is collecting the utmost extent of power from the solar PV system to load among improved harmonic profiles. The input parameters V_{pv}, I_{pv} of PV is given to an MPPT controller. The MPPT Controller controls the voltages along with current through duty cycles. The Pulse Width Modulation approach reproduces the pulse intern pulse stand to get back to the boost converter. The existing V_{dc} correlate for reference voltage V_{dc}* through fuzzy rule base combination by the fuzzy controller. To sustain the output of V_{dc} is inclined to load over inverter regulation among switches. The gating pulses persist delivered to switches in the inverter (S_a to S_f).

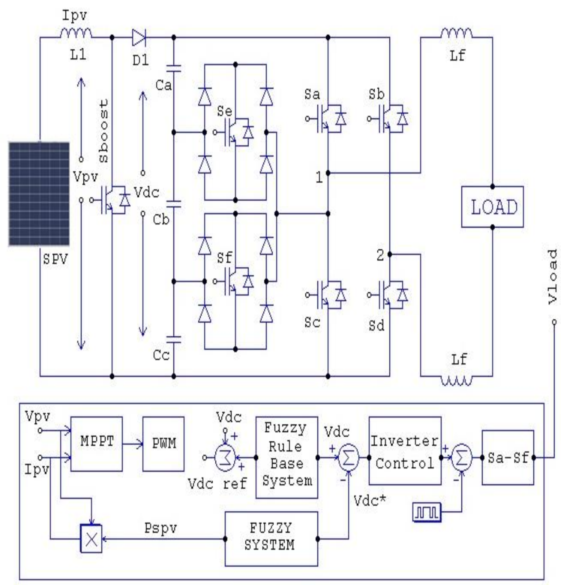


Figure 9. 1∅ Seven Level Inverter by Closed-Loop System

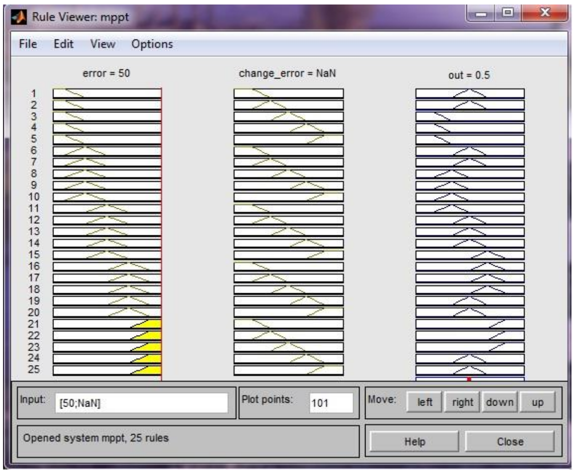


Figure 10. Fuzzy Rule Viewer for Closed-Loop System

6. Results
6.1 Simulation Result

This technique has been proved in MATLAB SIMULINK simulation results, as demonstrated in figure 11.

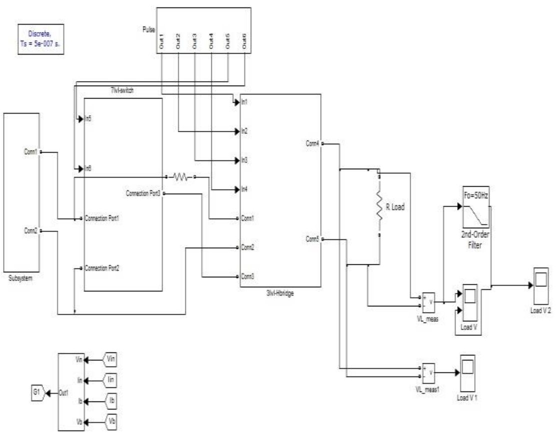


Figure 11. Simulation Circuit considering Modified H-Bridge Seven Level Inverter

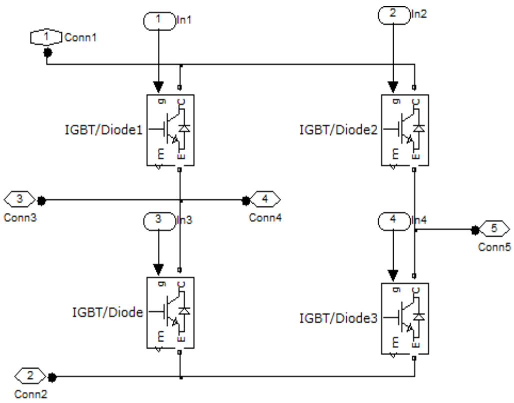


Figure 12. A Sub-system of Cascaded H-Bridge MLI

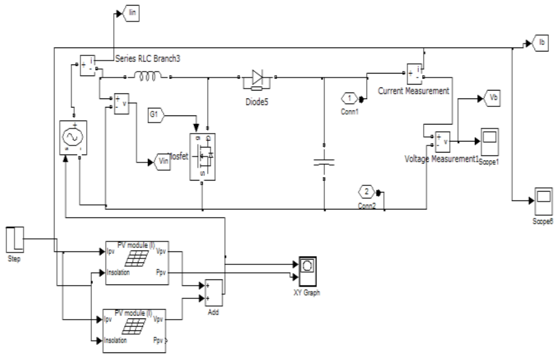


Figure 13. A Sub-system of MPPT Boost Converter

The sub-system of the seven-level CHB circuit is intended in figure 12. The MPPT Boost converter as the designed 7-level inverter is illuminated in figure 13. The output was switching pulses for switches S_a to S_f, as shown in figure 14.

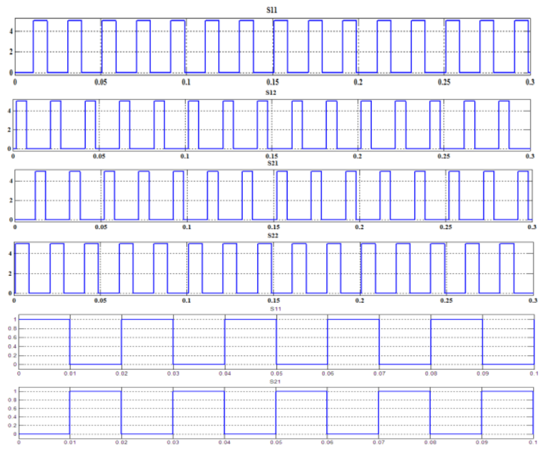


Figure 14. Switching pulses for Seven Level Inverter

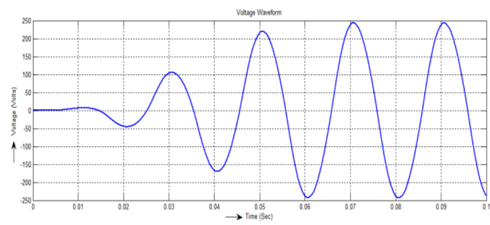


Figure 15. The Input Voltage waveform of 7-Level Inverter

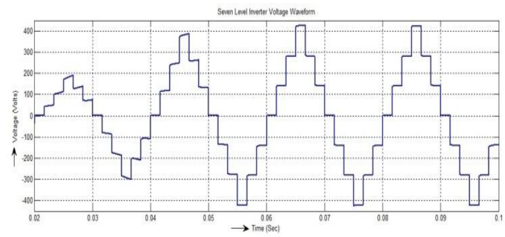


Figure 16. The Output Voltage waveform of 7-Level Inverter

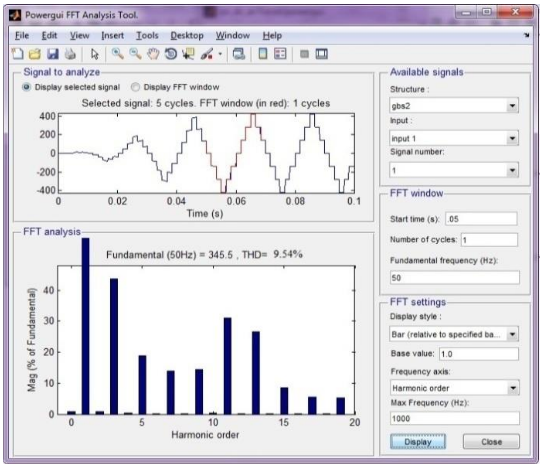


Figure 17. THD for Modified 7-Level Inverter

The input voltage waveform based on the 7-level inverter is characterized in figure 15, and the output voltage waveform made from the 7-level inverter is represented in figure 16. The proposed system's THD is 9.54%, as disposed of in figure 17.

6.2 PROTEUS Model

Proteus is an isolated function for generous execution modules contribution varied convenience, i.e., graphic representation, Printed Circuit Board layout. The proposed 7-level inverter is converted during the Proteus spreadsheet, drawing the extended apparatus competence with the PIC micro-controller schedule. Results obtain recognized future equivalent to facilitate MATLAB SIMULINK. The proposed 7-level inverter is imitated in Proteus operating system, in the act demonstrated in figure 18.

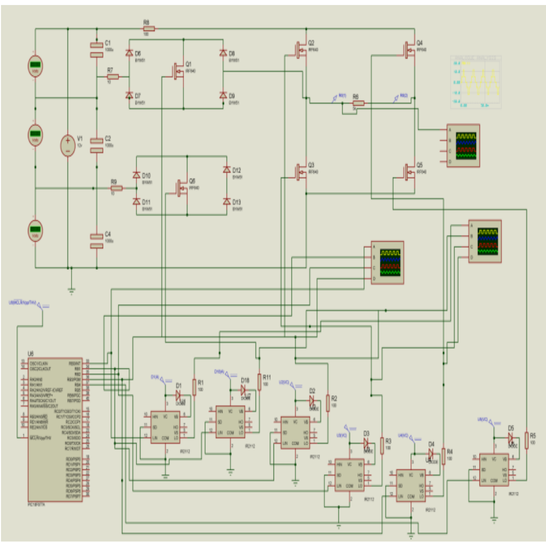


Figure 18. Schematic of Modified Seven-Level Inverter using PROTEUS Software

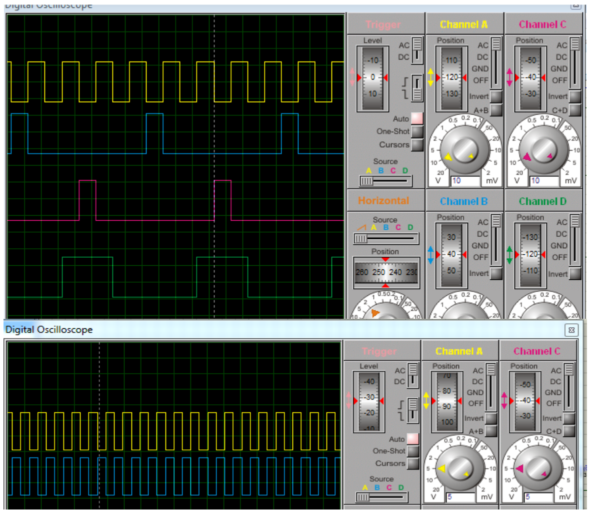


Figure 19. Output switching Pulses for 7-Level Inverter

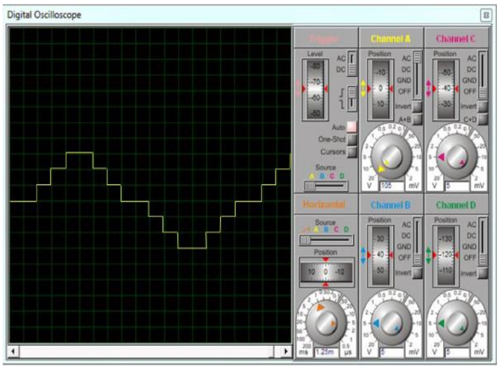


Figure 20. Output Voltage for Modified 7-Level Inverter using Proteus software

The output switching Pulse for switches S_a, S_b, S_c, S_d, S_e & S_f, as illustrated in figure 19 and figure 20, demonstrates the output voltage as the designed 7-level inverter in the Proteus model.

7. Conclusion

The designed 1Ø modified 7-level inverter produces approximately sinusoidal output waveforms that exploit a small number of power switches. This proposed system is fulfilled in all conditions like fewer capacitors, single DC supply, small filter size, and improved harmonic profiles than the other MLIs. This arrangement provides boosting voltages along with enhancing the power quality. MLI is enriched against improving technology through a well-established, attractive medium and high power utilization intention. However, the continuous progress related to devices with the expansion concerning modern utilization will permit a current challenge and opportunity to enhance MLI topology further. The achievement of the proposed combination is demonstrated by employing MATLAB/SIMULINK and PROTEUS Software.

References

[1] Ponraj, Ram Prakash, Titus Sigamani, and Vijayalakshmi Subramanian. "A Developed H-Bridge Cascaded Multilevel Inverter with Reduced Switch Count." Journal of Electrical Engineering & Technology 16, no. 3 (2021): 1445-1455.

[2] Shyam, D., K. Premkumar, T. Thamizhselvan, A. Nazar Ali, and M. Vishnu Priya. "Symmetrically modified laddered H-bridge multilevel inverter with reduced configurational parameters." International journal of engineering and advanced technology 9, no. 1 (2019).

[3] Yousofi-Darmian, Saeed, and S. Masoud Barakati. "A new asymmetric multilevel inverter with reduced number of components." IEEE Journal of Emerging and Selected Topics in Power Electronics 8, no. 4 (2019): 4333-4342.

[4] Jefry, Nur Atiqah, Law Kah Haw, and Wong Kiing Ing. "The New Topology of Multilevel Inverter with Reduced Number of Switches." In 2020 11th IEEE Control and System Graduate Research Colloquium (ICSGRC), pp. 94-99. IEEE, 2020.

[5] Maheswari, K. T., R. Bharanikumar, V. Arjun, R. Amrish, and M. Bhuvanesh. "A comprehensive review on cascaded H-bridge multilevel inverter for medium voltage high power applications." Materials Today: Proceedings 45 (2021): 2666-2670.

[6] Dhanamjayulu, C., Devalraju Prasad, Sanjeevikumar Padmanaban, Pandav Kiran Maroti, Jens Bo Holm-Nielsen, and Frede Blaabjerg. "Design and implementation of seventeen level inverter with reduced components." IEEE Access 9 (2021): 16746-16760.

[7] Sarwar, Adil, Md Irfan Sarwar, Md Shahbaz Alam, Seerin Ahmad, and Mohd Tariq. "A nine-level cascaded multilevel inverter with reduced switch count and lower harmonics." In Applications of Computing, Automation and Wireless Systems in Electrical Engineering, pp. 723-738. Springer, Singapore, 2019.

[8] Mahato, Bidyut, Saikat Majumdar, and Kartick Chandra Jana. "Single-phase Modified T-type–based multilevel inverter with reduced number of power electronic devices." International Transactions on Electrical Energy Systems 29, no. 11 (2019): e12097.

[9] Thiruvengadam, Annamalai. "An enhanced H-bridge multilevel inverter with reduced THD, conduction, and switching losses using sinusoidal tracking algorithm." Energies 12, no. 1 (2019): 81.

[10] Ponraj, Ram Prakash, and Titus Sigamani. "A novel design and performance improvement of symmetric multilevel inverter with reduced switches using genetic algorithm." Soft Computing 25, no. 6 (2021): 4597-4607.

[11] Bana, Prabhat Ranjan, Kaibalya Prasad Panda, Sanjeevikumar Padmanaban, and Gayadhar Panda. "Extendable switched-capacitor multilevel inverter with reduced number of components and self-balancing capacitors." IEEE Transactions on Industry Applications 57, no. 3 (2020): 3154-3163.

[12] Kumar, Satish, and M. Sasi Kumar. "Asymmetric hybrid multilevel inverter with reduced harmonic using hybrid modulation technique." International Journal of Power Electronics and Drive Systems 11, no. 2 (2020): 605.

[13] Chavali, Punya Sekhar, PV Ramana Rao, and M. Uma Vani. "A Novel Multilevel Inverter with Reduced Number of Switches Using Simplified PWM Technique." Journal of The Institution of Engineers (India): Series B 101, no. 3 (2020): 203-216.

[14] Chlaihawi, Amer, Adnan Sabbar, and Hur Jedi. "A high-performance multilevel inverter with reduced power electronic devices." International Journal of Power Electronics and Drive Systems 11, no. 4 (2020): 1883.

[15] Pradhan, Ajoya Kumar, Sanjeeb Kumar Kar, Mahendra Kumar Mohanty, and Navneet Behra. "Design and simulation of cascaded and hybrid multilevel inverter with reduced number of semiconductor switches." International Journal of Ambient Energy 42, no. 8 (2021): 950-960.

[16] Muralikumar, Kola, and P. Ponnambalam. "Analysis of Cascaded Multilevel Inverter with a Reduced Number of Switches for Reduction of Total Harmonic Distortion." IETE Journal of Research (2020): 1-14.

[17] Abhilash, Tirupathi, Kirubakaran Annamalai, and Somasekhar Veeramraju Tirumala. "A seven-level VSI with a front-end cascaded three-level inverter and flying-capacitor-fed H-bridge." IEEE Transactions on Industry Applications 55, no. 6 (2019): 6073-6088.

[18] Ali, Ahmed Ismail M., Mahmoud A. Sayed, and Ahmed AS Mohamed. "Seven-Level Inverter with Reduced Switches for PV System Supporting Home-Grid and EV Charger." Energies 14, no. 9 (2021): 2718.

[19] Sandhu, Mamatha, and Tilak Thakur. "Modified cascaded H-bridge multilevel inverter for hybrid renewable energy applications." IETE Journal of Research (2020): 1-13.

[20] Bhanutej, J. N., and Rani Chinnappa Naidu. "A 7-level inverter with less number of switches for grid-tied PV applications." International Journal of Advanced Technology and Engineering Exploration 8, no. 78 (2021): 631.

[21] Mehta, Shivinder, and Vinod Puri. "7 Level New Modified Cascade H Bridge Multilevel inverter with Modified PWM controlled technique." In 2021 11th IEEE International Conference on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS), vol. 1, pp. 560-565. IEEE, 2021.

[22] Ali, A. Nazar, R. Jai Ganesh, D. Sivamani, and D. Shyam. "Solar powered highly efficient Seven-level inverter with switched Capacitors." In IOP Conference Series: Materials Science and Engineering, vol. 906, no. 1, p. 012014. IOP Publishing, 2020.

[23] Prem, Ponnusamy, Vidyasagar Sugavanam, Ahamed Ibrahim Abubakar, Jagabar Sathik Mohamed Ali, Boopathi C. Sengodan, Vijayakumar Krishnasamy, and Sanjeevikumar Padmanaban. "A novel cross-connected multilevel inverter topology for higher number of voltage levels with reduced switch count." International Transactions on Electrical Energy Systems 30, no. 6 (2020).

[24] Seifi, Ali, Majid Hosseinpour, Abdolmajid Dejamkhooy, and Farzad Sedaghati. "Novel reduced switch-count structure for symmetric/asymmetric cascaded multilevel inverter." Arabian Journal for Science and Engineering 45 (2020): 6687-6700.

[25] Siddique, Marif Daula, Muhyaddin Rawa, Saad Mekhilef, and Noraisyah Mohamed Shah. "A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources." International Journal of Electrical Power & Energy Systems 128 (2021): 106730.

[26] Sakile, Rajakumar, A. Bhanuchandar, Kasoju Bharath Kumar, Dongari Vamshy, Bandela Supriya, and Kowstubha Palle. "A Nearest Level Control Scheme for Reduced Switch Count Cascaded Half-Bridge Based Multilevel DC Link Inverter Topology." In 2021 8th

International Conference on Signal Processing and Integrated Networks (SPIN), pp. 287-292. IEEE, 2021.
[27] Shunmugham Vanaja, Dishore, Albert Alexander Stonier, and Ali Moghassemi. "A novel control topology for grid integration with modular multilevel inverter." International Transactions on Electrical Energy Systems 31, no. 12 (2021): e13135.
[28] Pratomo, Leonardus Heru, and Slamet Riyadi. "Design and implementation of a single-phase five-level inverter using a DC Source with voltage balancer on capacitor." International Journal of Power Electronics and Drive Systems 12, no. 2 (2021): 902.
[29] Ahmad, Marwan E., Ali H. Numan, and Dhari Y. Mahmood. "Enhancing performance of grid-connected photovoltaic systems based on three-phase five-level cascaded inverter." International Journal of Power Electronics and Drive Systems (IJPEDS) 12, no. 4 (2021): 2295-2304.
[30] Hosseini Montazer, Babak, Javad Olamaei, Majid Hosseinpour, and Babak Mozafari. "A generalized diode containing bidirectional topology for multilevel inverter with reduced switches and power loss." International Journal of Circuit Theory and Applications 49, no. 9 (2021): 2959-2978.