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Design and Comparison of SEU Tolerant 10T Memory Cell for Radiation Environment Applications

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Abstract

Single event upsets (SEUs), which are caused by radiation particles, have emerged as a significant concern in aircraft applications. Soft mistakes, which manifest as corruption of data in memory chips and circuit faults, are mostly produced by SEUs. The utilization of SEUs can have both advantageous and detrimental effects in some critical memory applications. Nevertheless, in adherence to design principles, Radiation-Hardening-By-Design (RHBD) methodologies have been employed to mitigate the impact of soft mistakes in memory. This study presents a novel memory cell design, referred to as a Robust 10T memory cell, which aims to improve dependability in the context of aerospace radiation environments. The proposed design has several advantages, including reduced area, low power consumption, good stability, and a decreased number of transistors. Simulations were conducted using the TSMC 65nm CMO technology, employing the Tanner tool. The parameters of the RHB 10T cell were measured and afterwards compared to those of the 12T memory cell. The findings obtained from the simulation demonstrate that the performance of the 10T memory cell surpasses that of the 12T memory cell.

Keywords: Single Event Upset , Memory Chip, CMOS, 10T Memory cell

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1. Introduction

Memory applications in digital circuits are complicated by SEU. Soft mistakes must be reduced to preserve radiation-sensitive memories. Radiation particles cause SEU, which corrupts memory chips and permanently damages circuits, causing electronic system failure. Radiation-Hardening-By-Design approaches accommodate soft memory errors. RHBD uses commercial Complementary Metal-Oxide-Semiconductor foundry processes without any process or design changes that would violate standards.

Static Random Access Memory-based Field Programmable Gate Arrays have been widely used in recent decades. Due to its instability, SRAM cannot be used in FPGA systems that require strong security and fast power-on. Non-Volatile Memories address these issues. Traditional NVM devices like anti-fuse, E2PROM, and flash require high voltage and have limited logic compatibility. These devices limit logic density and raise FPGA integration costs. Emerging NVMs like MRAM, PRAM, and RRAM are scalable and logic compatible.

The author proposes a single-ended 6T SRAM cell [1]. This design seeks to reduce dynamic power usage during read and write operations by approximately 50%. This reduction is believed to be possible without increasing read and write latency or standby power usage. The shortened read access time range shows the design's ability to endure process changes. A prior work [2] presented soft error protected 10T SRAM cells with two variations that improved static noise margin (SNM) and low-voltage functioning. The study found that the NMOS stacked-10T cell had better read stability margin and soft

error resistance than a normal 6T SRAM cell without protection. This evaluation used a 0.18µm standard CMOS technology for a Single Event Transient (SET) scenario.

A prior study evaluated Dual Dice architecture, which uses two Dice storage cells [3]. This architecture plan strengthens the system against multi-node disturbances. To optimize space, 4-interleaving dual dice cells are used during planning. The invention of an 11T SRAM cell [4] has improved leakage, stability, and read/write stability. The authors reduced static power via two cross-coupled inverters and a footer transistor. The scientists published the 22nm CMOS Double Node Upset Resilient Latch [5]. The latch links three single-node upset robust cells. Three Muller C-elements feedback in each cell. A basic soft-error-tolerant embedded memory construction method was reported in [6]. A four-transistor dynamic memory core with CDMR memory helped store complementary data values internally.

A new RHBD 12T memory cell [7] can withstand single and multiple node upsets. [8] reviewed power-gated 9T (PG9T) SRAM cell implementation. Power gating transistors and read decoupled access buffers permitted read and write operations in this system. The proposed 9T SRAM had mild error immunity from bit interleaving. In a previous study [9], a 7T cell with dynamic writing capabilities and sub-threshold operation from 0.4V was described. This design addressed 6T and 7T memory cell issues. The Monte-Carlo simulator CORIMS was used to analyse and approximate terrestrial neutron-induced soft-errors in SRAMs in [10]. SRAMs from 250 to 22 nm were examined.

The study [11] compared EDAC to three FPGA-based EDAC technologies. The authors analysed SEU and MBU statistically. Error detection in difference-set cyclic codes reduced memory access time [12]. An RHBD12 radiation-resistant memory cell was introduced in a prior study [13]. This memory cell uses 12 transistors and 65nm CMOS technology seen in commercial applications. HSPICE uses 12 transistors on commercial 65-nm CMOS technology to simulate. Several HSPICE post-simulations examined RHD12 and other advanced memory cells. In [14], researchers introduced two novel SRAM cells with better characteristics and single-event multiple effect resilience.

OLS codes were utilized to construct an efficient parity prediction system that could find flaws in individual circuit nodes [15]. A unique RHBD SRAM bit-cell was proposed in [16] employing Single Event Upsets' polarity upset technique. Previous research [17] created a radiation-hardened memory cell. Transistor sizes improve memory cell stability in space radiation with this architecture. A radiation-hardened quarto 10T memory cell was previously reported [18]. This memory cell was multi-node robust and immune to single-node upset. A new SRAM cell architecture increases power efficiency, stability, spatial requirements, and soft error resilience [19]. An FPGA memory architecture that tolerates single-event upsets was developed [20]. This architecture's multi-bit upset prevention was tested on two prototype FPGAs with and without SEU hardening. Radiation Hardened by Polar Design (RHPD) 12T SRAM cells were introduced in [21] to reduce n-channel Metal Oxide Semiconductor single event transient voltage. The recommended architecture improves SRAM cell endurance and speed, especially for space applications, using a polarity update mechanism.

Due to radiation, normal memory cells perform poorly at higher temperatures. The 10T memory cell is designed to survive high radiation levels in aerospace applications. In high-radiation conditions, 12T memory cells are less efficient than 10T ones. This study's low power consumption, small footprint, efficiency, and transistor count are its main advantages. The paper will have the following outline: Radiation Hardened by Design is explored in greater detail in Section 2. Section 3 elaborates on the design of a 12T SRAM memory cell, whereas Section 4 discusses the design of a 10T SRAM memory cell. The findings from the experiments are presented and discussed in Section 5. The research is summarized in Section 6.

2. Radiation Hardened by Design

Electronic components and systems are made via radiation hardening. These systems are resilient to ionizing radiation, especially in high altitudes, nuclear reactors, particle accelerators, and nuclear incidents. Radiation-hardened semiconductor electronics components are designed and produced similarly to non-hardened components, but with some alterations. Radiation hardened components must be improved and rigorously tested to create a radiation-resistant microelectronic chip design.

2.1. Radiation-Hardening Techniques

2.1.1 Physical

Toughened chips often use insulating substrates instead of semiconductor wafers. Many people use Silicon On Sapphire and Silicon On Insulator silicon. Commercial chips can survive 50–100 gray (5–10 kilorads) radiation. Space-specific SOI and SOS chips have hundreds of times the radiation tolerance of silicon devices. Radiation-hardened 4000 series semiconductors were introduced in one continuous development period. Radiation-induced effects are more likely in bipolar integrated circuits than in CMOS circuits. The LS 5400 series of low-power Schottky devices has a tolerance of 1000 krad, while other ECL devices have 10,000 krad. MRAM is the best rewritable, radiation-hardened, and non-volatile conductor

memory solution. According to fundamental physics and preliminary experiments, MRAM resists ionization-induced data loss. A radiation shielding system in the enclosure protects the instrument. SRAM replaces capacitor-based DRAM due to its longer lifespan. Silicon carbide and gallium nitride substrates with high band gaps resist deep level defects. Depleted boron is employed in the chips' borophosphosilicate glass passivation layer because of its quick neutron absorption and alpha decay.

2.1.1 Logical

In error-correcting memory systems, supplementary parity bits are employed to detect and potentially rectify corrupted data. The effects of radiation on memory retention are detrimental. Even during periods of system inactivity, a "scrubber" circuit is required to continuously perform the task of sweeping the RAM, extracting the data, verifying the parity for any data mistakes, and subsequently transmitting any necessary repairs back to the RAM.

At the level of the whole system, redundancy might be used. There are three separate microprocessor chips that may compute separately and then check their results against a standard calculation. If a system consistently generates results that are in the minority, it will be adjusted. It may be prudent to use rational means to begin the shutdown of a specific system if it keeps producing mistakes.

Redundant components can be utilized at the circuit level. In the context of data processing, it is possible to substitute three individual bits with a solitary bit, wherein each of the three bits possesses its own distinct "vote logic" mechanism to ascertain its real-time output. This approach is recommended solely for modest designs due to its propensity to amplify the chip design area by a factor of five. Nevertheless, one advantage of this approach is its inherent reliability in real-time scenarios. In the absence of a watchdog timer, the voting mechanism will persist in producing the correct outcome in the event of a single bit failure. Typically, the implementation of system-level voting across three distinct processing systems requires the inclusion of circuit level voting hardware.

When the watchdog timer detects that the system is not responding to normal control signals, such as a write operation initiated by the on-board CPU, it will perform a hard reset. The application routinely executes write operations to the watchdog timer to prevent the timer from timing out during normal operation. If the CPU fails due to radiation exposure, it is highly unlikely that the software will be able to restart the watchdog timer. A hard reset of the device will be required after the watchdog timer has run out. All other radiation hardening strategies have been exhausted, thus this is the last resort.

2.2 Sources of Severe Radiation

Ionizing radiation is found in Van Allen radiation belts, control electronics, nuclear reactors, spacecraft, chip packaging materials, and high-altitude airplanes. Protons (85%), alpha particles (14%), and heavy ions, x-rays, and gamma-rays (1%) make up cosmic rays, which come from diverse directions. The majority of collisions are caused by particles between 0.1 and 20 GeV. The Earth's atmosphere screens most of these particles, making them mostly hazardous for satellites and high-altitude airplanes. They can also harm ground-based computer systems. Solar particle events (SPEs) emit high-energy protons and heavy ions from the sun. X-rays usually follow these events.

The geomagnetic field confines electrons and protons up to 10 MeV in Van Allen radiation belts. Particle flow in distant locations from Earth fluctuates depending on Sun and magnetosphere conditions. Satellites worry about placement. Various radiation can interact with adjacent structures around electrical equipment, producing secondary particles. Neutron and gamma radiation from nuclear reactors can damage sensor and control circuits. Particle accelerators like the Large Hadron Collider generate high-energy protons and electrons, which damage delicate control and particle detector elements with an annual exposure of 10 MRad [Si].

Nuclear detonations produce electromagnetic, neutron, and charged particle radiation. During a nuclear war, electromagnetic pulses (EMPs) could damage civilian and military electronics. Radiation from chip packing materials caused soft errors in dynamic random-access memory (DRAM) chips in the early 1970s. Alpha particles are formed by minute amounts of radioactive chemicals in chip packing, sometimes discharging DRAM capacitors. The above effects have been reduced by using better packaging and error-correcting codes to fix DRAM problems.

2.3 Problem Caused by Radiation

Habitats subjected to high amounts of ionizing radiation have unique architectural challenges. A single charged particle can dislodge a large number of electrons, causing signal spikes and electrical noise. In the context of digital circuits, this could lead to garbled or incomprehensible results. The aforementioned subject is of paramount significance in the fields of spacecraft engineering, satellite technology, nuclear power plant building, military aircraft design, and nuclear weaponry. Manufacturers of military and aerospace electronics use radiation hardening techniques to make their products more resilient to the harsh environments in which they operate. The resulting systems feature radiation

hardening, sometimes known as rad-hardness or hardening.

3. 12T SRAM Memory Cell Design

3.1 Introduction

RHBD approaches using commercial CMOS foundry processes increased memory tolerance to mild faults without changing the process or design standards. These methods are usually divided into three categories: Layout-level solutions improve electronic device radiation resistance. The layout is adjusted using Annular-gate, T-gate, H-gate, and Shallow Trench Isolation (STI) schemes. The initial circuit-level solution to prevent memory and latch SEUs uses Triple Modular Redundancy (TMR). System-level error detection and correction codes (ECCs) accept fundamental faults. Compared to layout and system-level hardening, circuit-level RHBD memory design improves fault tolerance, temporal performance, and overheads. Thus, this study introduces a circuit-level RHBD 12T cell to improve resilience to single-event upsets.

3.2 Schematic of 12T SRAM Memory Cell

Figure 1 illustrates the proposed Redundant Half-Bit Differential 12T memory cell. The connection between the bit-lines and the output nodes is established by means of two access PMOS transistors. The state of being ON or OFF is determined by a word-line (WL). When radiation particles come into touch with a PMOS transistor, it leads to the generation of a positive transient pulse. Conversely, when radiation interacts with an NMOS transistor, it results in the production of a negative transient pulse.

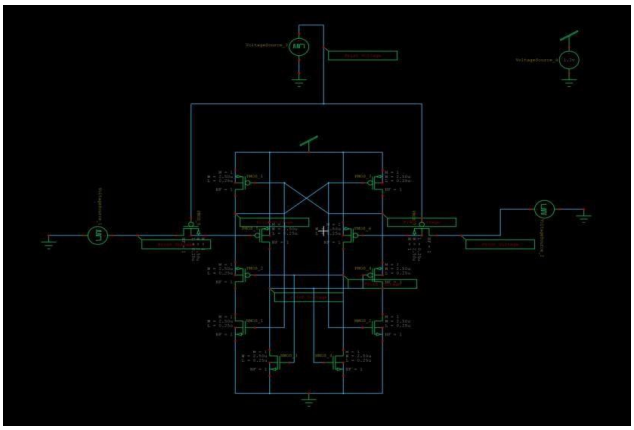

Figure 1. Schematic of 12T SRAM memory cell

4. 10T SRAM Memory Cell Design

4.1 10T SRAM Memory Cell

RHBD 10T memory cells have ten PMOS and NMOS transistors. The gates of NMOS access transistors are connected by a wordline. Thus, a high word line (WL) enables two access transistors for exclusive write and read operations. Two bit lines transfer the digital signal to the amplifier. Figure 2 shows the 10T SRAM memory cell.

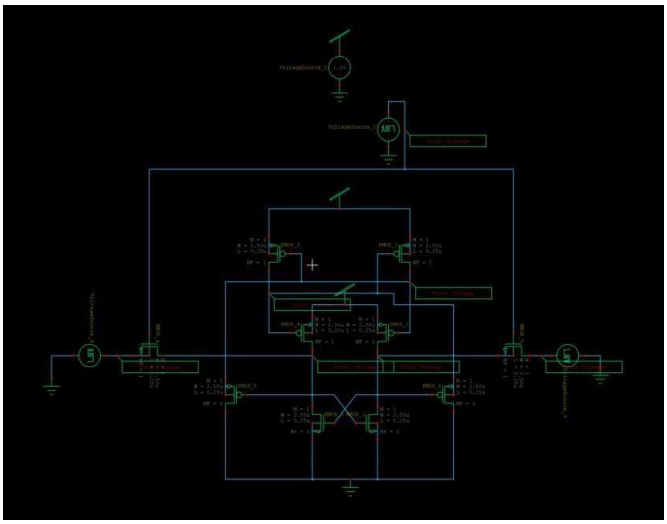

Figure 2. 10T SRAM cell schematic

4.2 Experimental Results and Discussion

4.2.1 Simulation Results of 12T SRAM Memory cell

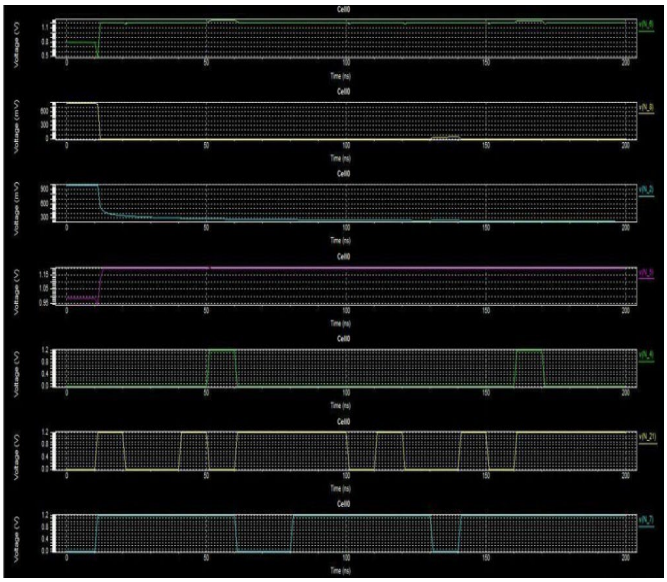

Figure 3. 12T SRAM Memory cell Read Write operations

Table 1 Power and Timing Analysis of 12T SRAM Memory cell

POWER ANALYSIS OF 12T SRAM MEMORY CELL	
Total power time	0 - 1e^{-009} s
Average power consumed	8.255343e^{-003} watts
TIMING ANALYSISOF 12T SRAM MEMORY CELL IN SECONDS	
Parsing	0.01
Setup	0.01
DC operating point	0.00
Transient analysis	0.00
Overhead	0.99
Total	1.01

4.2.2 Simulation Results of 10T SRAM Memory cell

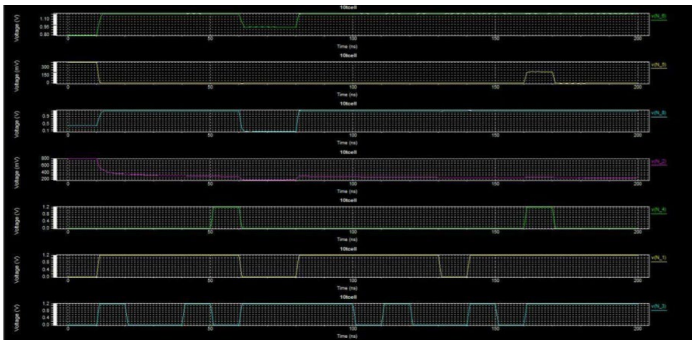

Figure 4. 10T SRAM Memory cell Waveform

Figure.4 describes the Read Write operations of 10T SRAM Memory ell.

Table 2 Power and Timing Analysis of 10T SRAM Memory cell

POWER ANALYSIS OF 10T SRAM MEMORY CELL	
Total power time	0 - 1e^{-008} s
Average power Consumed	1.460419e^{-002} watts
TIMING ANALYSISOF 10T SRAM MEMORY CELL IN SECONDS	
Parsing	0.01
Setup	0.01
DC operating point	0.05
Transient analysis	0.00
Overhead	0.06
Total	**0.13**

Table 3 Comparison of 10T and 12T SRAM Memory cell

Parameters	12T memory cell	10T memory cell
Time required	1.01 seconds	0.13 seconds
Power consumed	8mW	1mW
No.of transistors	12	10

Table 3 presents a comparative analysis of the 10T and 12T SRAM Memory cell, focusing on the use of transistors, power consumption, and time requirements. The comparison results indicate that the 10T memory cell exhibits greater efficiency than the 12T memory cell, as it consumes a lower power of 1mW in contrast to the 12T memory cell's power consumption of 8mW. Additionally, it should be noted that the 10T memory cell has a significantly shorter timing need of 0.13 seconds, in contrast to the 1.01 seconds required by the 12T memory cells. Additionally, it should be noted that the number of transistors needed is lower in the 10T configuration as compared to the 12T configuration.

5. Conclusion

This work presents the design of a RHBD 10T memory cell utilizing the TSMC 65nm CMOS technology. The design process is carried out using the Tanner tool. In contrast to the preceding hardened 10T memory cell, the suggested cell demonstrates the capability to rectify errors occurring in all sensitive nodes. The comparison is made between a 10T memory cell and the simulation results obtained for a 12T memory cell. The comparison results indicate that the 10T memory cell exhibits greater efficiency than the 12T memory cell in terms of power usage, reduced transistor count, and timing analysis. Therefore, it can be argued that the proposed RHBD 10T memory is a viable option for aerospace applications due to its ability to effectively manage performance, area, power, and reliability in radiation-intensive environments. The suggested memory cell design has several key applications in radiation environments, including spacecraft telemetry, processor scratchpad, flight data recorder, and payload data recorder.

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