A GaAs pHEMT MMIC Doherty Power Amplifier for 5G Mobile Handset

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Abstract. The design approach for a developed Doherty power amplifier (DPA) based on the WIN Semiconductors foundry's 0.1 m AlGaAs–InGaAs pHEMT technology is presented in this work. It is shown that altering a driver stage improves the DPA's gain performance. The wideband post-matching approach used here can minimise chip area while increasing average efficiency. The simulation results show that at 4V operation voltage, the monolithic drive load modulation PA produces a maximum output power of 29dBm at 1dB compression point. Over the frequency range of 25-27 GHz, the suggested DPA can give a 15dB power gain, as well as 35 percent PAE at peak power and 29 percent PAE at the 6dB OBO. The MMIC load modulation technique was created for 5G mobile handsets and takes up 4 mm2 of space.

Keywords: Doherty Power Amplifier, MMIC, mm-waves

1 Introduction

The unparalleled 5G evolution reshapes the wireless networks by optimizing the transceiver architectures, protocols and operations. For enhanced user experience and ultra-high speed services, the massive multiple-input multiple output (mMIMO) antennas at mm-wave spectrum are deployed that rely on the integrated RF front-end modules, including the power amplifier, filters, switches, phase shifter and various passives [1]. Moreover, advances in semiconductor technologies have resulted in promoting a cost-effective system. As a result of integration of several functions on a single chip, the space occupied by RF-Front-end is reduced attaining a compact transceiver system. Therefore, test and mounting costs have reduced and system reliability has improved. This degree of flexibility reflects the need for energy-aware power amplifier units.

Besides, as a result of employing phase-array MIMO antennas for spectrum efficiency improvement, the number of power amplifiers will be increased that place more stringent low power design requirements of a unit Power Amplifier (PA) at the emergence of a new radio frequency front-ends.

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On the other hand, anticipating wireless data traffic volume will require a spectrum bandwidth for connectivity [2]. Hence, wireless networks have already started deploying commercial 5G cellular network to accommodate the enormous expansion of data traffic by employing new frequency bands of mm-waves and the sub-6GHz spectrum. High-frequency spectrum is utilized in synergy with the multi-cellular topology for achieving improved wireless communication systems. This requirement propels the PA design towards wideband operating in contrast to 4G systems.

In battery-operated wireless communication systems such as mobile handset devices, the power saving is critical for longer battery lifetime. Since the PAs consume the largest portion of the current consumption budget, and the power and heat dissipation for the entire TX are determined by its power added efficiency (PAE) [3]. The PA's high power consumption is mostly attributable to two factors: the PA's limited attainable efficiency and the dynamic range within which it may achieve linear amplification. It is become an important enabler for energy-aware transmitter when deploying in a large amount of small and low power radios. The main research attention in 5G and beyond communication to overcome the daily re-charging issues of equipment has focused on low power consumption and elongated battery charge life duration. Among existing efficiency enhancement techniques, the dynamic load modulation Doherty PA (DPA) has become one of the most widely used Base-Stations (BSs) PAs market to maintain the modulated signals with high peak to average power ratio [4,5]. Based on good efficiency at deep power back-offs whilst enabling wideband operational capacity, DPA has been extensively explored to meet the 5G multimode applications.

This work develops a post matching DPA taking advantages of the MMIC technology, at mm-wave frequencies. Section 2 presents an optimized design procedure of a DPA based on the AlGaAs–InGaAs (pHEMT) process with high-yield 0.25-μm gate length on a 100-μm thick substrate. The circuit is designed using WIN process design kit. The large-signal simulation results of the two-stage DPA with a small supply voltage are presented in Section 2 as well. Some conclusion is discussed in Section 3.

2 Design Procedure of an Asymmetrical MMIC Doherty PA

2.1 Stability of the Device

It is paramount important to assure that no oscillation phenomena arise. In this work, an RC network can increase the input impedance of the device at the lower spectrum and provide a flat gain. The equivalent impedance of the stability at higher spectrum will be reduced by a shunt capacitor. Here, the compensation network consists of a TRF resistor and a MIM capacitor that can compensate the gain roll-off of the transistors in a wide frequency band. The K, Δ stability derived load and source factors [6,7] are shown in **Figure 1. (a,b)**.

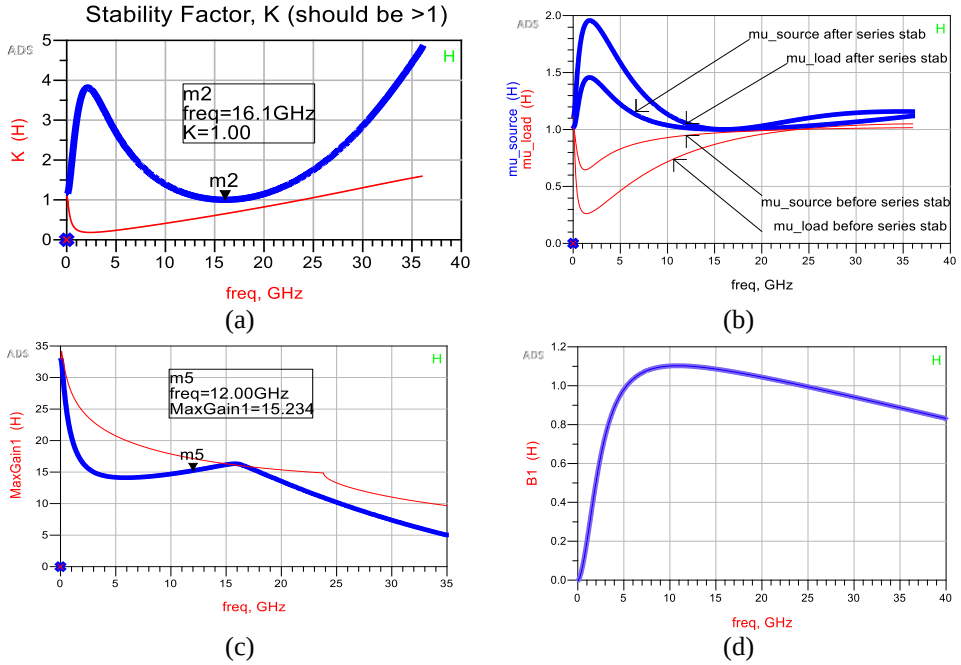


Fig. 1. Stability before (red) and after (blue) of the active cell, (a) K factor, (b) Mu factors. (c) MAG before (red) and after (blue) stabilizing (d) $|\Delta|$ factor.

Figure 1. (c plots the reduction of maximum available gain at the expense of preventing oscillations. **Figure 1. (d),** indicates that the stability is ensured by $|\Delta| > 0$ at all frequencies.

2.2 Matching Networks Design Flow

Figure 2 depicts the post-matching DPA technique that matches the load to lower impedance (Z_{sum}) towards the optimum impedances of main and peaking PAs. It is considered that main and peaking PAs are ideal current generators. In the symmetrical DPA the power ratio ($\beta = \frac{P_{sat\,peak}}{P_{sat\,main}}$) must be equal to one that delivers the maximum 6dB BO efficiency as the BO= $20\log(\beta + 1) = 6dB$. Since the PAPR of a modulated signal is typically up to 8.5dB, an asymmetrical Doherty ($\beta > 1$) with larger back-off efficiency is more desired. The output current of the main and peaking PAs (i_p and i_m), have the similar power at ($i_p = \beta i_m$) saturation region, since the voltage is constant, therefore, the add up impedance can be given by :

$$Z_{sum} = \frac{Z_m \cdot Z_p}{Z_m + Z_P} = \frac{\beta Z_p^2}{(\beta+1)Z_p} = \frac{\beta}{\beta+1} Z_p \qquad (1)$$

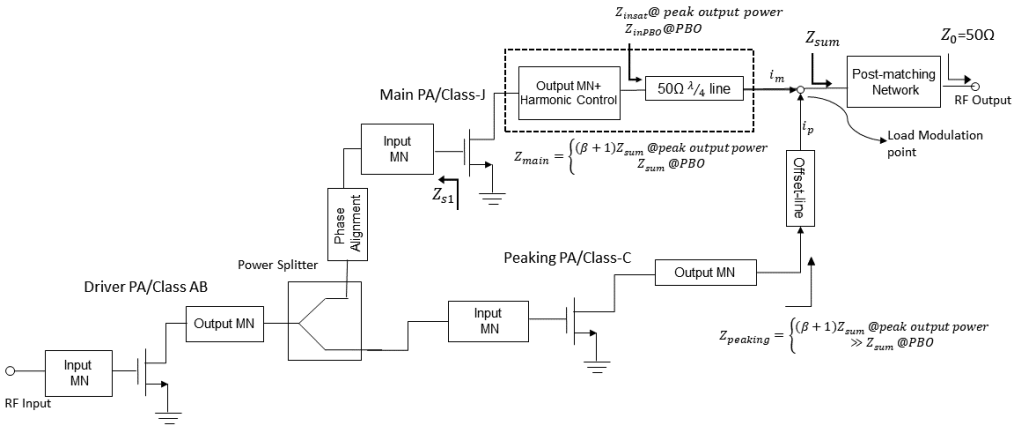


Fig. 2. The complete schematic of the proposed DPA.

Where the Z_p and Z_m are the optimum impedance of main and peaking PAs at the Doherty region. The Z_p , Z_m and the input impedance (Z_{insat}) of the impedance inverter can be obtained by,

$$Z_p = \frac{\beta+1}{\beta} Z_{sum} \tag{2}$$

$$Z_m = (\beta+1) Z_{sum} \tag{3}$$

$$Z_{insat} = \frac{(\beta+1)^2 {Z_{sum}}^2}{(\beta+1) Z_{sum}} = (\beta+1) Z_{sum} \tag{4}$$

The maximum output power of the main PA and the total output one ($P_{out,T}$) are obtained by,

$$P_{out,m} = \frac{1}{2} Z_m |i_m|^2 = \frac{\beta+1}{2} Z_{sum} |i_m|^2 \tag{5}$$

$$P_{out,T} = (\beta+1) P_{max,m} = \frac{(\beta+1)^2}{2} Z_{sum} |i_m|^2 \tag{6}$$

At the back-off the $Z_p = \infty$ and $i_p = 0$ therefore, the main PA impedance is $Z_{mod} = Z_{sum}$ and Z_{inBO} can be expressed as,

$$Z_{inBO} = \frac{(\beta+1)^2 {Z_{sum}}^2}{Z_{sum}} = (\beta+1)^2 Z_{sum} \tag{7}$$

The ratio between the load main PA impedance at the back-off (Z_{mod}) and at the peak (Z_m) where $Z_{inBO} = Z_{mod}$ and $Z_{insat} = Z_m$ are expressed by,

$$\Gamma = \frac{Z_{mod} - Z_m}{Z_{mod} + Z_m} = \frac{\big((\beta+1)^2 - (\beta+1)\big) Z_{sum}}{((\beta+1)^2 + (\beta+1)) Z_{sum}} = \frac{(\beta+1)\beta}{(\beta+1)(\beta+2)} = \frac{\beta}{\beta+2} \tag{8}$$

$$SWR = \frac{1+|\Gamma|}{1-|\Gamma|} = \frac{1+\frac{\beta}{\beta+2}}{1-\frac{\beta}{\beta+2}} = \frac{2\beta+2}{2} = \beta + 1 \quad (9)$$

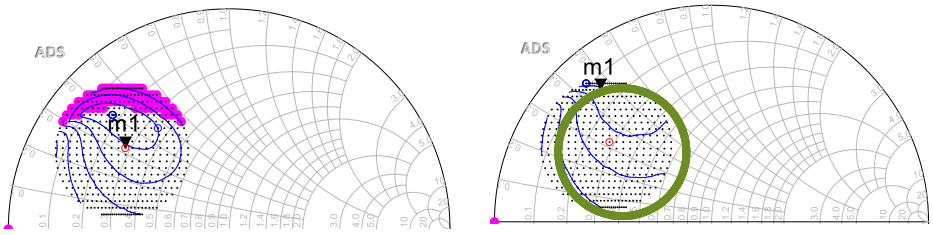
Therefore, the ratio of BO output power and saturated output power is given by (12):

$$i_{mBO} = \frac{i_m}{\beta+1} \quad (10)$$

$$P_{out,BO} = \frac{1}{2}(\beta+1)^2 Z_{sum} \cdot \left|\frac{i_m}{\beta+1}\right|^2 \quad (11)$$

$$\frac{P_{out,BO}}{P_{out,m}} = \frac{1}{(\beta+1)^2} \quad (12)$$

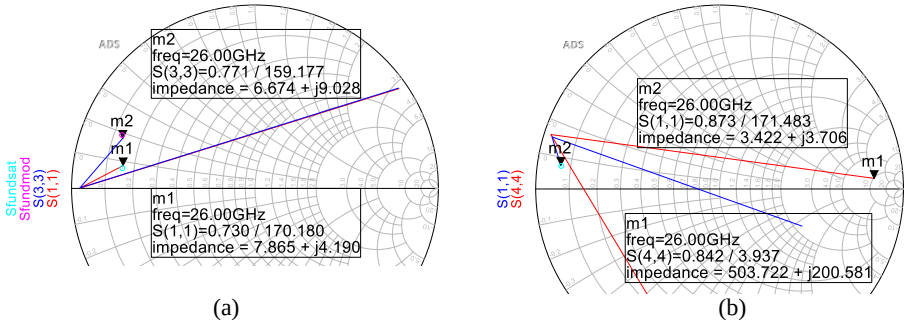
For maximum efficiency the load impedance when the device is compressed can be extracted using load-pull simulation. The load-pull simulation in **Figure 3. (a)** indicates that the best impedance at Z_m =7.8+j*4 **Ω** at 27dBm for the main PA output power. The main PA is biased at Class-B biasing condition of (-0.9V). Having obtained the efficiency and output power contours, the load-pull simulation is conducted at average output power of 24dBm, which is 6dB lower than the max o/p of 1W DPA. When the peaking PA is off, the load impedance of the main PA is determined by drawing VSWR $= \beta + 1$ circle [8]. The green circle of VSWR $=$ 2 in **Figure 3. (b)** is centered by Z_m helps to determine the Z_{mod}. The optimum impedance at the edge of VSWR circle and counters delivers the best compromise between gain and efficiency thus, the selected Z_{mod} is 6.6+j9 **Ω**.



(a) (b)

Fig. 3. Load-pull dataset of the main PA (a) at saturation (b) at the Back-off.

At the main path the output matching network (OMN) transfers the $2Z_{sum}$ to Z_m if β =1 in equation (3) and simultaneously it matches Z_{mod} to Z_{sum}. Here, $2Z_{sum}$ is selected to be 25-j*20 and the post-matching network matches this impedance to 50**Ω** load termination. The peaking PA only handels the signals at peak, therefore it requires an OMN to transfer the $2Z_{sum}$ to Z_p =3.4+j*3.7 at the saturation. The $2Z_{sum}$ impedance is identical for both devices and the Z_p is extracted by the load-pull simulation of the stabilized transistor for the peaking PA with the gate periphery of (8*100μm). The peaking PA is biased as Class-C (-1.6 V) conduction angle, so it starts to turn on at 6dB BO.



(a) (b)

Fig. 4. S-pars of the OMNs (a)Main and (b) Peaking PAs.

The Peaking PA is off at the lower power operation therefore, $Z_p$must be a very high impedance to prevent RF leakage, thus a delay line is embedded with the OMN of peaking PA. **Figure 4. (a, b)** respectively indicate the s-parameters results of designed OMN for Main PA and Peaking PA where the offset line is tuned for a high impedance of 500+j*200 Ω at BO. It should be noted that the phase delay imposed in peaking PA is necessary to compensate at the main PA to get the DPA output in-phase at the summing node. Hence, an offset line is placed at the main PA input path to align the phase. The main transistor input matching is computed to provide the conjugate match of the input impedance of Z_{in} = 2.4+j*19Ω and the IMN of peaking PA also transfers the conjugate of Z_{in}= 2.8+j*25Ω to the 50 Ω. Finally, asymmetrical Wilkinson power divider provides an in-phase flow of signal to both main and peaking PAs without loss.

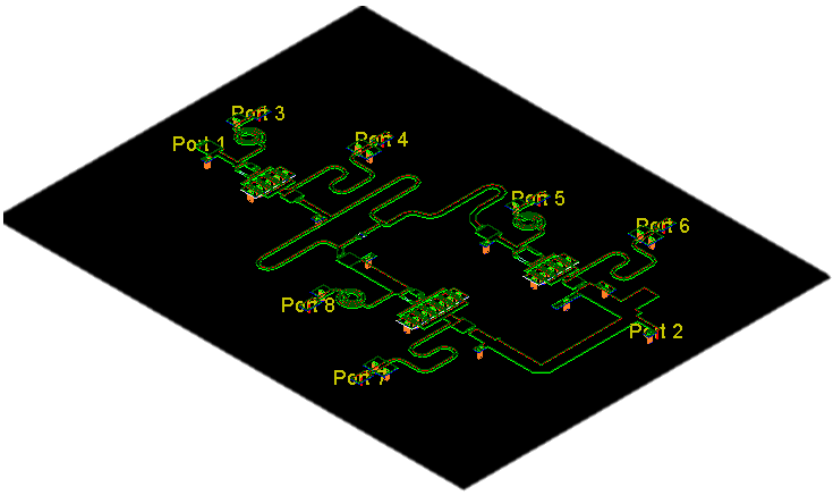


Fig. 5. The 3D review of complete MMIC DPA layout with die area size of $4mm^2$.

Figure 5 illustrates the complete layout of designed PA including a driver stage. The transistors include backvias to minimize the reduced channel temperature.

2.4 Simulation Results

In **Figure 6. (a)** a maximum PAE of 34% at the output power of 29dBm and 29% at 6dB OBO are achieved. **Figure 6. (b)** shows the DPA can deliver 14dB power gain at 26GHz. Under large-signal conditions, the gain is gradually reduced with increasing the output power. The $P_{out,1dB}$ is 29dBm. The driver stage incorporates the device size of 4×100 µm gate to achieve gain flatness. **Figure 6. (c)** shows that the DPA exhibits a gain flatness of above 15dB over the frequency range of 25.5-27.5GHz, While the Main PA provides 7dB power gain. The DPA maintains a power gain variation when peaking PA active that requires higher voltage for conducting current. **Figure 6. (d)** indicates that at the lower power levels the peaking device consumes no power and once it turns ON, its voltage increases based on C biasing condition at the Doherty region, and at the peak power, both main and peaking PAs provide the same voltage. The outcomes of the proposed DPA is related with recently reported ones in Table 1. The results confirm that the presented MMIC DPA offers an reasonable operation based on gain, back-off efficiency and output power for 5G mobile handset application.

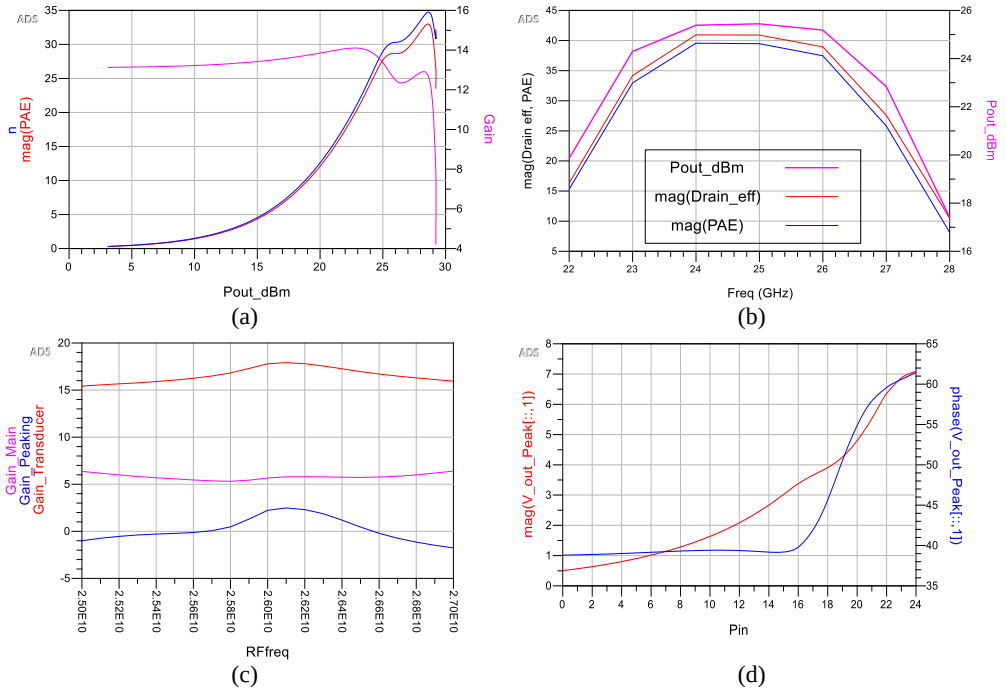


Fig. 6. (a) Modelled PAE, drain efficiency and power gain (b) frequency responses of the PAE, Darain efficiency and output power, (c) transducer power gain, gain of Main PA (pink line) and peaking PA (blue line) over the band frequency. (d) Voltage behavior of the main (blue) and peaking (red) PAs.

Table 1. The mm-waves Doherty power amplifiers

Ref.	Technology	Freq. (GHz)	Gain (dB)	Pout (dBm)	PAE% at BO	Area (mm^2)
[9]	SiGe BiCMOS	28	18.2	16.8	19.5	1.76
[10]	0.15-µm GaAs	28	12	26	29	2.85
[11]	COMS	34	19.8	20.7	13.1	0.45
[12]	0.15-µm GaAs	23	12.5	30	28	4.29

This work	0.1-μm GaAs	25-27	15	29	29	4

3 Conclusion

In summary, the design methodology of a developed mm-wave MMIC Doherty PA is described. The DPA is designed based on a 0.1-μm gate GaAs pHEMT on a 50- μm substrate thickness occupying an area size of $4\ mm^2$. Wideband impedance matching based on L-type topology is employed exploiting the foundry design kit. The output power of DPA at the 1-dB compression point corresponds to the 800 mW/mm power density based on the output power of the two devices.

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