Design of SOC Based SRAM Cluster for Reliability and Functional Safety Applications

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Abstract. In this paper the design of SOC based SRAM cluster is implemented for reliability and functional safety. The main objective of this research is to improve the accuracy and reduce the delay using SOC based design. The designed system initially generates the network using network generator. This network generator basically uses the strategies of both user's clusterization and hierarchy optimization. After the strategy of hierarchy structure the electronic design automation (EDA) generator will generate the test standards based on the access of tests. This generated components test will be extracted based on the standards. Next H-Array generator will generate the arrays of H-arrays for different cluster level sub networks. All these arrays will be cross compiled by mapping the cells. At last this will be saved in SRAM cluster. Hence the SOC based SRAM cluster will improve the accuracy and reduce the delay in effective way.

Keywords: System on chip (SOC), Electronic Design Automation (EDA), SRAM (Static Random Access Memory), H-Array generator, Network Generator.

1 Introduction

In the semiconductor technology, Electronic Design Automation (EDA) plays important role for the growth of tools that are used. In the pre defined design phase of chip, all chips are pre-verified. For the system reliability and functional safety, EDA tools are used in system on chips. Hence to reduce the delay and increase the accuracy of this design SRAM cluster is introduced. Basically in the domains of safety and critical mission, SOC is most widely used. By using SRAM cluster, the functional safety is provided to the design [1]. Earlier Built in self test technique is used to provide the safety for system on chip, but it doesn't give effective results. Hence SOC based SRAM cluster is introduced.

Generally, the system on chip requires only power to operate. In the field of effect, at certain point the delay is continuous. Chip area and delay are increased when it widely applied to the circuits. Hence, Two methods are commonly used to consume the power [2]. Based on the applied voltage circuits, speed limit of given chip is determined. By mixing the number of inverting and non inverting stages, chip of the system is provide with odd number of bits.

System on chip in complementary metal oxide semi conductor (CMOS) is composed of source- coupled differential resistively-loaded delay cells which are investigated. CMOS

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voltage-controlled System on chip with good phase-noise performance is presented. Chip and transmission line systems are specifically coupled to obtain the chip stabilization due to interaction of cell as at same time between the chip operation and a wave traveling in the transmission line systems [3].

In the System on chip (SoC) based on complementary metal oxide of semi conductor (CMOS), the on-chip inductors of the output chip is controlled. The system on chip(SoC) can be changed further by changing either voltage supply or number of stages. There is a low power in the cell phones and the computer of mobile chip is which is another important scaling factor.

Using the System on chip (SoC), the design is constructed on the Chip designs and they occupy the chip of less area and improving both the performance and cost. If delay cells of even numbers are used, it will generate both in the quadrature phase outputs and phase outputs. Because of their low quality factor the phase-noise performance of system on chip is poor. In the System on chip (SoC) basic element is a cell of a Dependability Manager. The complementary pairs of positive channel of metal oxide and negative channel of metal oxide obtained from the cell. The complex circuit behavior is estimated and determined by the results of obtained Dependability Manager (DM) [4].

Using the technology of complementary metal oxide of semi conductor (CMOS). all the digital and the designs of analog can be fabricated. In the gain stages a system on chip (SoC) is connected to a loop from the last of that output stage and it is given to the input of first stage. The system on chip (SoC) has been designed for different stages. Because of the various advantages, CMOS technology is widely used in commercial applications. Reliability is another important parameter which is also needed for designing of low power circuit [5].

In this most of the digital and electronic systems shows oscillatory behavior. Oscillators have now become the most important for all digital components, and the optical devices of a communication system. The electronic devices size is reduced greatly after the integrated circuits introduction of the technology. While designing any integrated technology and integrated chip, designers have to take care of some parameters. They are power consumption, speed, silicon area, delay and the System on chip is a closed loop.

The system on chip consists of different stages which has designed by using the technology of complementary metal oxide of semi conductor (CMOS) based on tanner tools. There are 5-stages of System on chip (SoC) and it is cascaded in to the output of the stage as one and it is fed into the next stage of input and finally it is feedback in to the output and the input of first stage. The voltage supply is also sufficient and it should be given and reset in to the voltage of input and it is applied at once to the circuit, so it spontaneously arise the oscillations. Where the positive channel of metal oxide of semi conductor which is also called as the network of pull-up and the negative channel of metal oxide of semi conductor also called as the network of pull-down. Hence, in this paper, the design of SOC based SRAM cluster is implemented for reliability and functional safety is implemented.

2 Background

The design of Modern complementary metal oxide of semi conductor is based on the consumption of reducing power and the circuit design which is stable. With respect to the time, it shows that the chip varying the voltage while performing simulation. The SRAM Power area is occupied by the consumption of current which is observed from the nearest chip which is wireless by maintaining 2.4 GHz frequency.

The output of amplifier rises slightly, when noise is reduced in the circuit. In this variation, voltage is presented from the output which will pass through the elements of delay. In this the amplifier, the negative gain will be always greater than 1. Input and output will be directly opposite to each other. The input value changes when the value is greater than 1.

The signal which is amplified and inverted will pass through the output block. Again this obtained value will be amplified and inverted for effectiveness. The given input value is sequential to the square wave and obtained output value is square wave. This output square wave consists of equal time period with less delay. Hence, the growth depends on the amplifier output voltage.

In the iJTAG network component, Segment Insertion Bit (SIB) plays important role. This will allow the network to organize the hierarchy. If the SIB is opened then 1 is updated and gives an active scan path. When the path is excluded then the SIB will update 0 and it will be closed.

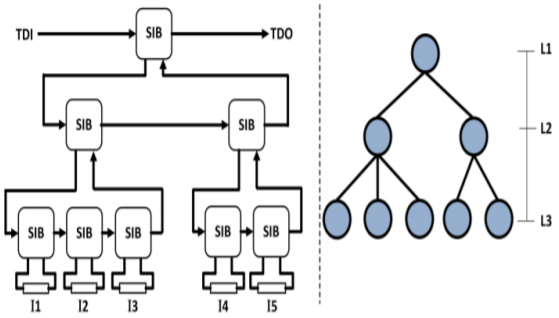

Fig. 1: An Example of a Hierarchical internal iJTAG Network

The above figure (1) shows the example hierarchical SIBs network. Segment Insertion Bit (SIB) consists of one parent and more than one child's. The parent will be at higher level and children will be at lower level. When the both upper and lower level is opened then SIB is selected. These are propagated from the parent SIB to children SIB. Based on the controller the roots of SIB are selected.

The wave grows from the noise of exact analysis and it will show that the initial and the square may not grow, square is formed when the limit of output is reaches the amplifier. Oscillator system is named as the version of the oscillator delay. The system oscillator uses the number of DM and the single amplifier effect of a DM greater than one. Hence the name

system on chip is having a delay rather than the single element, and it contributes the inverter of each and around the signal of the system which inverts the delay cells.

Adding the pair of the system oscillator is to increase the inverters of total delay cells and the chip decreases the delay. The changes in supply voltage of each delay inverter and the decrease in higher typical voltage and increase in the chip of the delay oscillator. Some methods have been described by the Bratislava of the chip stability which improves the consumption of power and the oscillator of system complementary metal oxide of semi conductor. The comprised system on chip has the number of delay stages, with the last stage and the output is fed back into the first input.

The sensitivity supply is the measure and the variation effect of the voltage supply on the response of circuits. According to the change the percentage which is defined by the chip, voltage supply varies. The sensitivity supply decreases the chip with increase in delay. At the frequencies of higher operating, the sensitivity falls below negative to a zero value. The design of Modern complementary metal oxide of semi conductor is based on the consumption of reducing delay and the stable circuit design.

3 SOC Based SRAM Cluster Architecture

The below figure (2) shows the architecture of SOC based SRAM cluster. The designed system initially generates the network using network generator. This network generator basically uses the strategies of both user's clusterization and hierarchy optimization. After the strategy of hierarchy structure the Electronic Design Automation (EDA) generator will generate the test standards based on the access of tests. This generated components test will be extracted based on the standards. Next H-Array generator will generate the arrays of H-arrays for different cluster level sub networks. All this arrays will be cross compiled by mapping the cells. At last this will be saved in SRAM cluster.

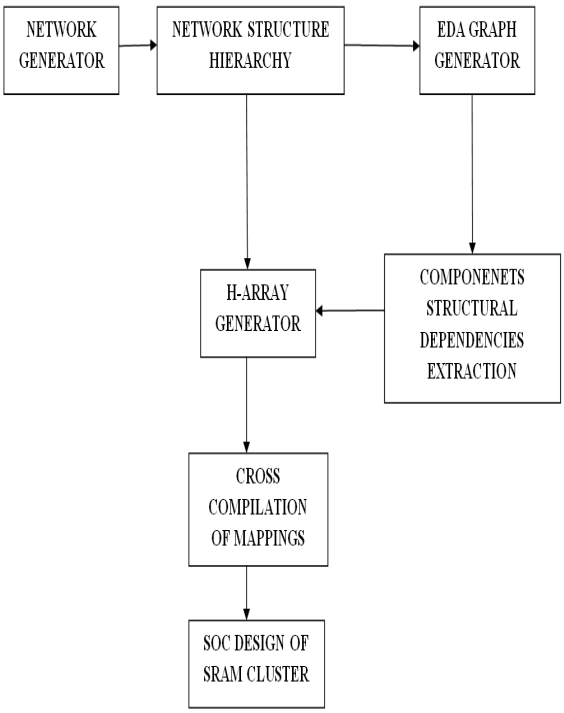

Fig. 2: SOC Based SRAM Cluster Architecture

By using both the user's clusterization and the hierarchy optimization strategy, network hierarchy is generated from network generator. EI clusters are controlled by the user and this is depending on the modules. This module will define the reliability and functionally of Cluster-DM by managing independently. In a modules, the group of EL clusters are represented as non-controlled EI cluster. Scanned signals perform the routing, when the clusters will be grouped together.

H-Arrays are generated by using H-Array generator. This H-Array generator is based on the cluster-level sub-networks which are correspondent to the Cluster-DMs. In system-DM, H-Array network is maintained. Cross compilation of mappings is done after arrays are generated from the H-arrays. Now this will be saved in the cluster of system on chip.

On-chip stores involve a larger division of the present superior microprocessors and handheld compact devices. Because of the expansion in off-state streams in every innovation era, reserves keep on accounting for a large measure of dissipation power in a microprocessor. Besides, as innovation scaling proceeds with, the cell turns out to be less steady because of lower supply voltage and expanded spillage. The soundness of SRAM cells is communicated by its static commotion edge. Consequently, the third piece of research is centered on the design of SRAM cells with low delay and high commotion edge without much corruption in performance.

4 Results

The below figure (3) shows the number of MOSFET's and independent nodes of SOC based SRAM cluster.

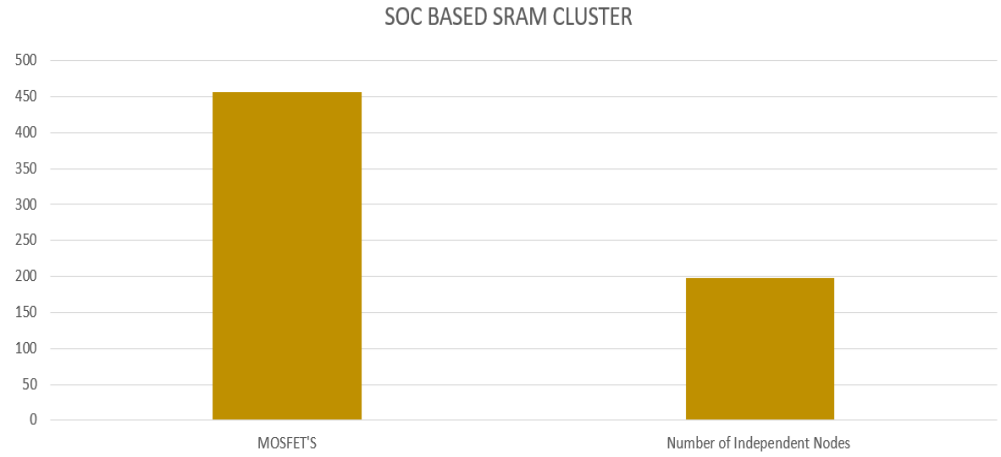

Fig. 3: Number Of MOSFET'S And Independent Nodes Of SoC Based SRAM Cluster

The below figure (4) shows the number of boundary nodes and total nodes of SOC based SRAM cluster.

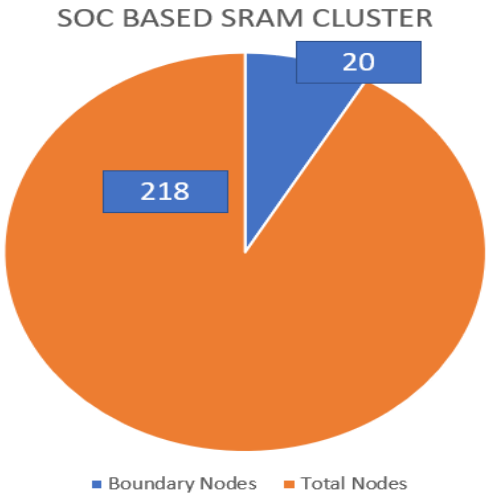

Fig. 4: Boundary Nodes And Total Nodes Of SoC Based SRAM Cluster

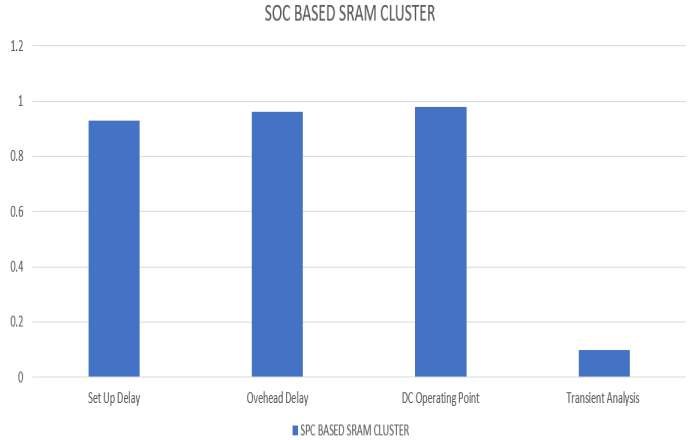

Fig. 5: Set Up Delay, Overhead Delay, Dc Operating Point And Transient Analysis Of SoC Based SRAM Cluster

5 Conclusion

Hence in this paper the design of SOC based SRAM cluster is implemented for reliability and functional safety. The designed system initially generates the network using network generator. After the strategy of hierarchy structure the electronic design automation (EDA) generator will generate the test standards based on the access of tests. Next H-Array generator will generate the arrays of H-arrays for different cluster level sub networks. All this arrays will be cross compiled by mapping the cells. At last this will be saved in SRAM cluster. Hence the SOC based SRAM cluster will improve the accuracy and reduce the delay in effective way.

References

[1] Ahmed M. Y. Ibrahim and Hans G. Kerkhoff, “An EDA Framework for Reliability and Functional Safety Management of System-on-Chips”, 978-1-7281-4823-6/19/$31.00 c 2019 European Union.

[2] Ahmed M. Y. Ibrahim and Hans G. Kerkhoff, “An On-chip IEEE 1687 Network Controller for Reliability and Functional Safety Management of System-on-Chips”, 978-1-7281-4718-5/19/$31.00 ©2019 European Union DOI 10.1109/ITC-Asia.2019.00032.

[3] PremachandranCS, Seungman Choi, Salvatore Cimino, ThuyTran-Quin, Lloyd Burrell,Patrick Justison , “Reliability Challenges for 2.5D/3D Integration: an Overview”, 978-1-5386-5479-8/18/$31.00 ©2018 IEEE.

[4] Konstantin Shibin, Sergei Devadze , Artur Jutman, “On-line Fault Classification and Handling in IEEE1687 based Fault Management System for Complex SoCs “,978-1-5090-1331-9/16/$31.00 ©2016 IEEE.

[5] Poorani.P, Ms.Vijayashree.B M.E, “Implementation of AHB Bus Protocol For System On Chip Security”, 978-1- 4788-7225 -8/15/$31.00©2015 IEEE.

[6] Buyoung Yun, Kang G. Shin, Shige Wang, “Thermal-Aware Scheduling of Critical Applications Using Job Migration and Power-Gating on Multi-Core Chips”, 978-0-7695-4600-1/11 $26.00 © 2011 IEEE.

[7] L. Larcher, P. Pavan, " Flash Memories for SoC: an Overview on System Constraints and Technology Issues", Proceedings of the 9th International Database Engineering & Application Symposium (IDEAS'05) 1098-8068/05 $20.00 © 2005 IEEE.
[8] Haim Marom, "DF-RQA Practice for SoC", 0-7803.851 7-91041520.00 '2004 IEEE.
[9] J. L.Silva, R.M. Costa, G. H. R. Jorge, "RtrASSoc - An Adaptable Superscalar Reconfigurable System-On-Chip The Simulator", Proceedings of The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications ISBN 0-7695-1929-6/03 $17.00 © 2003 IEEE.
[10] Neil Bergmann, Peter Waldeck, John Williams , "A Catalog of Hardware Acceleration Techniques for Real-Time Reconfigurable System on Chip", Proceedings of The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications ISBN 0-7695-1929-6/03 $17.00 © 2003 IEEE.