FPGA Based Dual Controller Design for EMI Reduction in Dc-Dc Converters

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Abstract. In high frequency electronic power converters, the suppression of Electromagnetic Interference (EMI) and the improvement of Electromagnetic Compatibility (EMC) have become important. Field Programmable Logic Array (FPGA) has become a low-cost platform offering the ability for power electronics to create unique EMC control techniques. In FPGA, however, it is complicated to accomplish some of the features required in the power electronic control system. The key difficulties are related to the operation of the fixed point, and the need to change the dynamic number range. Constructing filters to comply with the EMI limits is a significant part of the production cost of power converters. Therefore, a simple yet powerful dual controller based FPGA is therefore discussed to provide a substantial motor control for noise reduction. A model of a prototype has been tested and hardware findings indicate a substantial drives with low performance requirements. In terms of speed and torque, the theoretical algorithms, hardware information and experimental findings are presented and discussed.

Keywords: Field Programmable Logic Array, DC-DC Converters, Electromagnetic Compatibility, Electromagnetic Interference..

1 Introduction

The rapid growth of the electronics sector, the challenge of circuit design is rising and the preparation time for designing devices is shrinking due to competition. The DC-DC converters are critical for the supply of DC power from a DC power supply such as batteries, photovoltaic cells and fuelling in portable electronic devices such as tablets, laptops or electric vehicles, such as mobile phones. Such electronic devices also include many sub-circuits, each of which requires a specific level of voltage varying from the one given by the source Trong *et al*. [2017]. Designers usually create DC/DC switch mode converters using analogue components to monitor the feedback loop and provide Pulse-Wide Modulation (PWM) necessary for switching. For use of analogue components like these, a range of considerations have to be taken into account in ensuring design reliability, such as tolerances, electrical stress, ageing drift and temperature drift.

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A common misconception is that if all the control systems pass varying emitted, implemented and traditional noise requirements in the agency, the system also passes required noise standards Jalnekar *et al*. [2015]; Elrefay *et al*. [2017]. The noise conducted by the drivers connecting the transducers to the input source, the load or any control signals is detected. A system does not have the requisite noise standards. The emitted noise is the radiation noise emitted by the voltage, current or magnetic flux switches by the convertor au *et al*. [2016]. Because of parasitical elements such as input/output power, leakage inductance, and insulation resistance, common-mode noise is common to the converter input and output. The adverse effects of parasites on the power changer have led power designs to deploy resonance transversals and other designs which are part of the circuit with ever growing frequency variation and power densities. Switching on the input switching transistor at zero voltage or zero current decreases input noise and increases performance.

Null-voltage or null-current converters regulate the frequency of switching to retain power. However, large filters are needed for noise reduction in DC-DC convertors Park *et al*. [2015]. The significant amount of electromagnetic interference produced by repeated switching operations is generated by power electronics converters. EMI spectrums are especially concentrated on several critical switching frequencies. The significant amount of switching losses is caused by the electromagnetic interference power converter. The output of EMI sensitive products is influenced by switching losses in converter topologies. EMI noise reductions are achieved in the early days by traditional methods that cause additional cost effects on power converters. The new randomized sigma delta modulation, which is effectively accomplished by randomization of switching cycle parameters, reduces current electromagnetic interference.

Variations in switching frequency, duty ratio and pulse location result in an important effect on the density of the power spectrum. But on the other hand, negative feedback is used in traditional sigma delta modulators to monitor a system's nonlinear response and to realize the attenuation of the signal band quantization noise due to noise shaping Wu *et al*. [2015]; Benhadda *et al*. [2018]. Now, the FPGA will replace the conventional analog solution with an inexpensive low-performing FPGAs combined with analogue to digital converters. FPGA is a semiconductor system not limited to pre-characterized equipment works; it is used exceptionally well and could be arranged in accordance with its structural specifications by the implanted framing engineer. For the installation of custom equipment FPGAs use pre-constructed logic blocks and programmable channels depending on how built framework developers arrange those components. FPGA is an appealing design choice for hardware Sulaiman *et al*. [2009]; Monmasson *et al*. [2011]; Aridhi *et al*. [2012].

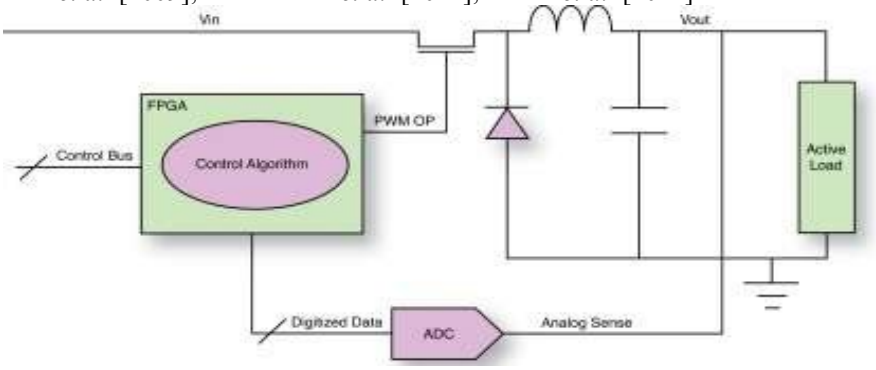


Fig 1. DC - DC regulator using FPGA

For a fine review of traditional and recent FPGA technical advances that concentrate on the application of industrial control systems. Although FPGA is now commonly deployed in a variety of military, defense and signal processing applications, it is versatile rather than analogue control, becoming less cost-effective and applicable for applications in power supply. Using FPGA-based digital controllers, implementation of the noise reduction systems can be achieved. Figure 1 depicts the FPGA-based framework comprising PWM generation and error calculation as well as a control algorithm for the adaptation of the PWM. The FPGA offers several distinct advantages at the same time, most of which are conveniently accessible inside the FPGA itself, except for a bit of HDL coding. This technique requires an analog-to-digital transition scheme to transfer the current output voltage back into FPGA, either using the ADC-based or some other solution, to promote the ability of the control algorithm to adapt to the output of the PWM Sinha roy *et al*. [2019]. One of the most special capabilities of the FPGA is reconfiguration to fully exploit FPGA. This allows for the recovery of a part of the FPGA while the remainder of the FPGA still functions normally. This technology has been widely used in computer vision and communications, but researchers in power conversion have recently become interested in it Kourfali *et al*. [2019]. Therefore, in this analysis, an FPGA with a reconfiguration is used to implement two controllers - vector power, and frequency - voltage control (f/Hz). This configuration shows that a stable and potentially noise-reduction transition between controls can be achieved Gandhare *et al*. [2019]; Shimoda *et al*. [2019]. The main contribution of the present work is,

1. To design a dual controller based FPGA to provide a substantial motor control for noise reduction.
2. To demonstrate the hardware findings that indicates substantial drives with low performance requirements.

Section II exploits the dual control schemes. Section III depicts the proposed system design of hardware VHDL implementation. Section IV demonstrates the simulation and testing results followed by conclusion in Section V.

2 Dual Control Schemes

The normal method for control of triphase motors is still vector energy control while torque control is being used more and more in the industry; however, this method has numerous failure points as it uses sensors to obtain feedback. In high performance controls, sensor less open-loop controls are usually not preferred, but if the operation of engines is vital to safety, it is desirable to use as a safeguard to maintain control over loss of control. Due to its prominence in the frequency industry, vector power control was therefore chosen as a backdoor device. The vector control system tries to control the engine torque. This is normally done by regulating the engine currents, which align the flow of the stator to regulate the torque. Figure 2 demonstrates the configuration used in this work. The method can be divided into the conversion to control variables and the control of these parameters.

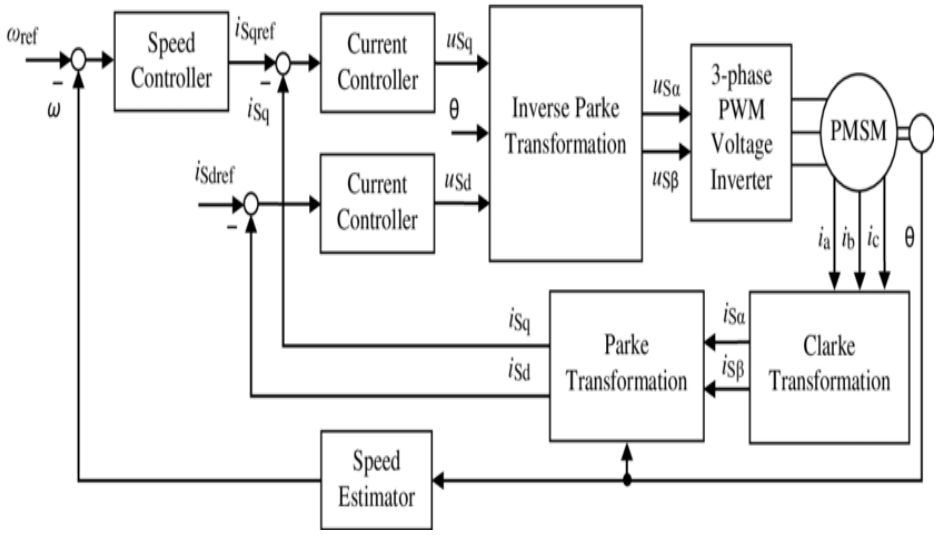


Fig 2. Block diagram of Vector power control

The aim of the first step is to convert the instantaneous current (i) in two phases, time-independent, and a stationary reference context (u) from the rotating frame of the engine. Due to their frequent changes, the input triplet is very hard to monitor but the changes allow a more regulated pair of values,

$$\begin{bmatrix} iS\alpha \\ iS\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} iq \\ id \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} uSq \\ uSd \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} iS\alpha \\ iS\beta \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} uS\alpha \\ uS\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} uq \\ ud \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} uS\alpha \\ uS\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} uS\alpha \\ uS\beta \end{bmatrix} \quad (4)$$

The transformation starts in the order shown in equations (1) and (2) of the Clarke and Park transformations. To make the system simpler, the system was presumed to be balanced, thereby reducing the number of sensors required for final implementation by removing the need to complete one of the three transition phases. θ is the park transformation, where the rotor is rotated. The results (i_{sq}) are then moved to the Proportional Integral (PI) controller. i_s the motor flow control effective and i_q controls the engine torque effectively. In order to obtain the desired torque the PI control tries to hold the id value closer to 0 and the iq value near a defined value. The PI controller manufactures a couple of voltage values (uS_{qd}), but always in the revolving reference frame, depending on time. The reverse park and Clarke transformations, in this order shown in Equation 3 and Equation 4 respectively, are passed by to achieve a three-phase, time-dependent, stationary control voltage (u_{abc}) frame collection. The results are moved to the PWM generator.

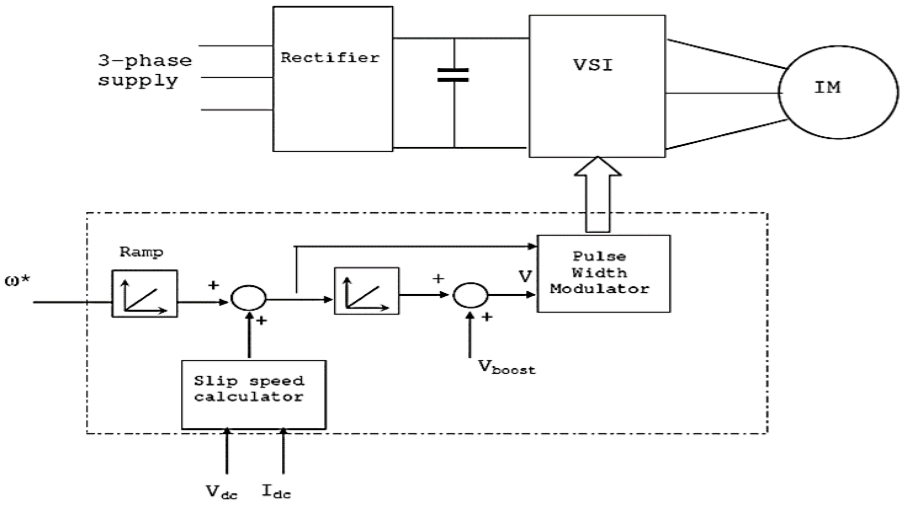


Fig 3. Block diagram of Frequency - voltage control

The frequency-voltage regulates the engine speed while the applied torque is being maintained continuously. This approach primarily preserves the voltage and frequency movement of the motor, as can be seen from the block diagram shown in Figure 3. The explanation for this is that the motor functions continuously in the linear magnetic region if the motor operates. The phasor equation σ_c for the magnetizing current is,

$$\sigma_c = \frac{2\pi f}{v} \quad (5)$$

This implies that if the $f = v$ ratio remains constant; the stator flow will remain constant. Thus, when that ratio is constant, the speed of the motor will adjust while maintaining constant flux. This results in just slip speed determination of the torque. Without a justification, a slip speed controller was not introduced because this added complexity.

3 System Design

3.1 PWM Generator

This work has been carried out using the PWM generator to work with the two-way control algorithms $\frac{f}{v}$ as well as with the vector power.

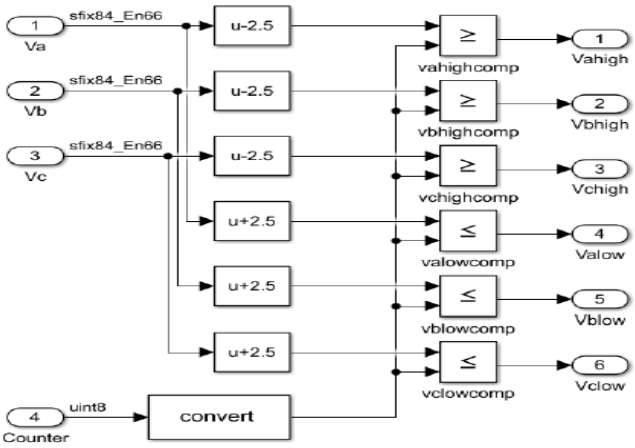


Fig 4. Block diagram of PWM generator

Figure 4 shows the basic diagram of the block. This is a basic PWM generator, in which the incoming signal is simply compared to the triangular shape of the PWM. The Triangle Waveform was developed as a controller which ranged from 0 to 50 and then from 50 to 0 as the device had been binary configured. Thus, the entering waveforms were centered at 25 before the triangle shape was compared. Prior to the actual comparators, they moved the incoming waveform to the lower and downwards to add dead times in the PWM to stop shootings in the inverter. The waveforms were contrasted. The inclusion of the larger and smaller comparators ensured a minimum performance delay between comparator pairs. To compare incoming signals with the generator, a triangle wave is required. This wave generator was configured as a counter up/down with a specimen-fitting upper limit. For that job, it was reset to 50, started counting to 0, and repeated. This counter counts the defined limit. The carrier wave was then used to produce the PWM.

3.2 Dual Control Reconfiguration

In the top-level design, the controller was left as a black box with only inputs and outputs listed. The controllers were deployed and the netlists were produced separately from the high standard design to ensure both controllers had the same inputs and outputs, even if they needed foreign ones. Upon completion of the design, the Xilinx PlanAhead Analysis and Design Tool was used to assign the FPGA resources and set clock requirements for generating final bit files Svyd *et al*. [2019]. In the tool it can be described as a reconfigurable partition for the black box configuration of a top-level module design. The programme can then be allocated to the Black-Box several netlists, for example the vector controller and the *f*/v controller. This empty implementation has been used to speed up initial configuration and provide the reprocessing configuration controller with a known starting point Usmani *et al*. [2019]. The programme uses these configurations to ensure that the user has the minimum hardware specifications for the repository. This partition is defined by the user and shows whether the requirement for the resource was complied with.

Table 1. Address verification of dual controls

Control	Logic Elements	Pins	Memory Bits	9 Bit Multipliers
Vector Power	2836	368	0	34
f/v	1499	50	516 128	41

The programme uses these configurations to ensure that the user has the minimum hardware specifications for the repository. This partition is defined by the user and shows whether the requirement for the resource was complied with. The consumer synthesises the initial configuration, the empty partition in this case. The other confidence configurations are then synthesized and combined with the initial configuration, enabling the new confidence configuration to use the same static confidence. The results of each synthesis are then compared to each other to indicate that the static portions are the same. Upon completion, the bit streams are created for each configuration. This provides a complete configuration image for null, vector, and f/v, and even minimal bit files for reconfiguration. After this, the device is ready for testing and putting on FPGA Aubakirov *et al*. [2019].

3.3 Reconfiguration Control

A black box portion where the shifting system is situated must be introduced with the top level system. This prohibits standard tools from synthesizing and restricting preliminary debugging to syntax checks and generating a netlist. In particular, around this black box a filter needs to be introduced to stop signals entering or leaving the reconfiguration segment during configuration. In the controller's top-level architecture, a set of disabled registers were implemented around the engine algorithm black box, output all of the zeros, while the reconfigure was being used.

3.4 VHDL Hardware Control

AD7822's standalone Operation portion of the AD7822 data sheet has been developed with the FPGAs interface to the current sensors. In this mode, the system begins a conversion with a single signal and has only one signal when the conversion is complete.

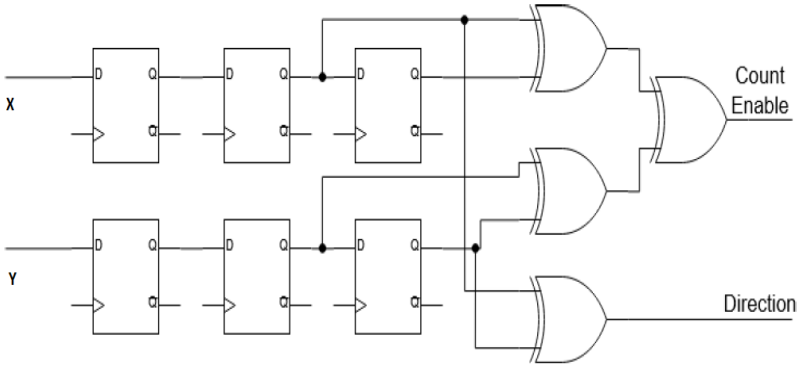


Fig 5. Decoder design

The way the conversion signal was mounted in VHDL was to turn on/off from the internal clock and save the data into a register when the transmission signal is activated at the end. The encoder outputs consist of two quadrature signals. Both these two signals indicate the location of a magnet in the encoder. These are near each other, but physically slightly offset. This allows the direction of the signal to be determined first. This information can be connected to an up/down counter to determine the position of the encoder. The circuit shown

in Figure 5 is one way to extract direction and allow signals by using hardware. In each transformation of the inputs it is called a 4x decoder, which calculates 4 times per transition. The FPGA includes all the logic of control and reconfiguration. The optoisolators and the engine driver lie between the FPGA and the engine. Opto-insulators are supplied to isolate the responsive FPGA from the high-voltage motor driver electrically. The control system transforms the FPGA signals to low-power signals that drive the engine. The sensors provide information on phase current and motor location for the control algorithms. The memory modules include the partial bit, which defines the FPGA control algorithm. Interface boards are also available to make logical level adjustments for communicating FPGA / memory modules. Partial bit files are accessed as part of the reconfiguration process. The partial bit files used by the standard EEPROM interface have been stored on the flash memory.

Table 2. FPGA Time Performance

Modules	**Latency**	**Computation time**
A/D Interface	256	0.4μs
Park transformation	14	0.35μs
Inverse Park transformation	14	0.35μs
PWM	4	0.1μs
Execution time	292	7.3μs

4 Simulation and Results

The physical test design was developed in a way that regulated the torque by the motor at a constant speed. In the simulation, the motor block was connected to a constant speed input in the experiment. The DC motor is fed inputs to drive it at constant speeder speed in physical simulation Banik *et al*. [2019].

Table 3. DC-DC converter simulation setup

Parameter	**Value**	**Parameter**	**Value**
V_{IN}	12V	Inductance (L)	1μHz
Efficiency	0.9	Capacitance (C)	8840 μF
Frequency	530 KHz	Maximum Output Current I_{max}	60(A)
V_{OUT}	1.30 V	R_L	2.3mΩ

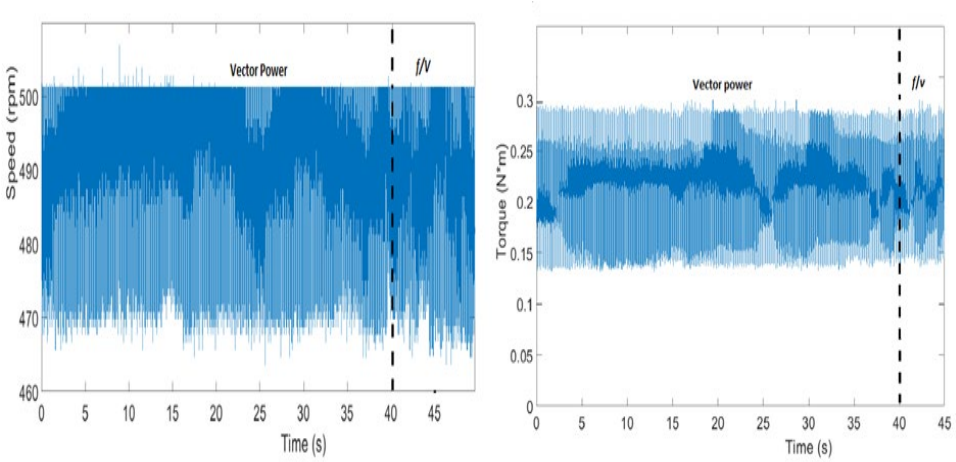
A DSPACE DS1104 controller was used to drive the DC engine and to track the system's real-time speed and torque characteristics. The dSPACE interface was designed via MATLAB Simulink to deploy a simple DC speed controller along with a device to read the DC motor current, voltage and speed to show and measure torque using equation 5.

$$\rho = \frac{60p}{2\pi r} \quad (5)$$

Where ρ is torque, p is power and r is rotational speed.

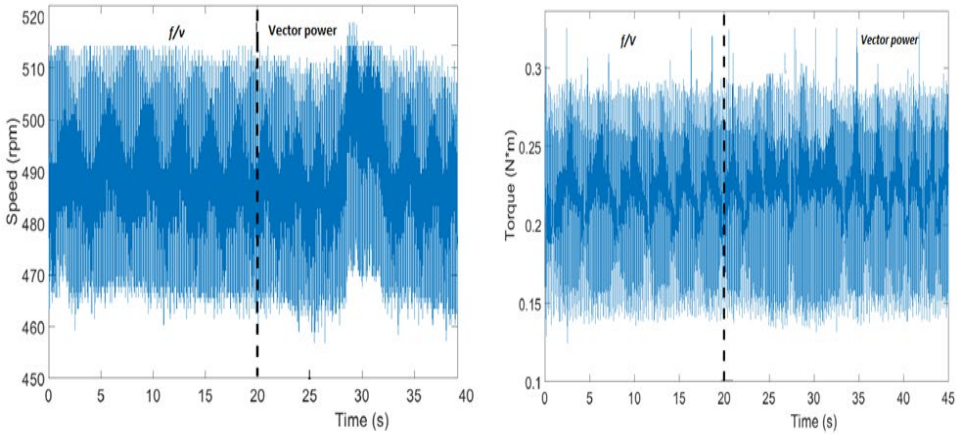
Table 4. FPGA Hardware quality results

Stage	**Cycle Latency**	**Clock frequency**	**Deterministic Latency**
Initial	800	150MHz	5.33μs
Optimized	450	210MHz	2.14μs



(a) **(b)**

Fig 6. (a) Speed transition between vector power and *f*/*v* at 600 rpm; (b) Speed transition between vector power and *f*/*v* at 600 rpm.



(a) **(b)**

Fig 7. (a) Speed transition between *f*/*v* and vector power at 600 rpm; (b) Torque transition between *f*/*v* and vector power at 600 rpm.

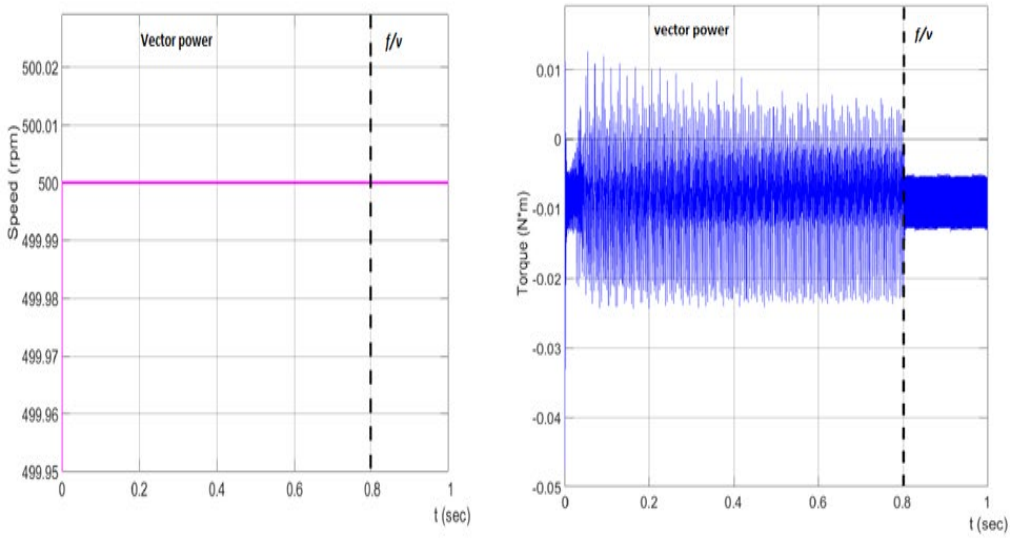


Fig 8. (a) Simulated speed transition between vector power and *f/v* at 600 rpm; (b) Simulated torque transition between vector power and *f/v* at 600 rpm.

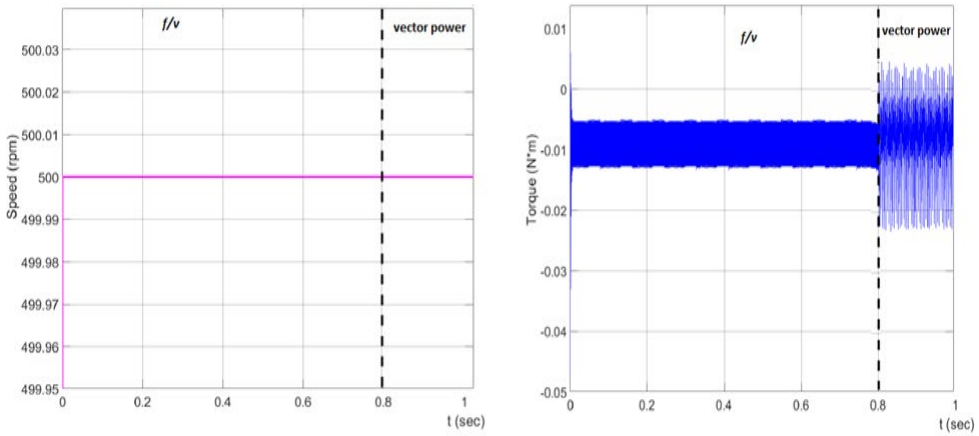


Fig 9. (a) Simulated speed transition between *f/v* and vector power at 600 rpm; (b) Simulated torque transition between *f/v* and vector power at 600 rpm.

Figure 6 shows the speed transitions from vector power to f/v at 600 rpm. Figure 7 depicts the torque transitions from vector power to f/v at 600 rpm. Figure 8 shows the speed transitions from f/v to vector power at 600 rpm. Figure 9 depicts the torque transitions from f/v to vector power at 600 rpm. The primary source of the noise was the constant-speed DC-engine, so it didn't have a constant impact on the driver. The DC motor had speed oscillations around the desired speed, so the calculations were carried out with the constant driver average speed. At higher speeds, the effects of the transformation are clearer. In each of these outcomes, a dramatic shift follows immediately after the transfer, signalling the completion of the reconfiguration process and the takeover of the new controller. The machine was tested at three speeds: 200 rpm, 400rpm, 600 rpm and 800 rpm to accurately reflect the switching

controller. Tests may have been conducted at higher speeds, but a great deal of error was observed given the maximum rated speed of 2000 rpsm and the potential for unknown behavior. In a switch between the controllers, each speed was evaluated to ensure the behavior corresponded with the simulated results.

5 Conclusion

Most of the research on FPGAs engine controls uses it as a new type of microcontroller for the work. Furthermore, much of the work on motor controls in general is to produce large and complex motor controls which work well under various conditions. This study suggested dual controller-based reconfiguration is a special function of FPGAs that enables a part of its material to be recalculated while the FPGA remains working. This work has shown that a double controller could provide the vector power and f/v controllers with a stable transition and it suggest that this could lead to other changes between different controllers. In addition, consideration should be given to the conditions under which controllers switch, for example, the conditions under which controller switching is controlled. Although this work means that smooth transitions between other controllers are possible, this area still requires confidence. Furthermore, this work did not concentrate on the output of each controller, which may also be an area of potential inquiry for the development of dual controllers.

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