A Comprehensive Review on FPGA based PWM techniques for DC-DC converters

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Abstract. Pulse Width Modulation (PWM) modules are immensely significant in the design of real power converters. Mainly, the variable duty cycle pulses generated from the PWM module vary the average dc voltages across the load in the power converter circuits. All the regulator and dc/dc converter ICs include the clock, MOSFET switch and the PWM control module apart from the external components such as resistor, inductor and capacitor, diodes, and the transformers. In this review article, the five different PWM generation methods include using a free-running counter, up/down counter, hardware accumulator, two de-bounced push button switches and swapping bits method. The PWM wave generation modules are implemented on an Altera FPGA device using Quartus II synthesis software tool. The performance metrics such as the logic elements (LEs) utility, the clock speed, and the power dissipation are analyzed in detail. Also, Matlab/Simulink and the DSCH/Microwind tools are used to generate the PWM wave.

Keywords: Accumulator, de-bounced push buttons, FPGA, free-running counter, Microwind, PWM, Simulink.

1 Introduction

PWM techniques have been the topic of demanding exploration in the past few decades. The PWM is the widely used technique for controlling DC power to ambiguous electrical devices in sophisticated electronic power switches. Moreover, AC choppers exploit PWM techniques. For instance, the overall current delivered to the load is controlled by the switch's position and state (duration). If the ON time of the switch is higher than the OFF time, the more power will be delivered to the load. For example, if the PWM wave contains the duty cycle of 80%, then the load would receive higher power. Hence the PWM wave's switching frequency plays a vital role in delivering power to the load in the modern electronic power supplies (Guellal et al. 2015).

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More importantly, in the era of power electronics, the demand for AC motor speed control with a variable frequency supply is that the input voltage or current signals accommodate the least possible distortion. The inverter is the optimal solution through the generation of three sinusoidal signals of aligned phasor proportions (Aravind et al. 2014). But the drawback is that the device cost (expensive) requires more number of switching elements. The PWM technique can generate such sinusoidal motor voltage waveforms effectively. In the ac power measurement, the circuits such as PAM and PWM can be used effectively to incorporate multiplier (Aravind et al. 2016).

Most of the power-electronic circuits do have PWM block as the core one. An amplitude signals are encoded into a rectangular signal using the PWM technique with varying pulse-width. Primarily, there is a need of PWM wave in switched-mode power supplies (SMPS) such as servo-motor drivers, DC-DC converters, and power amplifiers. PWM methods would enhance the power efficiency results in more than 95% in some of the recent power-electronic circuits (Karaca et al. 2018).

The PWM waveform generation is either directly or indirectly exploited in the biomedical instrumentation field. For instance, in the typical biomedical instrumentation, successive-approximation ADC using PWM is the widely used technique to obtain digital control signals. Also, the PWM output using either microcontroller or digital signal processor or Field-Programmable Gate Array (FPGA) can generate the ECG signal. For example, in speciic clinical applications, the arbitrary waveform generator using PWM is often used in ultrasound research applications. The PWM based lock-in bioimpedance measurement is widely used in implantable biomedical devices, such as, in pacemakers. The photonic biomodulator often exploits the PWM frequency meter for its measurement. The PWM modules are often used in the phototherapy system.

2 PWM using Simulink

Figure 1 show the generation of the PWM wave using a Simulink model. Here, the instantaneous voltage of the triangular wave is added with a constant, for instance, with 0.8, as illustrated. Then the result is compared to zero, that is, if the adder output is higher than zero, the PWM output becomes zero else becomes one. Figure 2 shows the PWM output wave.

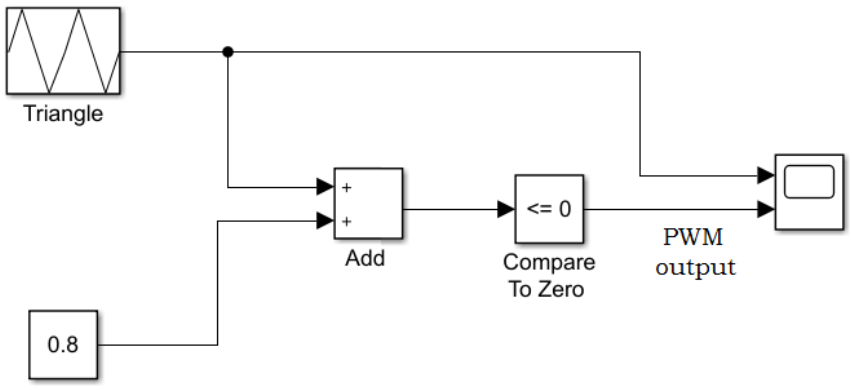

Fig.1 PWM Generation using a Simulink Model

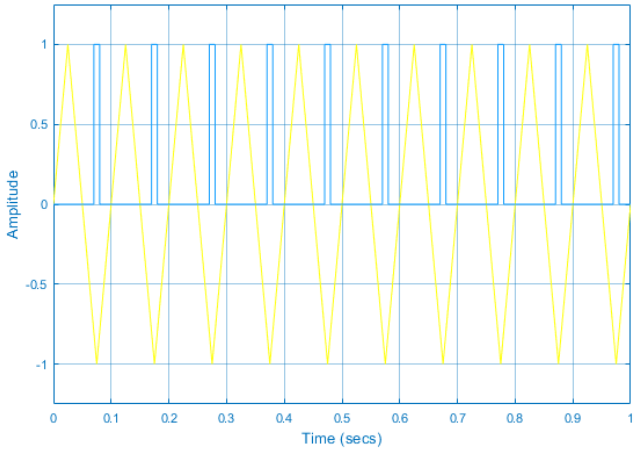

Fig.2 PWM Output Wave

2.1 PWM using Free-Running Counter

Here, as illustrated in Figure 3, the counter output is compared with the PWM_in data. If the counter value is higher than the PWM_in data, then the PWM output becomes one, or the result becomes zero. The RTL schematic of the PWM generation using the free-running oscillator is shown in Figure 3. Figure 4 shows the functional simulation of the same using the Quartus II synthesis software tool.

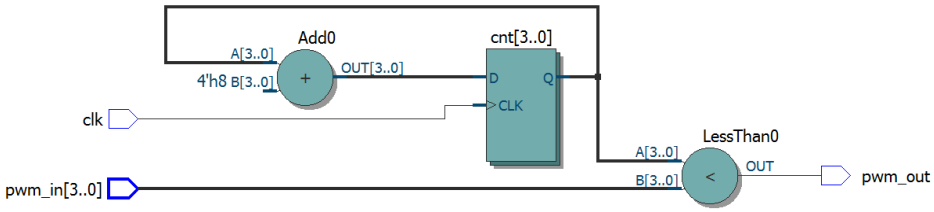

Fig.3 The RTL schematic of the PWM generation using a free-running counter

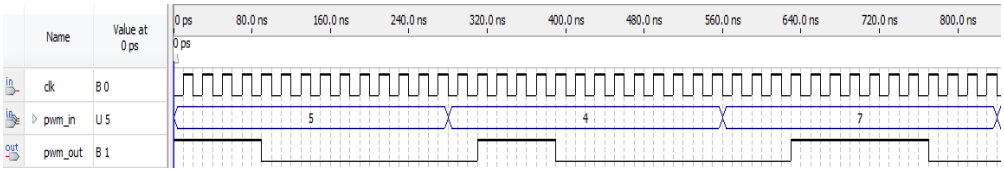

Fig.4 The functional simulation results with the PWM output

2.2 PWM using an Up-Down Counter

Figure 5 illustrates the RTL schematic view of a much-sophisticated design, a loadable up-down counter with the absence of comparator at the output. Since it has got 17 states rather than 16 as in the previous case, the PWM out varies from 6% (1/17) to 94% (16/17).

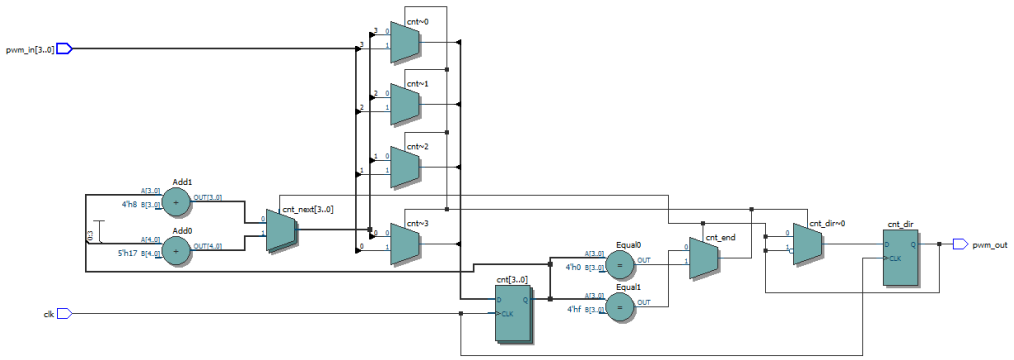

Fig.5 RTL schematic of the PWM generation using an up-down counter

2.3 PWM using Digital-to-Analog Converter

Using an accumulator, the simple first-order sigma-delta DAC can be designed, as shown in Figure 6. If there is an overflow in the hardware accumulator, the PWM_out becomes '1' or else becomes '0'. One such sample functional simulation result is shown in Figure 7.

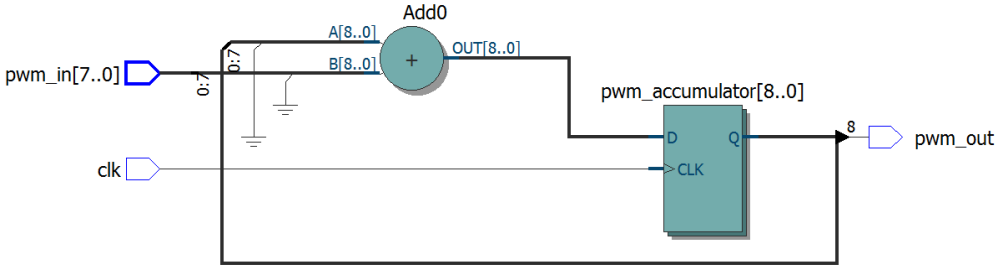

Fig.6 PWM generation using the hardware accumulator

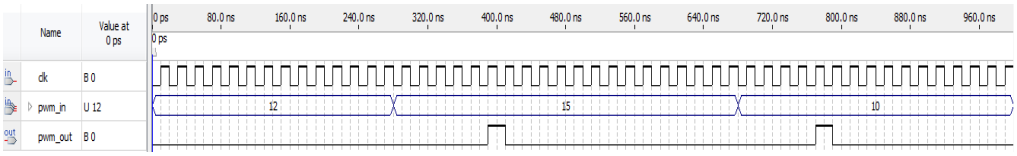

Fig.7 PWM out using functional simulation results

2.4 PWM using two de-bounced push-buttons

PWM output can be generated using two de-bounced push-buttons – one is to increase the duty cycle by 10%, and the other is to decrease the duty cycle by 10%. Thus the variable duty cycle during the PWM generation can be achieved. Figure 8 shows the RTL schematic view (portion) of the PWM generation using two de-bounced push buttons.

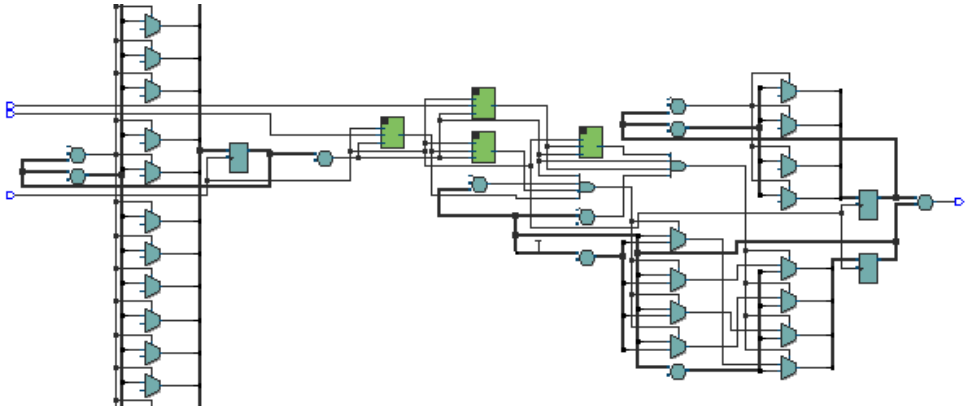

Fig.8 Portion of an RTL schematic view of PWM generation using a variable duty cycle approach

2.5 PWM generation with higher performance

The performance of the PWM generation can be improved by swapping all the bits in the binary comparator. That is, the most significant bit (MSB) is wired to the least significant bit (LSB), the LSB is wired to the MSB, and so on. No additional hardware components such as registers and logic circuits are required due to only rewiring (EDN 2007). Figure 9 shows the RTL schematic view of the PWM generation by exchanging the LSB-to-MSB bits approach.

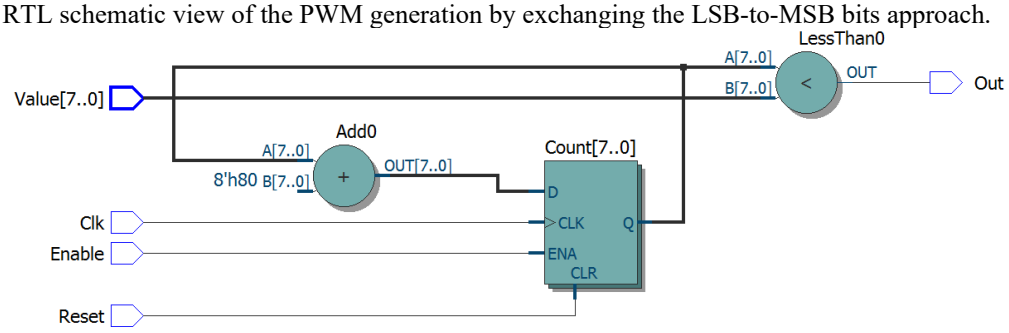

Fig.9 RTL schematic view with the rewiring (LSB-to-MSB) method

3 Simulation Results and Discussion

We experiment with our methods using the Altera Quartus II synthesis software tool. The design implementations were performed on an Altera FPGA device EP4CE115F29C7. A laptop (Dell Vostro 1540) is used in this study, configured as a 2.5 GHz CPU and 4GB RAM. For ASIC implementation, the digital schematic (DSCH) and the layout editor (Microwind) are used. Also, one method demands to use the Matlab R2018a tool, with a Simulink companion software package.

3.1 Resources Utilization

In general, FPGAs include prefabricated logic blocks, input/output blocks, and interconnect resources. We can estimate the number of logic elements (LEs) required for the design using

the device utilization summary obtained from the Quartus II synthesis tool. Figure 10 shows one such report using the methods involved in this study. From the results, the PWM wave generation using two-de-bounced push-buttons requires more number of LEs (56) than others due to the hardware complexity in the design. On the other side, the PWM wave generation using the simple hardware accumulator approach requires only lower LEs (6) than others.

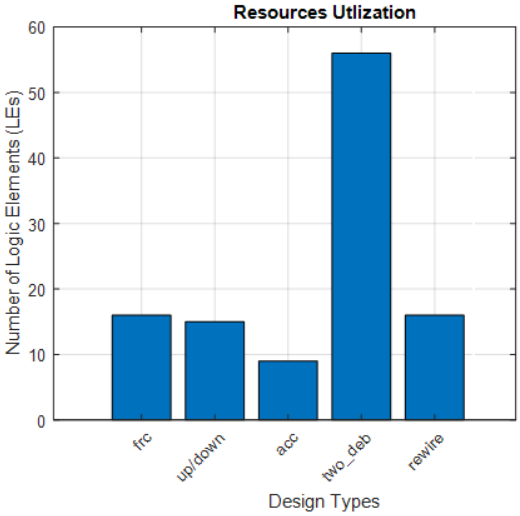

Fig.10 Results on Resources Utilization

3.2 Performance

The critical path is the path that holds a maximum delay in the complete design. Using the Altera Quartus Time Quest Time Analyzer tool, this critical path can be found. The performance or clock speed of the design is calculated by computing the reciprocal of the critical path delay. For instance, the critical path delay of the PWM wave generation using the rewiring method is 2.15 ns, and hence the performance becomes 463 MHz, as illustrated in Figure 11. It is evident from the results that the "accumulator" method obtains better performance (481 MHz) than others.

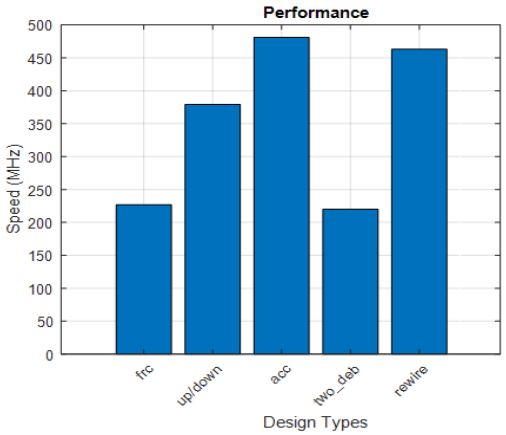

Fig.11 Results on Clock Speed

3.3 Power Dissipation

The power dissipation is one of the significant design parameters with FPGA implementation. It is broadly classified into two categories, namely the static power dissipation and the dynamic power dissipation. The static power is not design-dependent and will be determined by the number of unused logic elements in the design; also, it is called “leakage power”. But the dynamic power dissipation is the design dependent. That is, the used logic elements, the clock frequency, and other resources such as an embedded multiplier, RAM, and PLL in the design will determine the switching activity of the circuit, and hence the dynamic power appears in the circuit.

Figure 12 shows the total power dissipation used by the PWM generation methods used in this study. For instance, the PWM generation using the rewiring method consumes the total power dissipation as 131.04 mW. In contrast, the static power yields 98.46 mW, the I/O power produces 31.09 mW, and the dynamic power yields 1.49 mW.

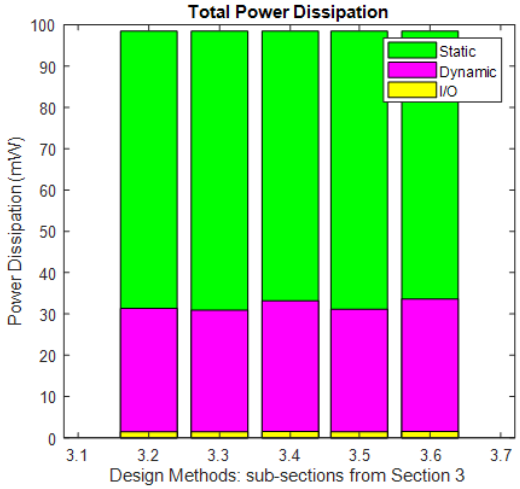

Fig.12 Results on Power Dissipation

4 Conclusion

PWM generation modules are used in many applications such as audio/video amplifiers, telecommunication systems, smart lighting systems, synthetic ECG signal generators, implantable medical devices, etc. This article’s main motive is to analyze the different methods of PWM wave generation and to implement them in an Altera FPGA device. The tools such as Matlab/Simulink, DSCH/Microwind, and Altera Quartus II synthesis software tools are used to generate the PWM wave. The six different PWM methods such as free-running counter, up/down counter, accumulator, two de-bouncing switches, swapping bits, and modified counter are explored, and the results are analyzed in detail.

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