

# LMS Adaptive Filter Design and Implementation of a Low Complexity LMS Filter

Dr P Kalpana<sup>3</sup>  
{kp.ece@psgtech.ac.in<sup>1</sup>}

Student, ME VLSI, ECE, PSG College of Technology, Coimbatore<sup>1</sup>, Assistant Professor(Sel Gr),  
Department of ECE, PSG College of Technology, Coimbatore<sup>2</sup>, Professor, Department of ECE, PSG  
College of Technology, Coimbatore<sup>3</sup>

**Abstract.** In real-time applications, an adaptive filter is used to model the applied input and output signals of the filter iteratively. Errors are minimised through the use of an adaptive algorithm that iteratively changes filter coefficients ( $n$ ). For the LMS method, the coefficients of filters are adjusted by an adaptive algorithm. Error computation and weight-update blocks comprise the LMS adaptive filter's direct form. These blocks of filter determine the filter's efficiency. A low-power, small-area adaptive filter is presented in this paper in two different architectures, namely a zero adaptation delay and a two adaptation delay version. A zero adaptation delay adaptive filter saves nearly 52% of the area compared to a conventional adaptive filter, and the delay is reduced by 26%. Thus, the proposed filter structures can be used in high-speed applications that require minimal space.

**Keywords:** Adaptive Filter, Least Mean Square Algorithms, LMS Adaptive Filter, Adaptation Delay, Area, Delay.

## 1 Introduction

Adaptive filters mainly used in signal prediction, signal enhancement, channel equalization, system identification and noise cancellation. However real time operations are required in filtering applications. In Adaptive filter, the transfer function could be adjusted automatically and high accuracy can be obtained by changing its characteristics [1]. An adaptive filter has two main blocks namely, filter to process input signal and adaptive algorithm that updates the filter coefficients. The adaptive filter diagram is presented in Fig. 1 where  $d(n)$  represents the desired response,  $y(n)$  represents the output response of the filter. The error  $e(n)$  represents the difference between  $d(n)$  and  $y(n)$ . The filter weight coefficients are updated iteratively till the desired response and output response of filter are same [2].

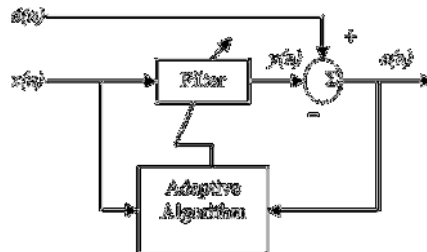


Fig 1 Block Diagram of adaptive filter

Adaptive equalizers use adaptive algorithms to minimize signal errors. It is selected based on the performance measures such as rate of convergence, misadjustment, level of complexity and numerical properties. The various algorithms used in adaptive equalizers are Zero forcing (ZF), least mean squares (LMS), Kalman, and LSL[3]. LMS algorithm is popularly used because of fast convergence, low complexity and superior performance. A fast convergence feature of LMS algorithm takes minimum time to compute filter coefficients. During each sample period, the algorithm updates the filter weights by using the estimated error. The operations of LMS algorithm are

1. Calculates the output signal  $y(n)$  from the FIR filter

$$y(n) = \sum_{j=1}^p \hat{w}_j(n)x_j(n) \quad (1)$$

2. Updates the filter coefficients by using the following equation:

$$W(n+1) = \hat{w}(n) + \eta[d(n) - x^T(n)\hat{w}(n)]x(n) \quad (2)$$

The filter coefficient is  $w(n)$ , the step size is  $\eta$ , the input signal is  $x(n)$ , and the number of samples is  $n$ . Traditional adaptive filters are complex in terms of area, time and performance. Using an efficient addition scheme for error computation and weight update, this paper proposes an LMS Finite Impulse Response (FIR) adaptive filter. In addition, the proposed architecture has a high convergence factor and reduces the critical path.

## 2. Conventional Adaptive Filter

The conventional adaptive filter structure consists of  $N$  multipliers. The error computation block of conventional filter is shown in Fig.2(i). The multiplier consists of two inputs, one input is from the common tap delay line which has delayed input signals  $x(n-D)$  and the other input comes from 2:1 multiplexer. The multiplexer gets the inputs from error block i.e. the estimated error value multiplied by the step size and updated coefficient values from weight update block [5]. The proposed structure also consists of  $N$  adders for calculating  $N$  weights. The adder tree produces output based on  $N$  multipliers. It is possible to estimate the error signal by subtraction of expected and actual responses from the output signal. A 2:1 de-multiplexer is required for the product to be passed on to either the adder tree blocks or the weight update blocks.

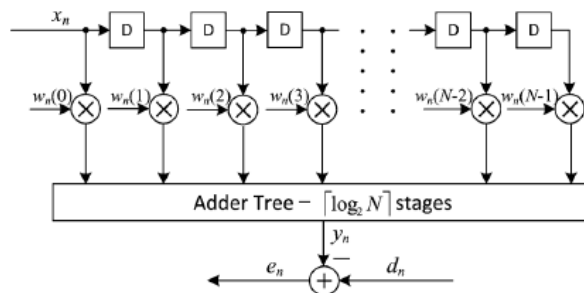


Fig. 2(i). Error Computation Block

The weight updation block is shown in Fig.2 (ii). In error computation block, the error value gets multiplied with step size and pipelined latch is introduced. The multiplication is performed using shift method. Both the blocks uses same set of Registers. So, the number of registers used gets reduced.

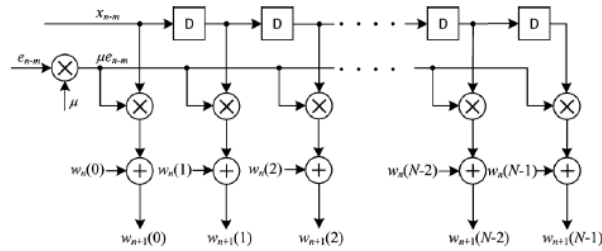


Fig. 2(ii). Weight Update Block

### 3 Implementation Of Proposed Structures

#### A. Zero Adaptation Delay Adaptive Filter

Zero adaptation delay denotes that the computation of error value and weight updating takes place at the same clock cycle. This cannot occur concurrently because the structure is non-pipelined[7]-[9]. Zero adaptation delay can be achieved by making the blocks to complete its operation within half clock cycle and multiplexing the multipliers. The registers are shared in both the blocks. The register overhead is reduced in the architecture. The zero adaptation delay adaptive filter is presented in Fig 3.

At every clock cycle, a new input sample is taken. During the clock period, the multiplexer transfers the weight present in registers to multipliers. After multiplication, the multiplier passes the product words to adder tree to calculate the filter output through the demultiplexers and the subtractor computes the error value. After right shift operation, the error computed values are applied to multipliers that are present in weight update block.

The functionality of filter is based on select lines of the multiplexer and demultiplexer. When the select line is zero, then the filter updates the coefficient values and when select line is one it functions as normal FIR filter. Since the error is multiplied by the step size in error computation block and given to weight update blocks, adaptation time of the filter is totally decided by the performance of those two blocks. The weight updation takes lesser time when compared to error computation, Therefore, the structure is implemented in such a way that error computation is done first and weight updation is performed in cycle 2[7]-[11].

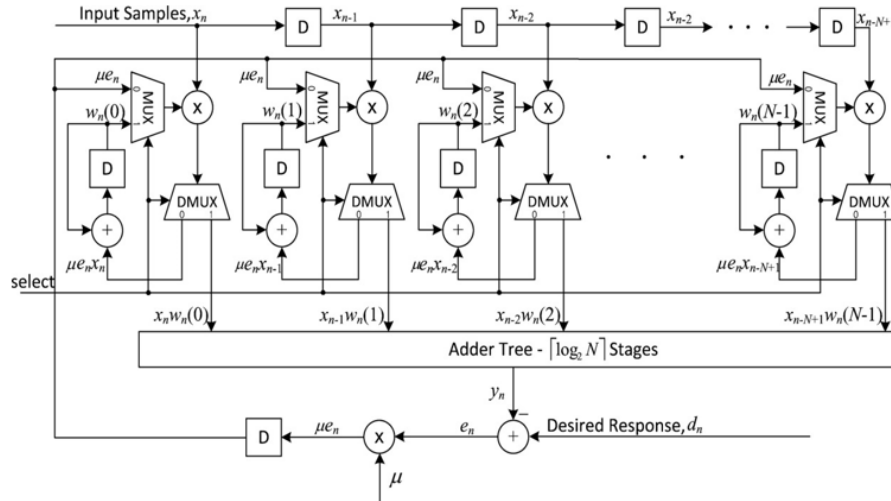


Fig. 3. Structure of zero adaptation delay adaptive filter

### B. Two Adaptation Delay Adaptive Filter

Fig.4 shows the proposed LMS adaptive FIR filter structure with two adaptation delays. Three pipeline stages are used to implement the structure. The error computation block includes an adder tree in the first stage of the pipeline. The weight update block is present in third pipeline stage. Compared to conventional adaptive filter, this structure requires more registers because of pipelining. This structure has  $N$  multipliers and  $N$  adders for calculating weights. The adder tree produces output based on  $N$  multipliers.

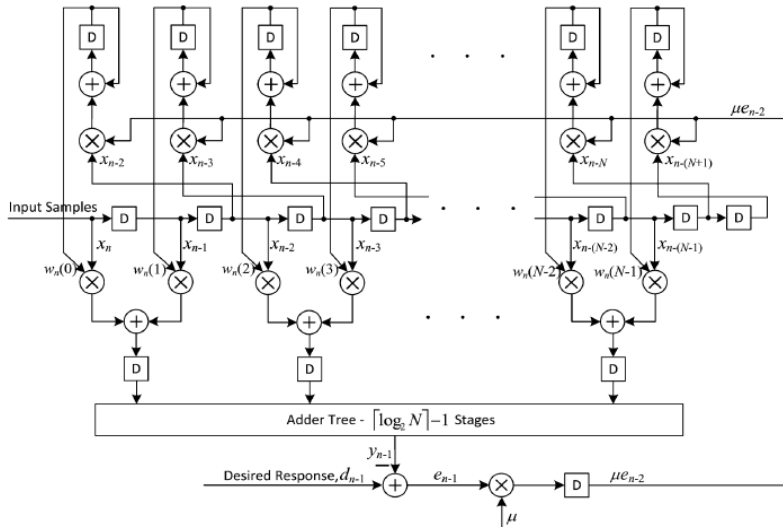


Fig. 4. Structure of two adaptation delay adaptive filter

## 4 Simulation Results

The conventional LMS Adaptive filter and the proposed structures are implemented using Verilog HDL. This design is simulated using Modelsim 6.4c and Synthesized by Xilinx 13.2/9.1[12]-[15].The comparison is made on area and delay of conventional, zero adaptation delay and two adaptation delay adaptive filters.The simulation waveform of conventional filter is presented in Fig. 5. The simulated waveform shows that when reset goes high then the error value and expected response value is same since the output value is zero. If reset goes low, the filter calculates the error value and update the filter coefficient value with one adaptation delay that is with one clock cycle delay.

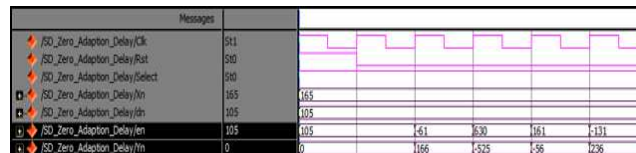


Fig. 5. Simulation result of Conventional adaptive filter

The simulation wave form of zero adaptation delay filter is shown in Fig. 6. From the waveform, it is inferred that if reset is zero, the filter calculates the error value and update the filter coefficient value without any delay. Hence, the structure is called zero adaptation delay adaptive filter.



Fig. 6. Simulation result of zero adaptation delay adaptive filter

The output waveform of filter is shown in Fig.7.This structure calculates the error value and updates the filter coefficients with delay of two clock cycles.



Fig. 7. Simulation result of two adaptation delay adaptive filter

Table I shows the comparison between conventional, zero adaptation delay and two adaptation delay adaptive filters. From the comparison table, it is inferred that hardware

requirement for zero adaptation delay adaptive filter is lesser than two adaptation delay adaptive filter at the cost of increase in delay.

Table I Comparison on area and delay

Method Name	Area			Delay		
	Gates	Slice FF	LU T	Max Delay (ns)	Gate Delay (ns)	Path Delay (ns)
<b>Proposed Structures</b>						
A. Zero Adaptation Delay[6]	17,253	78	165	21.205	13.879	7.125
B. Two Adaptation Delay[6]	33,017	98	99	17.241	13.118	4.288
Conventional Adaptation Delay[6]	33,441	33	110	23.303	16.855	6.448

## 5 Conclusion

A low-complexity LMS adaptive filter architectures are proposed based on area and delay calculations. The proposed structure has fast convergence factor than the transpose form adaptive filter. But the drawback is delays produced due to weight adaptation and large area requirement. To overcome these drawbacks, the LMS adaptive filter is proposed with zero adaptation delay adaptive filter and two adaptation delay adaptive filter. Zero adaptation delay adaptive filter has minimum area requirement. But, the drawback is extra select pin needed and this architecture will not update the coefficient value automatically. So, it can be used in the areas where noise is very less like noise cancelling in AC electrical measurements. In two adaptation delay adaptive filter, path delay is very less and it will automatically update the coefficient value based on the error, so no need of extra pins to update the coefficient values. The weights get updated in two clock cycle. It can be used in application which require accurate data like noise removal in ECG signals.

## References

- [1] W. A. Harrison, J. S. Lim, and E. Singer, "A new application of adaptive noise cancellation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 34, no. 1, pp. 21–27, Feb. 1986.
- [2] R. H. Hearn, J. R. Zeidler, E. Dong, Jr., and R. C. Goodlin, "Adaptive noise cancelling: Principles and applications," *Proc. IEEE*, vol. 63, no. 12, pp. 1692–1716, Dec. 1975.
- [3] Harjeet Kaur and Dr. Rajneesh Talwar, "Performance Comparison of Adaptive Filter Algorithms for Noise Cancellation" *IEEE Signal Process Letters.*, vol. 16, no. 1, Jan. 2009.
- [4] P. K. Meher and M. Maheshwari, "A high-speed FIR adaptive filter architecture using a modified delayed LMS algorithm," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2011, pp. 121–124.
- [5] G. Long, F. Ling, and J. G. Proakis, "The LMS algorithm with delayed coefficient adaptation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 37, no. 9, pp. 1397–1405, Sep. 1989.
- [6] M. D. Meyer and D. P. Agrawal, "A modular pipelined implementation of a delayed LMS transversal adaptive filter," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 1943–1946.

- [6] Pramod Kumar Meher, Sang Yoon Park, "Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm," in IEEE Transaction on Circuits and Systems—I: regular papers, vol. 61, no. 3, March 2014
- [7] S. Haykin and B. Widrow, Least-Mean-Square Adaptive Filters. Hoboken, NJ, USA: Wiley-Interscience, 2003.
- [8] G. Long, F. Ling, and J. G. Proakis, "The LMS algorithm with delayed coefficient adaptation," IEEE Transaction on Acoustic, Speech, Signal Processing, vol. 37, no. 9, pp. 1397–1405, Sep. 1989.
- [9] L. D. Van and W. S. Feng, "An efficient systolic architecture for the DLMS adaptive filter and its applications," IEEE Transaction on Circuits System II, Analog Digital Signal Processing, vol. 48, no. 4, pp. 359–366, Apr. 2001.
- [10] L.-K. Ting, R. Woods and C. F. N. Cowan, "Virtex FPGA implementation of a pipelined adaptive LMS predictor for electronic support measures receivers," IEEE Transaction on Very Large Scale Integration, vol. 13, no. 1, pp. 86–99, Jan. 2005.
- [11] E. Mahfuz, C. Wang, and M. O. Ahmad, "A high-throughput DLMS adaptive algorithm," IEEE International Symposium on Circuits System, pp. 3753–3756, May 2005.
- [12] G. A. Clark, S. K. Mitra, and S. R. Parker, "Block implementation of adaptive digital filters," IEEE Trans. Acoust., Speech, Signal Process., vol. ASSP-29, no. 3, pp. 744–752, Jun 1981.
- [13] S. Y. Park and P. K. Meher, "Low-power, high-throughput, and low-area adaptive FIR filter based on distributed arithmetic," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 6, pp. 346–350, Jun. 2013.
- [14] <https://www.xilinx.com>