Design and Implementation of Folded QRS Detector for Implantable Cardiac Pacemaker

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Abstract. This paper proposes an area and power efficient technique for the design of an ECG detector. In biomedical applications, like the ECG detector for implantable cardiac pacemaker systems, area and power consumption plays a major role. Thusin this paper an area efficient ECG detector with folded pipelined FIR filter is proposed. In conventional wavelet filter bank structure,the decimated wavelet filter bank used makes use of 3 LPFs and 1 HPF of pipelined architecture. This pipelined filter structure requires more hardware. Thus in the proposedarchitecture folding transformation technique has been applied to the pipelined filter structure in order to reduce the hardware. The decimated wavelet filter bank consisting of the filter structures followed by downsamplers is used to denoise the ECG signal. The QRS complex detector consisting of a comparator, counter and a threshold block is used to find the correct location of the QRS complex.In order to furtherreduce the number of registers that occurs as a resultof the folding transformation, folding transformation with register minimization technique is applied to the pipelined filter that results in less hardware utilization.The proposed technique is implemented using XilinxSytem Generator. Thus a total area of 22.78% is saved using the proposed method. Considerably a low power of 115mW is also achieved which makes it useful for high performance medical applications.

Keywords: Implantable Cardiac Pacemaker (ICP),Wavelet Filter Bank (WFB),ElectroCardiogram (ECG),Detection Error Rate (DER)..

1 Introduction

Enhanced health care and cost reduction has become a major challenge for the aging population. The demand for health care applications such as the implantable medical devices are nowadays increasing rapidly. One of the most commonly used biomedical devices is the cardiac pacemaker which is implanted in the human body to detect and monitor the heart beating rate of a person. The required cure is provided to a patient after receiving abnormal signals from the pacemaker[1].The Electrocardiogram (ECG) detector used in the cardiac pacemakers checks the heart-beating rate and rhythm with the help of digitized signals.The ECG has three main components: the P wave, which depolarizes the atria; the QRS complex, which depolarizes the ventricles; and the T wave, which repolarizes the ventricles. Of all the three waves QRS complex has higher larger amplitude over R –R interval than the P and T waves. In order to monitor the heart beating rate of the patients in precise, the exact detection of R wave is required. QRS detection offers the foundation for almost all ECG analytical algorithms, as after the QRS diagnosis the heart rate and certain other parameters can be

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analyzed to prevent severe pathologies. The pacemaker once implanted into the body is expected to operate with high detection reliability over several years.To avoid repeated surgeries due to battery exhaustion, low power and area consumption is another extremely important design requirement[2].Here a novel method to implement the ECG detector is proposed.

The paper is organized as follows: Section I provides an introduction to the paper. The literature survey done is described in Section II. Section III provides information about the conventional detector design approach. The proposed ECG detector design approach is described in Section IV. The performance evaluation and the simulation results of the proposed technique are detailed in Section V. Finally,Section VI concludes the paper.

2 Literature Review

In [1] Bhavtosh and D. Berwalproposes the design of QRS complex detector with Multi Scaled product and Soft Threshold algorithms. A radix-4 Booth multiplier is used in the detection of the QRS complex wave. This detector has lesser complexity. Though the overall delay is reduced, the hardware utilization is more. In [2] Y.J. Min, H.K. Kim, Y.R. Kang, G.S. Kim, J. Park and S.W. Kim proposes the design of wavelet-based ECG detector with wavelet filter banks, a noise detector and a QRS complex detector of hypothesis testing with the wavelet demodulated ECG signals.The detection accuracy of the detector is high and has low power consumption whereas the hardware utilization is more as the wavelet filter bank (WFB) uses more number of LPFs and HPFs. The wavelet-based R-wave detector proposed [3] is implementedusing 0.13-um low-leakage UMC technology. When the patient is not exposed to noise, power is saved by a mode that usually closes nearly two-third of the hardware.This technique has the advantage of reduced leakage power by the addition of sleep transistors in the rails of the power supply. Though the leakage power of the detector is reduced, the inclusion of a noise detector adds onto to the hardware utilization.The design of QRS complex detector proposed [4] uses dyadic wavelet transform (DyWT) which is generally robust to time-varying QRS complex based morphology.For the contractions of ventricles in the earlier stages like the couplets tapes and bigeminy, the proposed DyWT-based detector exhibits better performance. The detector is robust to noise and has excellent flexibility in analyzing the time varying characteristics of ECG data. An approach to the design of QRS complex detector [5] is proposed where the complexes are detected by the application of a very simple morphological operator. The operator acts as an extractor in the peak valley and is then operated by a structuring component. This helps in very quick execution time.A drawback of this technique is that testing in 24-hr Holter ECG recordings is required in order to completely assess the performance of the detector which istime consuming.

3 Conventional ECG Detector

The ECG detector usually consists of two main components : the wavelet filter bank and the QRS complex detector [6].

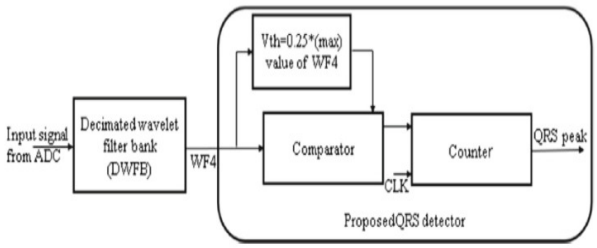

Fig.1.Block Diagram of the ECG Detector

Wavelet Filter Bank

The wavelet filter bank circuit is based on the decimated wavelet transform. There are several wavelet transforms used in general like Dyatic, Haar, Symlet and Biorthogonal wavelet transform [4]. Here biorthogonal 2.2 wavelet transform is used since it has better SNR and resembles an ECG wave.The wavelet filter bank consists of 3 low pass and a high Pass filters namely WFB1, WFB2, WFB3 and WFB4 followed by down samplers [6]-[7]. The filter structures are pipelined-based architectures.Pipelining is an important technique used in several applications such as digital signal processing (DSP) systems. It results in the increasing the speed of the critical path The pipelined structure is obtained by introducing delays done by means of cut set introduction to a normal 3-tap FIR filter.The Wavelet Filter banks are used to filter the noise where at each stage the clock frequency gets divided by 2 and finally the original signal is obtained [6]. The Fig.2 shows the wavelet filter bank structure and Fig.3 shows the pipelined architecture of the filter.

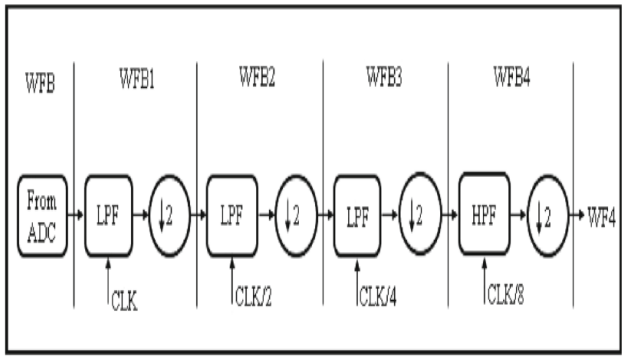

Fig.2. Block Diagram of the Wavelet Filter Bank

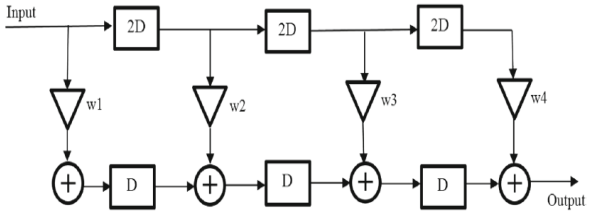

Fig.3.Pipelined Architecture of the FIR Filter

QRS Complex Detector

QRS complex detector can consists of two types of threshold: hard threshold and the soft threshold [2].The QRS complex detector in the used here consists of a soft threshold, a comparator and a counter as shown in Fig.1. The output of the WFB4 is given to the comparator and the soft threshold (Vth) is set at the maximum value of one fourth that is 0.25 of the wavelet filter bank (WFB) output. The comparator compares the wavelet filter bank (WFB) output with the threshold value. If the output of WFB4 is greater than the threshold it is counted as a peak otherwise it is not counted as a peak. The number of peaks in total is counted by the counter[6].

3 Proposed ECG Detector

A. Folding

Folding is a technique in which a single functional unit is used which performs many algorithm operations based on time multiplexing.Folding techniquethus helpsto reduce the number of computational blocks used. Though folding reduces the area occupied in the chip it also leads to increase in the number of registers used in the design. In orderminimise the number of registers, register minimization technique is adopted in which the number of register are reduced by means of a life time chart [8][10].

B. Folding of Pipelined FIR Filter

Let us consider the pipelined FIR filter shown in Fig.3The filter has folding order N=4 and folding sets S1 = {3, 1, 2, 0} for adders and S2 = {0, 2, 3, 1} for multipliers. The folding equation is given by,

$$\boldsymbol{D_F(U \rightarrow V) = NW(e) - P_U + v - u} \quad (1)$$

Where W(e) represents the weight of the edge,$P_U$represents the pipelined stages,v and u represents the folding order of V and U node respectively [10].

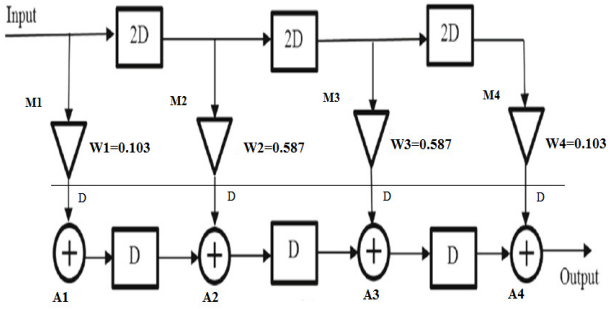

Fig .4.Pipelined FIR filter showing cut set retiming

The folding equation is applied to all the edges present in the filter to find the number of delays present in the folded structure.

$$\boldsymbol{D_F(A1 \rightarrow A2) = 4(1) - 1 + 1 - 3 = +1}$$
$$\boldsymbol{D_F(A2 \rightarrow A3) = 4(1) - 1 + 2 - 1 = +4}$$
$$\boldsymbol{D_F(A3 \rightarrow A4) = 4(1) - 1 + 0 - 2 = +1}$$
$$\boldsymbol{D_F(M1 \rightarrow A1) = 4(0) - 2 + 3 - 0 = +1}$$

$$D_F(M2 \rightarrow A2) = 4(0) - 2 + 1 - 2 = -3$$
$$D_F(M3 \rightarrow A3) = 4(0) - 2 + 2 - 3 = -3$$
$$D_F(M4 \rightarrow A4) = 4(0) - 2 + 0 - 1 = -3 \qquad (2)$$

Since the folding equations consist of negative values for edge M1→A2, M3→A3, M4→A4 and it cannot be realized,cutsets are applied in these paths as shown in Fig.4 to perform retiming. The retimed pipelined FIR filter is shown in Fig .4. Again the folding equations are applied to the retimed filter to construct the folded filter.

$$D_F(A1 \rightarrow A2) = 4(1) - 1 + 1 - 3 = 1$$
$$D_F(A1 \rightarrow A3) = 4(1) - 1 + 2 - 1 = 4$$
$$D_F(A3 \rightarrow A4) = 4(1) - 1 + 0 - 2 = 1$$
$$D_F(M1 \rightarrow A1) = 4(1) - 2 + 3 - 0 = 5$$
$$D_F(M2 \rightarrow A1) = 4(1) - 2 + 3 - 0 = 1$$
$$D_F(M3 \rightarrow A3) = 4(1) - 2 + 2 - 3 = 1$$
$$D_F(M4 \rightarrow A4) = 4(1) - 2 + 0 - 1 = 1 \qquad (3)$$

As there are no negative values in the folding equations (14) to (16), the folded architecture can be constructed from the folding sets and the folding equations.

C. Register Minimisation Technique

In orderminimise the number of registers, register minimization technique is adopted in which the number of register are reduced by constructing the life time table [8]. The life time of a node is given by,

$$T_{input} \rightarrow T_{output}$$
$$U + P_U \rightarrow U + P_U + max_V\{D_F(U \rightarrow V)\} \qquad (4)$$

Where T_{input} and T_{output} represents the time instance of input and output variables.

TABLE I.Lifetime for retimed Pipelined FIR filter

Nodes	**Tinput→Toutput**	
A1	4	4 → 5
A2	2	2→ 6
A3	3	3→ 4
A4	4	1→ 1
M1	5	2 → 7
M2	6	4 → 5
M3	7	5 → 6
M4	8	3 → 4

From the life time values shown in 0life chart for the retimed FIR filter is constructed as shown in Fig .5

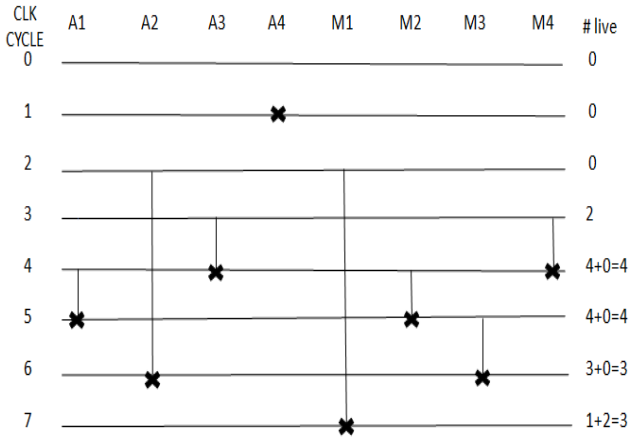

Fig.5.LifeTime chart for the retimed FIR filter

From Fig.5 it is clear that the maximum number of registers required is 4. By using only 4 registers data allocation table is constructed as shown TABLE II.

TABLE II. Data Allocation Table

CLOCK CYCLE	INPUT	R1	R2	R3	R4	OUTPUT
0						
1	A4					A4
2	A2 , M1					
3	A3 , M4	A2	M1			
4	A1 , M2	A3	A2	M1	M4	M4,A3
5	M3	A1	M2	A2	M1	A1,M2
6		M3		M1	A2	M3,A2
7				M1		M1

Using the data allocation table as shown in the above table,the folded pipelined filter with minimum number of registers is shown in Fig.6.

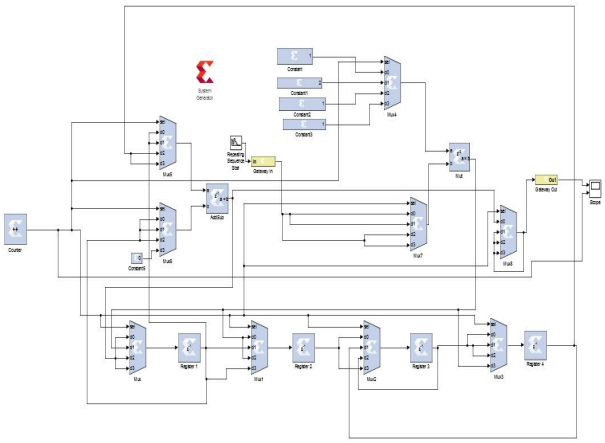

Fig.6.Folded pipelined FIR filter

4 Simlulation Results and Discussions

Filter Design using FDA Tool

The FIR filter is designed using the Filter Design and Analysis Tool (FDA Tool).The conventional ECG is of 0.05-100 Hz but higher frequencies are also present in ECG signal [9].Generally, the incoming ECG signals must be sampled (digitized) at least at twice the rate of the highest frequency of interest for the high frequencies signal retention otherwise the signals are distorted. This means that if the frequency range of interest is in the 150-250 Hz range, the sampling rate must be at least 500 Hz. In practice a higher sampling rate is required, and therefore in most high frequency applications the sampling rate has been 1000 Hz or more[11]-[13].

The properties of the filter are given using the FDA tool and the filter coefficients are obtained both for the pipelined Low pass and High pass filters.The filter order is 3.The Fig.7 shows the setting of FDA tool.

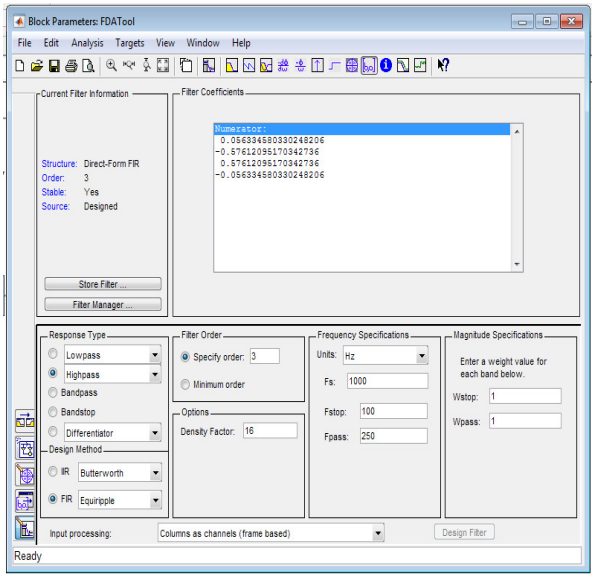

Fig.7.FDA tool design wizard

Wavelet Filter Bank Implementation using System Generator

The decimated wavelet filter bankis implemented in system generator as shown in Fig.11using the above specification. The filter coefficients are taken from the FDA tool. The filter bank consists of pipelined LPFs and HPFs as shown in Fig.8 The filter is tested using the .mat files taken from MIT-BIH arrhythmia database[14]-[16]. The noise signals are added to theECG signal and finally the filtered output is obtained. The output of the wavelet filter bank for a input of 100.mat ECG signal is shown in Fig.10.

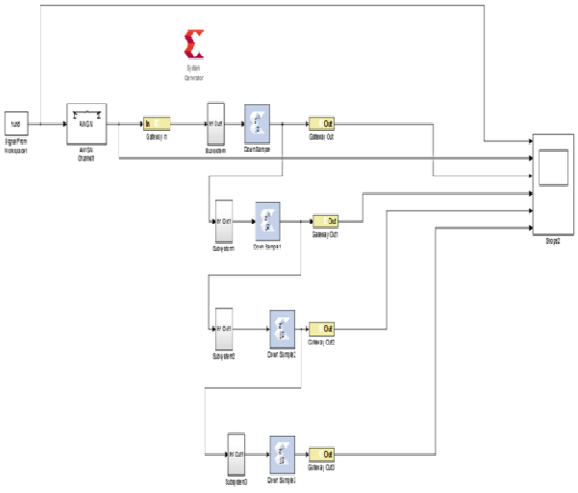

Fig.8. Decimated Wavelet Filter Bank

The subsytem of the filter bank which is the pipelined FIR filter structure is shown in Fig.9

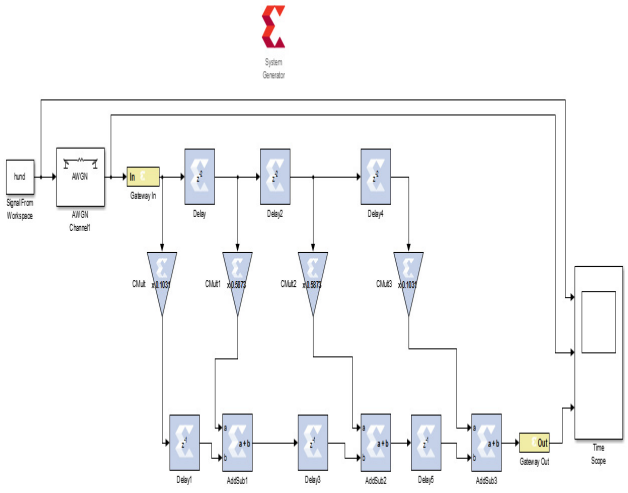

Fig.9. Pipelined FIR Filter Implementation

The output waveforms for nearly 10 samples of ECG signal taken from the MIT-BIH Arrhythmia database were obtained. The output waveform for .100 mat file is shown in Fig.10.The first window in Fig.10 shows the input ECG signal, the second window shows the noise added input signal,window three, four and five shows the output of LPF's after each stage of noise filteration.The window six shows the output of HPF which is the final reconstruted input signal after noise removal.

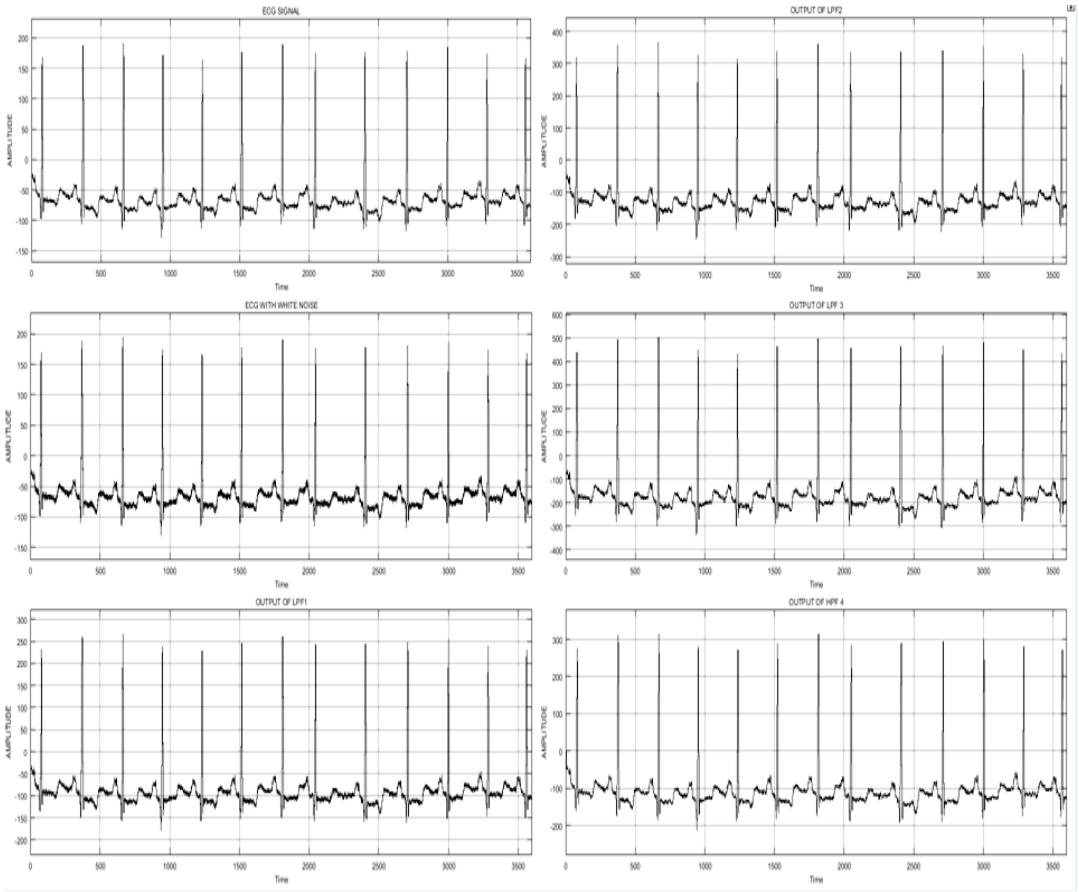

Fig.10.Output of Decimated Wavelet Bank for an input of 100.mat ECG signal

Implementation of QRS Complex Detector

The QRS complex detector circuit is design with a soft threshold block, a comparator and a counter. Output of the WF4 is given to the comparator and a soft threshold is set at the maximum value of one fourth that is 0.25 of the wavelet filter bank output. The comparator compares the wavelet filter bank (WFB) output with the threshold value. If the output of WFB4 is greater than the threshold, it is counted as a peak otherwise no peak is counted[17],[18]. The total number of peaks is counted by the counter.

The output waveforms for nearly 10 samples of ECG signal taken from were taken. The output waveform for .100 mat file is shown in Fig.12 the first window shows the input ECG sisgnal,second window shows the noise added input signal and the last one shows the detection of a QRS Complex.

The implementation of the QRS complex detector for an input of 100.mat ECG signal is shown in Fig.11.

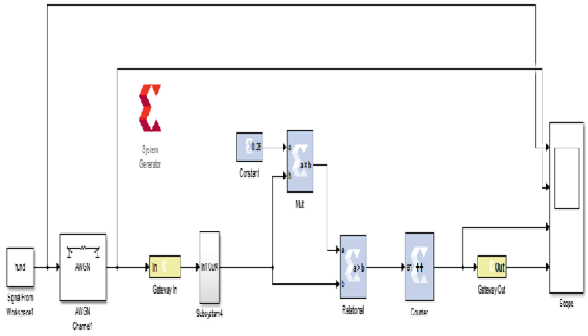

Fig.11. Implementation of QRS Complex Detector

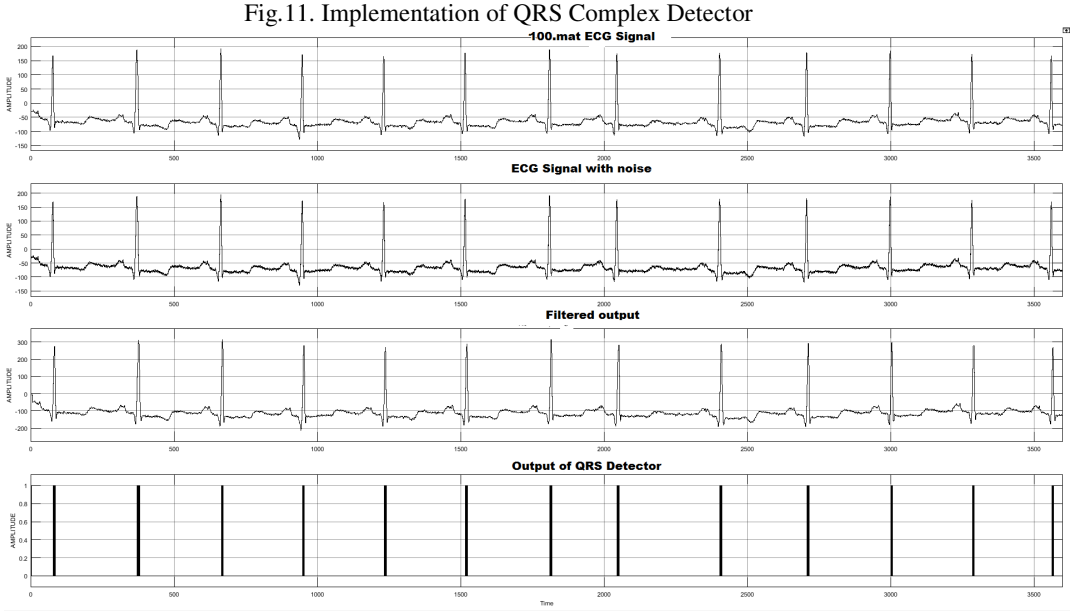

Fig .12. Output of QRS Complex detector for an input of 101.mat ECG signal

Performance Parameters

The performance parameters for the ECG detector such as sensitivity (Se), predictivity (P+) and Detection Error Rate (DER) for different samples of ECG signal are calculated and tabulated [12],[19].

Sensitivity (Se) is given as follows

$$Se = \frac{TP}{TP + FN}\% \qquad (5)$$

Where TP is the true positive which represents the number of correctly detected QRS complexes and FN is the false negative which denotes the number of missed detections.

Positive predictivity (P+) is given as follows

$$P^{+} = \frac{TP}{TP + FP}\% \qquad (6)$$

Where FP is the false positive which denotes the detection of false QRS complexes.

Detection Error Rate (DER) is calculated using

$$DER = \frac{FP + FN}{TOTAL\ NUMBER\ OF\ QRS\ COMPLEXES}\% \qquad (7)$$

Table III. Performance parameter of the Pipelined Filter Based ecg detector for different samples of ecg signal Using 10 second MIT-BIH Database

ECG Signal	*Total (beats)*	*TP (beats)*	*FN (beats)*	*FP (beats)*	*Se (%)*	*P^{+} (%)*	*DER (%)*
100	*13*	*0*	*0*	*0*	*100*	*100*	*0*
101	*13*	*13*	*0*	*1*	*100*	*92.85*	*0.07*
102	*12*	*11*	*1*	*0*	*91.66*	*100*	*0.08*
103	*14*	*13*	*1*	*1*	*92.85*	*92.85*	*0.14*
104	*13*	*13*	*0*	*0*	*100*	*100*	*0*
105	*11*	*11*	*0*	*1*	*100*	*92.85*	*0.07*
106	*13*	*12*	*1*	*0*	*92.30*	*100*	*0.07*
107	*12*	*11*	*1*	*0*	*91.66*	*100*	*0.08*
108	*11*	*11*	*0*	*0*	*100*	*100*	*0*
109	*14*	*14*	*0*	*1*	*100*	*92.85*	*0.06*
Total	*126*	*122*	*5*	*5*	*96.84*	*97.14*	*0.07*

Thus a sensitivity of 96.84%, positive predicitivity of 97.14% and Detection Error Rate (DER) of 0.07% is achieved using the pipelined filter based ECG detector circuit for 10 second MIT-BIH Database.

Table iv. Performance parameter of the Pipelined Filter Based ecg detector for different samples of ecg signal Using 1 Minute mit-bih Database

ECG Signal	*Total (beats)*	*TP (beats)*	*FN (beats)*	*FP (beats)*	*Se (%)*	*P^{+} (%)*	*DER (%)*
100	*75*	*75*	*0*	*0*	*100*	*100*	*0*
101	*74*	*73*	*1*	*0*	*98.64*	*100*	*0.013*
102	*74*	*74*	*0*	*0*	*100*	*100*	*0*
103	*71*	*71*	*0*	*1*	*100*	*98.61*	*0.014*

104	***74***	***74***	***1***	***0***	***98.66***	***100***	***0.013***
105	***70***	***70***	***0***	***1***	***100***	***98.59***	***0.014***
106	***73***	***72***	***1***	***0***	***98.63***	***100***	***0.013***
107	***79***	***76***	***2***	***0***	***97.43***	***100***	***0.025***
108	***70***	***70***	***0***	***2***	***100***	***97.22***	***0.028***
109	***75***	***75***	***0***	***0***	***100***	***100***	***0***
Total	***735***	***730***	***5***	***4***	***99.33***	***99.44***	***0.12***

Thus a sensitivity of 99.33%, positive predicitivity of 99.44% and Detection Error Rate (DER) of 0.12% is achieved using the pipelined filter based ECG detector circuit for 1minute MIT-BIH Database.

Resource Utilization of ECG Detector

The system created in system generator is converted to HDL netlist. For synthesis Zedboard and Zynq Evaluation board is selected and imported to Xilinx Vivado 2016.2 and then the analysis of resource utilization, power and delay consumption is done [20]. The overall resource utilization of the pipelined filter and folded filter structures and the total area saved is as shown in TABLE V.

Table v. Comparison of Resource utilization of the Existing and Proposed Architectures

IMPLEMENTATION	***Slice LUTs (Out of 53200)***	***Slice Flip Flops (Out of 106400)***	***Slice DSPs (Out of 220)***	***Slice IOs (Out of 200)***	***Slice LUT RAMs (Out of 17400)***	***Overall percent of resource used (%)***
Conventional Pipelined FIR Filter	***188***	***147***	***0***	***33***	***48***	***22.12***
Proposed Folded Filter	***104***	***105***	***1***	***33***	***48***	***17.08***
Total Area Saved in (%)						***22.78***

The power consumed by the sytem using pipelined filter structure is shown in Fig 13.

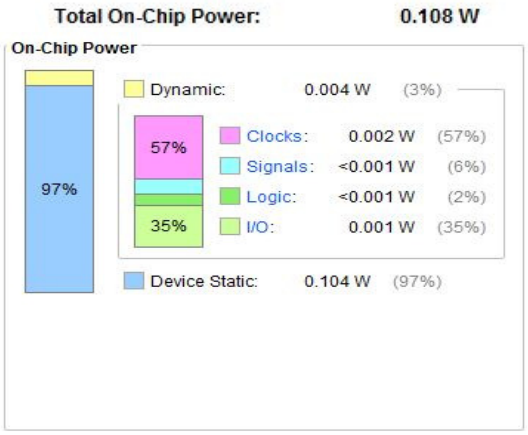

Fig.13. Power consumed by the system using pipelined filter structure

The power consumed by the system using folded filter structure is shown in Fig.14

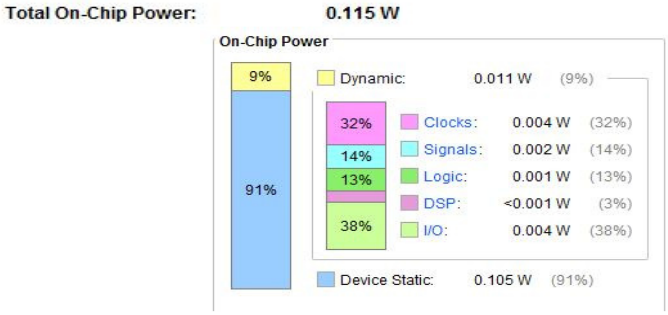

Fig.14. Power consumed by the system using Folded filter structure

Thus it can be seen that a total area of 22.78% is saved using the proposed technique. The total on chip power of the proposed circuit using folded filter structure is only 0.115W.

Comparison of Proposed Architecture with Existing Method

The comparison of total hardwares used between the proposed method and the existing method is shown in TABLE VI.

Table vi.Comparison of Hardwares Between Proposed Architecture and existing method

HARDWARES USED	CONVENTIONAL ECG DETECTOR (PIPELINED FIR FILTER BASED)	MODIFIED ECG DETECTOR (FOLDED FIR FILTER BASED)

Adder	4	1
Multiplier	4	1
Registers	9	4

Conclusion

An area efficient ECG detector for Implantable Cardiac Pacemaker Systems is proposed in this paper. The hardware efficient wavelet filter bank consisting of low pass and high pass filter structures help in the filtering of noise added ECG signals. The R-wave peak detection is also achieved by means of the QRS complex detector. Thus reduced hardware utilization is achieved by applying folding transformation with register minimization technique to the pipelined FIR filter. A total area of 22.78% is saved using the proposed technique. The total on-chip power consumed by the detector is also considerably less which is 115mW. This makes the design hardware and power efficient. The proposed methodology can further be extended to areas of data compression of ECG signals using Run-Length Encoding (RLE) technique.

References

[1] Bhavtosh, D. Berwal and Y. Kumar, "High performance QRS complex detector for wearable ECG systems using Multi Scaled product with booth multiplier and soft threshold algorithm," IEEE International Conference on Signal Processing and Communication (ICSC), Noida,vol. 15, pp. 204-209,2015.

[2] Y. Min, H. Kim, Y. Kang, G. Kim, J. Park and S. Kim, "Design of Wavelet-Based ECG Detector for Implantable Cardiac Pacemakers," in IEEE Transactions on Biomedical Circuits and Systems, vol. 7, no. 4, pp. 426-436, Aug. 2013.

[3] S. Kadambe, R. Murray, andG. F. Boudreaux-Bartels, "Wavelet transform-based QRS complex detector," IEEE Trans. Biomed. Eng., vol.46, no. 7, pp. 838–848, Jul. 1999.

[4] R. S. Sanders and M. T. Lee, "Implantable pacemakers," Proc. IEEE, vol. 84, no. 3, pp. 480–486, Mar. 1996.

[5] P. E. Trahanias, "An approach to QRS complex detection using mathematical morphology," in IEEE Transactions on Biomedical Engineering, vol. 40, no. 2, pp. 201-205, Feb. 1993.

[6] A. Kumar, D. Berwal,Y. Kumar, "Design of High-Performance ECG Detector for Implantable Cardiac Pacemaker Systems using Biorthogonal Wavelet Transform" Circuits Syst Signal Process ,vol. 37, pp. 3995–4014,2018.

[7] A. Kumar ,R. Komaragiri,M. Kumar "Design of wavelet transform based electrocardiogram monitoring system" ISA Transactions, vol. 80,pp. 381-398,2018.

[8] A. Joy and C. S. Vinitha, "Folding and Register Minimization Transformation on DSP Filter,"5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur,vol.18, pp. 1-6,2018.

[9] S.M.Szilagyi,L.Szilagyi," Wavelet transform and neural-network-based adaptive filtering for QRS detection," in Proc.22nd Annual International Conference ,IEEE Engineering in Medicine and Biology, Soc.Chicago,IL,USA,vol.2, pp.1267-1270,Jul.2003.

[10] Keshab K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley & Sons, 1999.
[11] S.Kadambe ,P. Srinivasan “Adaptive wavelets for signal classification and com-pression. Int J Electron Commun (AEÜ), vol. 60,pp 45–55,2006.
[12] D. L. Donoho, "De-noising by soft-thresholding," in IEEE Transactions on Information Theory, vol. 41, no. 3, pp. 613-627, May 1995.
[13] K.K. Parhi “High level Algorithm and Architectures for DSP synthesis” Journal of VLSI Signal Processing, vol. 9,pp.121-143,1995.
[14] J. Pan and W. J. Tompkins, “A real-time QRS detection algorithm,”IEEE Trans. Biomed. Eng., vol. 32, no. 3, pp. 230–236, Mar. 1985.
[15] K. K. Parhi and T. Nishitani, “Folded VLSI architecture for DiscreteWavelet Transforms”, IEEE International Symposium on Circuits and Systems,Chicago,vol. 3, pp. 1734-1737,May 1993.
[16] A. Kumar, R. Komaragiri, M. Kumar, “Heart rate monitoring and therapeutic devices:A wavelet transform based approach for the modeling and classification of congestive heart failure,” ISA Transactions, vol. 79,pp. 239-250,2018.
[17] Chio-In Ieong, Pui-In Mak,“A 0.83- QRS Detection Processor Using Quadratic Spline Wavelet Transform for Wireless ECG Acquisition in 0.35-µm CMOS” IEEE transactions on biomedical circuits and systems, vol.6, no.6, pp.586-595,Dec.2012.
[18] Jiang and A. Willson Jr., “ Efficient digital filtering architecturesusing pipelining,” IEEE Trans. Circuits Syst. II,Analog Digital Signal Process., vol. 44, no. 2, pp. 110-119, Feb. 1997.
[19] J.P. Martinez, R. Almeida, S. Olmos, A. P. Rocha, and P. Laguna. “A wavelet-based ECG delineator: Evaluation on standard database” IEEE Trans. Biomed. Eng,vol. 51,pp. 570–581,2004.
[20] K. K. Parhi, C. Y. Wang, and A. P. Brown, “Synthesis of control circuits in folded pipelined DSP architectures,” IEEE J. Solid-State Circuits, vol. 27, no. 1, pp. 29-43, Jan. 1992.