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Battery life optimization techniques for ultra-low power SOCs

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Abstract

The urge for devices with longer battery life in today's compute world has motivated multiple changes in the design, architecture, and SW optimizations. Ultra-Low Power products [Mobiles, Tablets, Notebooks, and Convertibles] are constrained by 2 major factors – thermal dissipation and supply of battery power. Thermal dissipation restricts power consumption of application processor, which additionally limits computational performance. Battery usage time is determined by power consumption of the device. Due to these reasons, power management to improve efficiency of electric power usage becomes a very crucial part of ULP products. Battery life suite is introduced with real time use cases or KPI's to analyze battery life of the product. This paper presents the optimizations that were developed for improving the battery life performance of ULP SoCs. The use cases/KPI's defined in BL suite were used as metrics to evaluate the features. We present the features in two categories spanning architecture and software optimization. A detailed power modeling exercise was undertaken for evaluating the features, including detailed model correlation with post-Si data from previous generation products. The combined benefit of the features translates to an overall improvement of ~34% SoC power and ~11.5% increase in battery life for suite i.e. ULP product is very close to the target of maintaining the hours of battery life expected by the suite. These features have been adopted by products across several segments.

Keywords: KPI (Key Power Indicators), SoC (System On Chip), Ultra Low Power (ULP), Battery Life (BL), Double Data Rate bandwidth (DDR BW), On Chip Variations (OCV), Mobile Industry Processor Interface (MIPI), embedded Display Port (eDP), Panel Self Refresh-2 (PSR2), High Bit Rate (HBR), Low Power (LP), Dynamic Random Access Memory (DRAM)

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1. Introduction

ULP products aim to provide a responsive user experience across several different use cases such as browsing, gaming and productivity while still striving to meet all day battery life comparable to products in the mobile segment. Battery life is largely determined by the performance of the product across Average Power KPIs introduced in BL suite. These KPIs represent how the product is used in a typical day. Battery Life for a particular use case of a product is defined as given in equation (1). It is the ratio of Battery Size (W.Hr) and Platform Power Consumption (W) for that use case.

$$Battery\ Life\ (Hrs) = \frac{Battery\ Size\ (W.Hr)}{Platform\ Power\ Consumption\ (W)} \quad (1)$$

The above equation holds true when we are estimating battery life for any particular use case. However, in ULP products, as described above, typical usage involves several use cases. In addition to active usage, the product could also be in the idle state for considerable amounts of time. Based on this, we can characterize the power consumption in two categories:

- Active power consumption, when different use cases are being run

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- Idle power consumption, when the SoC is in an idle state

The total power consumption is the time weighted average of the active power consumption and idle power consumption. Hours of Battery Life, on the other hand, is solely based on active use cases during a typical number of hours a day and hence there is no idle part in the calculation. Equation (1) can be modified to arrive at hours of battery life equation for the product, as shown in equation (2).

Use cases	Baseline Target SOC+Memory (W)	Optimized Target SoC + Memory (W)
Web Browsing	1x	0.8x
Productivity	1x	0.7x
Music Streaming	1x	0.2x
Photo Capture	1x	0.8x
Idle Screen On	1x	0.1x
Video Conferencing	1x	0.9x
Video Streaming	1x	0.7x
Video Playback, 30 FPS	1x	0.5x

$$\text{Hrs} = \frac{Battery\ Size\ (W.Hr)}{\sum_{i=1}^{n} KPI\ Weightage_i * \ Power\ Consumption_i(W)} \quad (2)$$

Table 1: BL use cases and targets

Table (1) shows the 20% improved power with optimizations.

The power optimization features pursued in this paper either have a broad impact on all of the KPIs in the BL suite or are targeted at the higher usage KPIs such as web browsing. Examples of features in the first category are display power optimization and the advocacy for low power clocking techniques. As an example of a feature in the second category, the core frequency is tuned to optimize overall SOC power consumption for Web Browsing.

The structure of the rest of the paper is organized as follows: We first present the features proposed, categorizing them into architecture/IP changes or Software changes. The changes are described briefly and their impact on SOC PnP is described. We roll up a conclusion of benefits due to features under each category on a representative use case. In the results section, we present a detailed analysis of the impact of the features on all of the use cases in the BL suite. In the final section, features directed towards further improving battery life are presented

2. Proposed features

In this section, we discuss the features and optimizations improving the battery life. We categorize the changes into two: architectural or IP features and software features. We briefly discuss these features next and show their impact on Web Browsing.

2.1 Architecture or IP Features

In this subsection, we'll briefly discuss the architectural features or IP changes done to get to optimized power. These features are proposed based on the savings they provide as well the need to provide a cost effective product with all the PnP requirements being met.

Command Mode Panel –Switching from video mode panel to command mode panel. The difference between Video mode and Command mode panel is that a Video mode panel has no buffer for local data storage and hence data is fetched from the DRAM every time a display frame requires to be refreshed, independent of the extent of change between the current and previous frame. However, a command mode panel, has its own buffer which enables it to store the data and only fetch from DRAM when any change is there in the contents of the frame. Hence command mode display panels allow for significantly lower active residency and DDR BW in the SoC in comparison to that of a video mode display panel, which allows significant power savings at SoC level.

Clocking Optimization – Redesigning the display clocking subsystem with selectively using jitter sensitive high power PLL for display PHY and using low power PLL for rest of the display subsystem. Also for the IP's which do not need higher frequencies were replaced with low power PLLs, which reduced significant power at SOC level. Opportunistically gating the clock distribution within the subsystem allowed the further power savings at SOC level.

LPDDR5 memory – LPDDR5 introduces a deep sleep mode, which reduces the IDD current by 40% that in turn saves power. Introduction of LPDDR5 instead of LPDDR4x reduced 30% of the Memory Power. Along with this, LPDDR5 can support 6400 MB/s while LPDDR4x can only support 4267 MB/s, a significant memory boost that helps in improving the performance and by reducing the latency.

Lowering of IO voltage – In general IO voltage is a fixed rail for most of the design. However, because of On Chip Variations (OCV), some parts will be faster i.e. can operate at lower voltages. Enabling voltage binning capability on IO rail allows for power savings. By selecting faster parts that have a lower IO voltage, the power on the IO rail is reduced significantly and all BL KPIs benefit.

The savings from these features on the web browsing use case w.r.t. SoC power can be seen in table 2. In the results section, the effect of these features for all KPIs is shown

Table 2. Savings from architecture changes in Web Browsing use case

Web Browsing Use case		
Feature	**Details**	**Savings (%)**
Command Mode Display Panel	Panel Self Refresh as it has internal buffer	10.2%
Clocking Optimization	Low Jitter/ LP PLL	1.3%
Memory Type	LPDDR5 used instead of LPDDR4x	3.7%
IO voltage lowering	To reduce the IO rail voltage	2.1%

2.2 Software Features

In this subsection, we discuss the software optimizations that were pursued.

PSR2 – As mentioned in the previous subsection, command mode display panel has a buffer which can refresh the panel itself without asking any data from the memory if there is no change in the frame. This is called Panel Self Refresh (PSR). However, we can further optimize the power savings and reduce the DDR bandwidth by enabling PSR2. PSR2 is the second level of Panel Self Refresh where we have the information about the exact changes for the frame at a pixel level i.e. the pixels that change their values in a subsequent frame with respect to the current frame (dirty pixels or dirty rectangle) and only fetch the data from the memory for those pixels and not for the entire frame. This allows memory to go into self-refresh faster, saving a lot of power in the display and memory subsystem.

eDP mode power savings – ULP products used only the MIPI PHY for its internal display requirements. Transitioning to combined MIPI and eDP solution provided an opportunity to save power in eDP mode by increasing the driver impedance to reduce the drive strength. This was broadly applicable to all BL use cases. However, the same power saving strategy cannot be implemented with MIPI PHY because it violates the MIPI electrical specification. Further, eDP has HBR (5.4 Gbps per lane) in comparison to MIPI (1.5 Gbps per lane). The higher bitrate ensures only 2 lanes of eDP are sufficient to provide the necessary bandwidth enabling us to gate the other 2 lanes to further save power in eDP mode.

Frequency vs. Residency tuning – Operating the CPU cores at a power efficient point is one of the features proposed to reduce power. In considering power efficiency, it is important to consider not only core power but also the rest of SOC power as dictated by core residency. Hence there is a sweet spot between running the core slow to reduce core power at the expense of higher residency and higher SoC power, v/s running the core faster at a higher power but reducing residency and the related rest of SOC power. In this exercise, maintaining responsive performance sets a lower bound to the Core operating frequencies.

The savings from these changes for the Web Browsing use case w.r.t. SoC power can be seen in table 3.

Table 3. Savings from software changes in Web Browsing

Web Browsing Use case		
Feature	**Details**	**Power Savings**
PSR2	Only dirty rectangles were read	18.9%
HBR2 Implementation	Impedance matching to reduce power	2.4%
Frequency vs Residency Tuning	Fix power optimized frequencies to be used	6.8%

3. Results

In this section, we show the impact of the proposed features for all the BL use cases. First, we discuss the architectural optimizations on all the BL use cases and then we move on to discuss the software optimizations. Note that the features that were taken up had broad impact on the entire BL suite and are not specific to one particular KPI.

Table 4. Savings from the architectural features

BL Use cases	Command Mode	Clocking optimizations	LP5	lowering IO voltage	Total
Web Browsing	10.2%	1.3%	3.7 %	2.1%	16.2 %
Productivity	14.0%	1.2%	2.9 %	1.6%	19.4 %
Music Streaming	0.0%	1.0%	0.0 %	1.0%	-1.9 %
Photo Capture	0.0%	1.0%	5.3 %	2.8%	8.0 %
Idle Screen On	67.2%	0.0%	0.7 %	0.0%	66.2 %
Video Conferencing	0.0%	1.2%	5.7 %	3.3%	8.9 %
Video Streaming	15.9%	1.4%	3.7 %	2.3%	21.9 %
Video Playback	15.6%	1.3%	3.1 %	2.0%	21.3 %

30 FPS					

Table 4 presents the power savings from the architectural or IP optimizations for the BL suite with respect to the n-1 SoC power for the respective KPIs. Command mode doesn't help for music streaming, Photo Capture and video conferencing use cases as the refresh rate assumed in these use cases in 60 fps and music streaming is a no display use case. Idle display has refresh rate of 1 fps which sees the highest benefit.

In table 5, we present the software optimizations discussed in the above sections for the BL suite. PSR2 gives higher benefit in Web Browsing and Productivity use cases w.r.t. other use cases because in these 2 KPIs the refresh rate is dependent on the speed of scrolling the webpage which is very low while video streaming and Video Playback assume 30 fps of refresh rate.

Table 5. Savings from the software optimizations

BL Use cases	PSR2	eDP Mode	Total Savings
Web Browsing	18.9%	2.4%	21.7%
Productivity	19.4%	1.0%	20.9%
Music Streaming	0.0%	0.0%	1.0%
Photo Capture	0.0%	0.5%	1.0%
Idle Screen On	3.4%	0.0%	3.4%
Video Conferencing	0.0%	1.4%	1.4%
Video Streaming	4.1%	0.7%	5.0%
Video Playback 30 FPS	5.4%	0.9%	6.3%

4. Conclusion

This paper presented the optimization techniques done for ULP SoC to achieve the lowest power possible with the minimum set of changes. Only the features that impacts the whole BL suite or the highest weighted KPIs were picked. The features selected spanned the entire SoC and reduce the power across several IPs. These optimizations are crucial to meeting the aggressive goals. Idle Display Screen ON KPI see the most amount of benefit (~70%). Less benefits in use cases such as Photo Capture and Video conferencing are observed because of high refresh rate. Overall BL has improved by ~11.5% in comparison to baseline targets and is now moving towards meeting the desired target of having certain hours of battery life. This paper emphasises on improvising battery life with various minimal techniques like architectural changes, SW optimizations which allows faster time to market with better battery life.

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