# Subthreshold Energy Harvesters Circuits for Biomedical Implants Applications

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## ABSTRACT
This paper reviews the state-of-art of the subthreshold level design energy harvesters for powering biomedical implants. Power consumption and lifespan are crucial requirements for the electronic circuitry of implantable systems. In order to meet these challenging requirements, a design for an energy harvester that operates in a subthreshold level offers a promising solution.

## Categories and Subject Descriptors
B.7.1 [Integrated Circuits] advance technologies, VLSI, simulation

## General Terms
Design, theory, documentation, simulation

## Keywords
Biomedical applications, energy harvesting, implantable devices, low power, subthreshold design

## 1. INTRODUCTION
Implantable medical devices are essential because of their direct impact on human lives, health and safety. The concept of energy harvesting from the human body for implant devices has gained a new relevance. As mentioned in [1], the energy harvesting technology enables monitoring of patients who are outside the clinical environment. To address the social needs of the increasing population of aging people with chronic long term health conditions and ensure their safety, recent research aims to develop technologies with low power requirements, higher energy efficiency, improved power management and improved sensor technology that will be able to monitor vital signs, communicate wirelessly, and will be implantable, biocompatible and self-powering. Therefore, it is important to use an implantable human energy harvester, as this would be an efficient alternative source of energy to continuously supply power to implant devices [2]. Since available power is a critical requirement for implantable devices to increase their lifespan, recent research on biomedical implants microsystems has focused on continued down scaling of electronic circuitry to achieve ultra-low power consumption [3]. Due to its ultra-low power consumption and high energy efficiency subthreshold level design has gained interest in the area of low lower design circuits, such as for biomedical implants. Subthreshold design enables wide-range dynamic voltage scaling by allowing circuits to operate in near/subthreshold voltages. Design requirements for implantable circuits include a minimal footprint or the surface area size of the integrated circuit implants and circuit operation must be at a very low power. In order to achieve the low power operation, subthreshold level operation of MOSFETS offers a promising solution.

This paper views self-powered biomedical implants from a systems perspective by reviewing both the energy created by the harvesting subsystem and the power needed by implant's electronics.

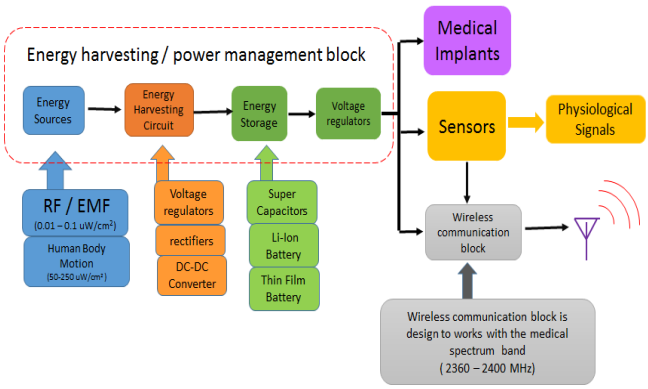


**Fig. 1: Block diagram of Energy Harvesting subsystem**

## 2. ENERGY HARVESTING SUBSYSTEM
An energy harvesting subsystem as depicted in Fig.1 is designed to harvest energy from the human body, Radio frequency and electromagnetic fields can provide source regulated voltages to the rest of the sub-circuits. The human body itself is also a potential source of energy. These source can be harvested in particular from the kinetic and thermal energies of the human-body [4].

Ambient radio frequency energy is a free flowing energy that can be collected and converted to dc power. It is an attractive approach due to its potential to provide power indefinitely. [5] For short ranges it is possible to harvest small amounts of energy from a typical WiFi transmitting power level of 50 to 100mW.

The power management block includes the front end harvesting circuit that is able to convert energy either in AC or DC to a regulated DC output. An energy storage super capacitor

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and voltage regulators need to be designed to meet the specific voltage required by an implant sub-circuits.

Table 1 reports average values of power required to supply some implantable medical devices [4]. As depicted in the table the power consumption is in the range of 8uW to 5mW. Table 2 depicts amounts of kinetic energy from body motion and the expected generated electrical energy. [6]

If harvest energy levels are realized as shown in Table 2, in the range of, 6.9mW to 1000mW for mechanical energy and 1.2mW to 170mW in its equivalent electrical energy, then it is possible to meet the required power consumption of the implantable devices in Table 1. With this, designing an in-body harvester is possible and it will extend the lifespan to the implant device.

Since several types of implants devices perform real-time monitoring of physiological signals, to be able to communicate wirelessly opens the possibility to perform at-home monitoring [7]. Wireless powering and communication has the advantage of reducing the size, complexity and power consumption of implantable devices without sacrificing robustness and functionalities. [8]

**Table 1. Power consumption of different implantable medical devices. [4]**

| Implantable Device | Power consumption |
|---|---|
| Cochlear | 5.16mW |
| Drug Pump | 400uW |
| Neuro-stimulator | 50uW |
| Muscle stimulator | 1.3mW |
| Pacemaker | 8uW |

**Table 2. Kinetic Energy from Body Motion and the expected generated electrical energy. [6]**

| activity | Mechanical | Electrical | Electrical energy per movement |
|---|---|---|---|
| Blood flow | 930mW | 160mW | 0.16J |
| Exhalation | 1000mW | 170mW | 1.02J |
| Breath | 830mW | 140mW | 0.84J |
| Fingers type | 6.9-19mW | 1.2-3.2mW | 226-406uJ |

## 3. SUBTHRESHOLD LEVEL DESIGN

Improvements in semiconductor technology in developing a low-cost, very low-power and energy efficient system designs have been the foundation in making information technology ubiquitous today. Scaling down the design size and power consumption of electronic equipment has recently encouraged researchers to find alternative ways to design it in a near/sub threshold level.

Subthreshold level operation is designed to have a supply voltage that is less than the typical threshold of the transistor. Operating at this modified supply voltage limits the performance of the system, but it is still acceptable given its substantial advantage in energy efficiency.

In order to achieve high performance, transistor sizes are aggressively scaling down, this increases the subthreshold leakage current, gate leakage, and reverse-biased source substrate and drain-substrate junction band to band tunnelling (BTBT) current increases. [9]

As shown in the Fig. 2, dynamic voltage dominates with higher power supply voltages in many of today's circuit designs. Note that leakage energy occurs when the circuit is not changing operational states, while the dynamic energy occurs in the circuit's switching mode, as the internal nodes are charging and it varies as the square of the supply voltage. Power is related to the supply voltage, reducing the voltage results in the reduction of power and energy consumption of the system. Fig. 2 also illustrates the region of operation for near/subthreshold design.

The tendency to reduce energy consumption at a cost of lower speed is suited for energy constrained applications such as wearable devices, implantable devices, and energy scavenging applications where lifespan extended and lower power consumption is the primary concern. Therefore, subthreshold level circuit designs offer promising solutions.

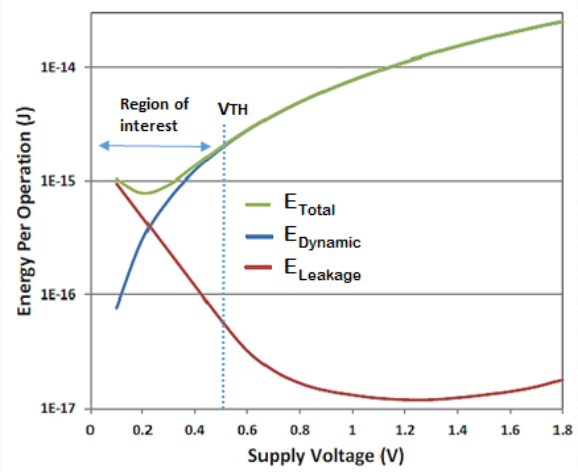


**Fig. 2 Energy as a function of supply voltage**

As the process technology continues to scale down, decreasing the supply voltage result an increase in subthreshold leakage current, as depicted in fig. 2. Thus, many of today's research is working on developing a circuit techniques to reduce the subthreshold leakage current in both dynamic and static mode in order to minimize the total power consumption of the system.

The expression for the total energy is given below;

$$E_{Total} = E_{Dynamic} + E_{Leakage} \quad (1)$$

$$= \propto \cdot n \cdot E_{switch,inv} + P_{Leak} \cdot t_d \quad (2)$$

$$= \propto \cdot n \cdot \left(\frac{1}{2} \cdot C_s \cdot V_{dd}\right) + (n \cdot V_{dd} \cdot I_{Leak}) \cdot (n.t_p) \quad (3)$$

where n is the number of stages, $E_{switch,inv}$ is the switching energy of a single inductor, $P_{Leak}$ is the total leakage power of the entire inverter chain, $t_d$ is the delay of the inverster chain, Cs is the total switched capacitance of a single inverter, $I_{Leak}$ is the leakage current of the single inverter and $t_p$ is the delay of a single inverter.

Fig. 3-4, show the distribution of power consumption levels of some of the reported subthreshold designs in mW (Fig. 3) and µW (Fig.4) respectively, against the year of publication. In there we can see a considerable scatter. The dotted red line shows a linear forecast of the trend over the years. As the process technology is scaling down, the power requirement is also shrinking down, thus, designing a low-power, low energy and more efficient circuit can be made possible, using subthreshold techniques.

Previous research has shown that optimizing process technology for subthreshold level operation can improve IC energy efficiency. However, for higher operating frequencies, devices need to be redesigned and optimized, as operating in the strong inversion region may not produces optimum results in the subthreshold region. Thus, there is much future research work to be done in the area of subthreshold architecture design. [9]

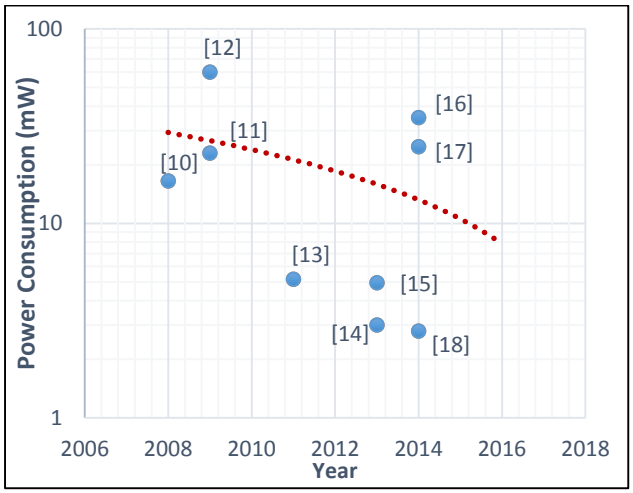


**Fig. 3. Comparison and linear forecast of power consumption (mW) of some subthreshold designs presented in literature [10] – [18]**

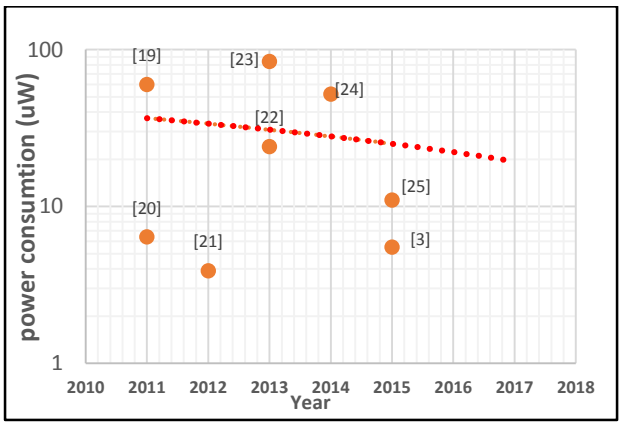


**Fig.4 Comparison and Linear forecast from power consumption (µW) of some subthreshold designs presented in literature [3], [19] – [25].**

## 4. RELATED STUDIES

In paper [26] by B.Zhai, et al, they presented the energy optimization for sensor processor and that subthreshold-voltage design offers an energy-efficient sensor network. They proposed a subliminal processor that is fully functional from a nominal supply voltage of 1.2 down scaled to 200mV. The processor attains maximum efficiency of 2.6pJ/instruction at 360mV with operating frequency of 8.33 kHz and concluded that tunning of the operating frequency is also an important factor aside from tuning the input voltage.

A.Yakovlev, J.Hoon et.al, [27] demonstrated a wirelessly powered transceiver design for implantable devices through a porcine heart tissue with the total power consumption of 10.7µW. The prototype consist of a rectifier, regulator, demodulator, modulator, controller and sensor interface. The forward link achieves 4 to 20 Mbps with 0.3pJ/Bit at 4Mbps and the backlink is 2 Mbps at 0.7 pJ/bit.

In [28], P.J Grossman, et,al. used a simulated-based approach to demonstrate the benefit of subthreshold-optimized transistor for logic gates to reduce the energy of the design circuit and achieved 57% percent energy efficiency improvement. Summary of the significant output from related studies id shown in table 3.

**Table 3. Summary of the significant output form related studies.**

| Ref. | parameter | Efficiency |
|---|---|---|
| [26] | Vsub = 360mV | 2.6pJ /instruction |
| [27] | Power = 10.7µW | Uplink = 0.3pJ/bit<br>Downlink = 0.7pJ/bit |
| [28] | Vin = 0.3 to 0.6V | 57% efficiency improvement |

## 5. SUBTHRESHOLD MOSFET CHARCTERISTICS

Subthreshold voltage characteristics of MOSFET devices can be harnessed and utilized in the nano power region, allowing a wide possibility of using repeatable circuits through redesigning in a subthreshold level. An energy harvesting circuit, for example, which is of interest in today's field of research and innovation, sees the potential of subthreshold level design for nano power operation.

The expression for Subthreshold leakage current is given below;

$$I_{DS} = K \cdot e^{(Vgs-Vth)\cdot\frac{q}{nkT}} \cdot \left(1 - e^{-Vds\cdot\frac{q}{kT}}\right) \quad (4)$$

where k: function of technology, $V_{GS}$: gate-to-source voltage, $V_{DS}$: drain-to-source voltage, $V_{th}$: threshold voltage, q: electron charge, k: Boltzman constant, T: temperature, n: nonlinearity constant 1~2, (kT/q = 0.0259).

Considering the behavioural characteristics of the MOSFET in the subthreshold region for analog applications. Fig. 5 illustrates the $I_{ds}$ vs. $V_{gs}$ characteristic curve of NMOS and the region of operation for the subthreshold operation. The region at the condition where $V_{gs} < V_{th}$ is said to be that the device is cut off, and no current flows or current is said to be wasted. However, when the MOSFET is switched off, there is still power behind the gate below the threshold, and so the gate is not really completely off in most cases. It is found out that for values of $V_{gs}$ smaller than but close to Vth, a small drain current flows to the device. In this subthreshold region the operation of the drain current is exponentially related to $V_{gs}$.

In subthreshold conduction, the transition from the ON state to the OFF state is gradual. This can be seen more clearly when Ids is plotted on a logarithmic scale as shown in Fig. 5, where $I_d$ is expressed as;

$$I_d = \exp\left(\frac{q\,Vgs}{nkT}\right) \quad (5)$$

This is generally the channel-source pn junction current. Some electrons diffuse from the source into the channel when this pn junction is forward biased.

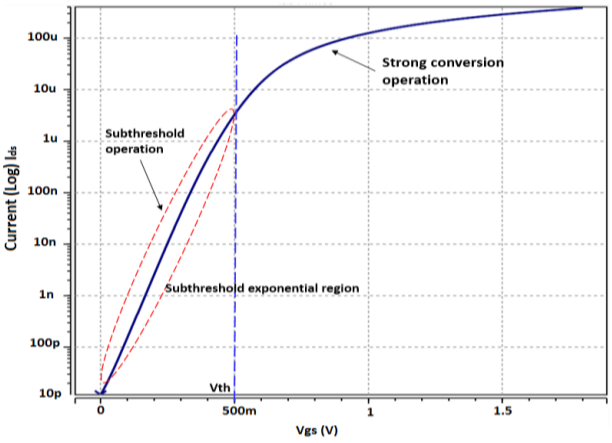


Fig. 5. $I_{ds}$ vs. $V_{gs}$ Characteristic Curve

The possibility to reduce the energy consumption at the cost of lower speed offers a solution to the following application in which the subthreshold level design is applicable. For energy constrained applications such as medical devices (like pace-maker, cochlear implants, wearable computing implants), wireless sensors, and energy harvesting circuits in which lower power consumption and extended battery lifetime is of concern, subthreshold circuits may be a good alternative. [9]

Fig. 6 illustrates the Ids vs, $V_{ds}$ subthreshold output characteristics curve of nmos with varying $V_{gs}$ from 0.2 to 0.5.

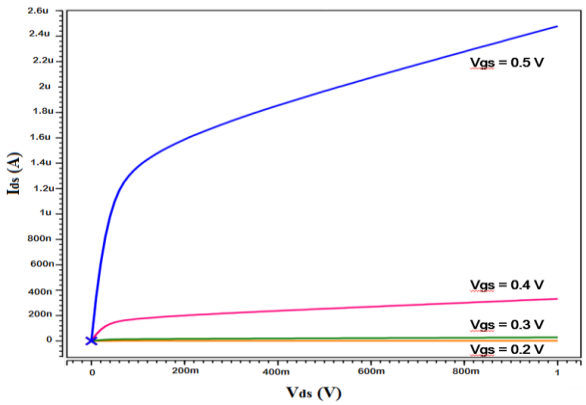


**Fig. 6 Ids vs. Vds output characteristic curve varying Vgs**

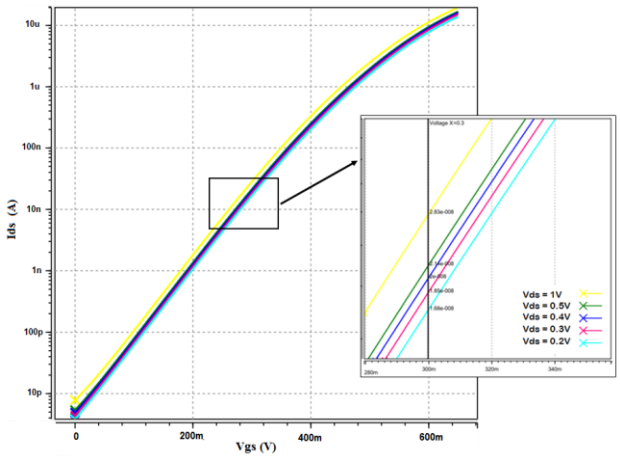


**Fig. 7. Ids vs Vgs characteristic curve varying Vds**

**Table:2. Summary of Ids vs Vgs Value at Vgs=300mV**

| @Vgs= 300mV | |
|---|---|
| Vds = 1V | Ids = 28.3nA |
| Vds = 0.5V | Ids = 21.4nA |
| Vds = 0.4V | Ids = 2nA |
| Vds = 0.3V | Ids =18.5nA |
| Vds = 0.2V | Ids = 16.8nA |

**Table:3. Summary of Ids vs Vds Value at Vds=400mV**

| subthreshold region: Vgs < Vth ; Vth = 530mV @Vds = 400mV | |
|---|---|
| $V_{gs}$ = 600mV | $I_{ds}$ = 8.88uA |
| $V_{gs}$ = 500mV | $I_{ds}$ = 1.82uA |
| $V_{gs}$ = 400mV | $I_{ds}$ = 239nA |
| $V_{gs}$ = 300mV | $I_{ds}$ = 20.4nA |
| $V_{gs}$ = 200mV | $I_{ds}$ = 1.29nA |
| $V_{gs}$ = 100mV | $I_{ds}$ = 78pA |

Fig. 7 shows the subthreshold current as a function of the sun-threshold voltage, for 0.18 CMOS technology. The typical value of $V_{th}$ is 530mV. When $V_{gs}$ is equal to 500mV the current Ids is equal to 1.82µA; when the value of $V_{gs}$ is equal to 400mV, the current Ids decreases to 239nA. A further reduction of $V_{gs}$ to 300mV drops the current Ids by another order of magnitude to about 20.4n; and when $V_{gs}$ is equal to 200mV, Ids is equal to 1.29nA. This shows that when $V_{gs}$ is less the $V_{th}$ there is still a current flowing through the device. A subthreshold level design will utilize this amount of current available in order to reduce the power consumption. The subthreshold voltage may vary from 200mV to 500mV, a drop of 100mV in the input voltage causes a drop of 1000 times in the drain of the source current Ids. Thus, it is important to have a precise control in the gate threshold and subthreshold voltage level in the circuit. Table 2 shows the summary of $I_{ds}$ vs. $V_{gs}$ when $V_{gs}$ is set to 300mV and table 3 shows a summary of $I_{ds}$ vs $V_{ds}$ is at 400mV

The subthreshold slope factor or the subthreshold swing is defined to be the inverse slope of the log ($I_d$) vs. $V_{gs}$ a characteristic in the sub threshold region, which is usually give as:

$$S_s = \ln(10)\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \qquad (6)$$

where, $C_d$ is the depletion layer capacitance, Cox is the gate oxide capacitance, and kT/q is the thermal energy divided by the elementary charge.

## 6. CONCLUSION

Energy harvesting subsystems offer an alternative approach to supply power to implantable biomedical devices with the scaling of the process technology that reduces the chip area and improves performance. This also offers an opportunity to develop electronic circuitry that is low-power, low-voltage and has a reduced power consumption, through redesigning and optimization of the circuits in the subthreshold level.

Subthreshold design offers a promising solution in the semiconductor road map in developing a very low-power consumption energy harvester that is suited to biomedical implant applications.

Based on trends in both energy harvesting and subthreshold design, it is reasonable to conclude that a cross-over point will occur in the next five years. This will create an opportunity, from a systems perspective, of a self-powered implantable device.

The ability to operate in the subthreshold region is imperative for unlocking the benefit of nano power devices and driving the innovation in energy harvesting and other fields.

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