Optimum Design of 2.4GHz Low Noise Amplifier (LNA)

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Abstract. A 2.4 GHz Low Noise Amplifier (LNA) design, optimization and simulation is presented in this paper. The optimization tool available in ADS software is employed to obtain minimum noise figure (NF) and minimum power consumption for an inductive source degeneration LNA topology. A comparison between this approach and another available analytical method is performed and found a significant improvement in noise figure (optimized NF=0.823), and in power consumption (optimized value =8.6 mW).

Keywords: LNA, ADS, NF, RFIC.

1 Introduction

Radio-frequency ICs (RFICs) are widely used in wireless communication systems. RFICs are analogue circuits that usually operate in the frequency range from 3 kHz to 2.4 GHz. LNAs are used in RF receivers' front-end to amplify weak signals from receiving antennas to an appropriate level with minimum noise. Therefore, both the gain and noise figure are important factors that have to be considered and optimized in LNA design [1].

In the design of LNA, it is necessary to make a trade-off between power consumption, noise figure, gain, input match and output match at any stage [2]. The performance parameters are varied according to condition bias. It is always serviceable for the LNA designer to have knowledge of suitable bias points for the several stages, depending on the requirements. A designer might also be interested in giving priorities to the parameters which they think are more important than others. Trade-offs between the performance parameters of an LNA can be done analytically or by optimization techniques. Optimization methods are used because of many reasons such as the design task of a high-performance circuit which is tedious, where analytical methods are being difficult [3].

In this paper, both analytical methods and optimization tools are used for the design of LNA and are compared as shown in Figure 1. The optimization tool available in the Advance Design System (ADS) is employed. A comparison between these two methods is presented to illustrate the advantage of using optimization in improving LNA performances.

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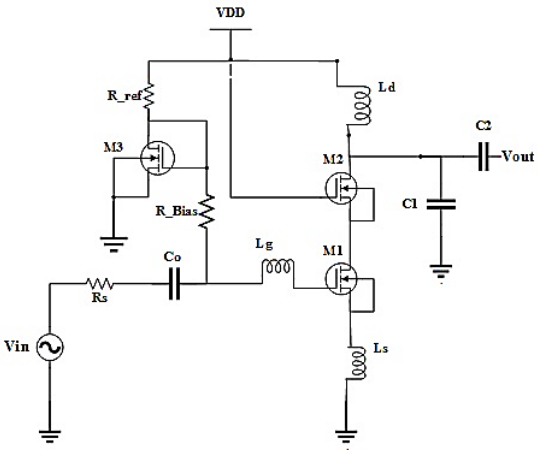

Fig. 1. Single-Ended LNA

2 LNA Design

2.1 The topology of low noise amplifier

Usually, the first stage in the receiver side is LNA, since, the operating frequency of the low noise amplifier is in a radio frequency band, and the minimization of the complexity for the circuit should be taken into account. The parasitic effects may distort the amplified signal in case the circuit is complicated. In addition to that, the LANs single-ended narrowband low power, low voltage design, have more than one topology, these topologies may include common gate, resistive termination common source, inductive degeneration common source, shunt series feedback common source, and cascode inductor source degeneration [2].

A proper topology should be selected to meet the required isolation between the input and output, high gain, low noise figure, and low power consumption. In this paper, the cascode inductive source degeneration topology has been chosen to investigate the proposed design technique.

2.2 Single-Ended LNA design (cascode inductive source degeneration)

A Single-Ended LNA is shown in figure 1, the circuit structure utilizes the inductor (L_S) that is connected to the transistor M_1 at the source (inductive source degeneration) [4]. The advantage of this structure is that the designer has flexible control over the value of the real part of the input impedance by choosing the proper inductance. Moreover, to reduce the interaction between the tuned output and the tuned input, the cascading transistor M_2 is used. The biasing circuit is realized by transistor M_1 and M_3 that form a current mirror. M_3 is selected to obtain minimum power overhead for the biasing circuit.

The reason for using the inductor L_d is to resonate with the output load to obtain maximum output power transfer. Moreover, a trade-off between the common source gain and increasing the parasitic capacitance of the transistor number 2 (M_2) is done by designing W_2 wider. Also, the transistor M_2 helps to reduce the Miller effect (C_{gd1}) as well as S_{21} [4]. The equivalent current

noise resulting from the R_{bias} can be ignored by choosing the value of this resistance large enough.

3 Case study

3.1 Analytical design of a 2.4GHz, 0.18 um technology LNA with inductive source degeneration

The design of an LNA must meet the specified performance requirements of the most important component values. These performances may include transistor widths W_1, W_2 and W_3, inductor values L_S, L_g, L_d, coupling capacitance C_o, C_1 and biasing current I_d. The single-ended low noise amplifier has the input resistance [5], [6], [7].

$$R_{in} = R_g + \frac{L_s \times g_{m1}}{C_{gs1}} + j(W \times L_s - \frac{1}{W \times C_{gs1}}). \quad (1)$$

It can be written as:

$$R_{in} = R_g + R_a + j(XL_s - XC_{gs1}) . \quad (2)$$

Where:

$$R_a = \frac{L_s \times g_{m1}}{C_{gs1}} . \quad (3)$$

Then, the resistance of the MOSFET with no feedback will be:

$$R_{in} = R_g - jXC_{gs1} \quad \rightarrow R_{in} = jXC_{gs1} . \quad (4)$$

As there is series reactance feedback, X_{LS} will be added to the original input impedance. Also, the inductor L_g designs and connects in series with the gate to cancel out C_{gs} at the resonant frequency. The input resistance can be written as $R_{in} = \frac{L_s \times g_{m1}}{C_{gs1}}$. The values of g_m and C_{gs} are calculated to give the required R_{in} after selecting the L_S value. The summary of designing the low noise amplifier steps is given below [7], [8]:

Step1. The optimum device width of transistor M_1 and M_2 are determined

$$W_1 = \frac{3}{2 \times C_{OX} \times L_1 \times Q_{opt} \times R_S \times W_o}$$

W_1=W_2= 370 um, L_1 = L_2= 0.18 um

Step2. The gate to source capacitance Cgs of M_1 is

$$C_{gs1} = \frac{2}{3 \times C_{OX} \times W_1 \times L_1} = 0.34 \text{ pF}$$

Step3. The device transconductance (g_{m1})

$$g_{m1} = \sqrt{2 \times \mu_n \times C_{OX} \times (\frac{W_1}{L_1}) \times I_d} = 85 \text{ mA /V}$$

Step4. The transistor unity gain frequency (W_T)

$$W_T = \frac{gm_1}{Cgs_1} = 250\ Grps$$

Step5. The inductor value ($L_{S)}$ that connect in the source is given by

$L_S = \frac{R_S}{W_T}$, Where R_S is the input resistance 50 Ω
Then the value of the inductance L_S is 0.2nH

Step6. The value of L_g

$$L_g = \frac{1}{W_o{}^2 \times C_{gs1}} - L_S = 12.7 \text{ nH}$$

Step7. The value of drain inductance is

$L_d = \frac{1}{W_o{}^2 \times C_L} = 4.4$ nH , where C_L = 1 pF

Step8. To obtain minimum power consumption the width and the length of M_3 is selected to be:
W_3 = 30 um, L_3 = 0.18 um

Step9. The bias resistor value R_{bias} = 3KΩ, R_{erf} = 2KΩ

Step10. The power dissipation $P_D = V_{dd} \times I_{d1}$=12.36 mW

Step11. The minimum noise figure "F_{Min}" is calculated based on the equation

$$F_{Min} = 1 + 1.62 \times \frac{W_o}{W_T} = 1.23 \text{ dB}$$

4 Optimum design of a 2.4GHz LNA with inductive source degeneration

The procedure in the design of LNA is the determination of minimum power consumption and minimum noise figure. An optimization technique is employed to meet these criteria and to guarantee optimized noise figure and power consumption for a specified fixed design scattering parameters S_{11}, S_{22}, S_{21}, and S_{12}.
The Advance Design System (ADS) RF simulator includes an optimization tool used to get optimum design parameters of multi-objective optimization of inductive source degeneration LNA. Figure 2 presents a proposed flow chart representing the optimization procedures that are employed for minimization of consumed power required and also to minimize noise figure.

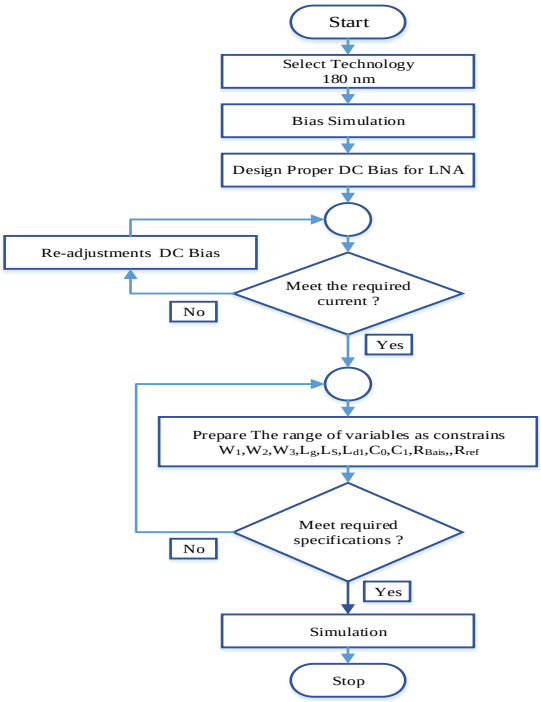

Fig. 2. Flow chart for design optimization of LNA

5 Design objectives and constraint optimizations of LNA inductive source degeneration

Dependent on the previous studies of Low Noise Amplifier, the design target for both the analytical method and optimization method of LNA is specified in Table 1.

Table 1. The target of LNA specifications design.

Topology	Single-ended LNA
Technology	CMOS 0.18 µm
Frequency	2.4 GHz
Noise Figure (NF)	< 3 dB
Current (I_{d1})	< 8 mA
The power gain (S_{21})	> 10 dB
Output return loss (S_{22})	< -10 dB
Input return loss(S_{11})	< -10 dB
Revers isolation(S_{12})	< -10 dB
Power consumption(P_D)	< 15 mW
Source/load impedance(Z_i/Z_o)	50 Ω

6 Design constraints

Design component values of LNA under study have been determined as constraints. These values have been selected by using the available literature as a starting point. These parameters may include (Lg, Ld, Ls, W_1, W_2, W_3). Table 2 presents the constrained values desired.

Table 2. Design variables constraints.

Variables as constraints	Value
W_1	50 To 700 um
W_2	50 To 700 um
W_3	10 To 100 um
L_g	1 To 10 nH
L_S	0.05 To 5nH
L_d	0.05 To 5 nH
I_{d1}	1 To 10 mA
C_0	0.1 To10 pF
C_1	0.1 To 10 pF
C_2	0.1 To 10 pF
R_{bias}	1000 To 6000 Ω
R_{ref}	1000 To 6000 Ω

The employing of an optimization technique using ADS simulator provides optimal values for the component realizing LNA and listed in Table 3.

Table 3. Optimal variables value of proposed LNA.

Variables as constraints	Value
W_1	220 um
W_2	400 um
W_3	20 um
L_g	5.5 nH
L_S	0.85 nH
L_d	2 nH
I_{d1}	4.5 mA
C_0	0.5 pF
C_1	1 pF
C_2	5.3 pF
R_{bias}	4 KΩ
R_{ref}	3 KΩ

7 Comparison between analytical method and optimization technique of Advance Design System (ADS)

The optimization algorithm available in the ADS simulator is developed to deal with the design under consideration with specified optimization goals (multi-objective functions) containing power consumption and noise figure. However, the performances and other design specifications are used as constraints in the optimization algorithm.

Table 4 shows a comparison between the optimization algorithm method used in the ADS simulator and the analytical method based on design equations [5] at frequency 2.4GHz. It can be shown from this table that a significant improvement is obtained by using the optimization technique.

Table 4. Comparison variables value of LNA between the optimization method and analytical equations.

Components	Optimization method	Analytical method
W_1	220 um	370 um
W_2	400 um	370 um
W_3	20 um	30 um
L_S	0.85 nH	0.2 nH
L_g	5.5 nH	12.7 nH
L_d	2 nH	4.4 nH
C_2	0.5 pF	1 pF
C_1	1 pF	1 pF
C_0	5.3 pF	10 pF
R_{ref}	3 KΩ	2 KΩ
R_{bais}	4 KΩ	3 KΩ
All Lengths 0.18um	0.18um	0.18um

Table 5 presents a comparison between optimization techniques and the analytical method for LNA designed in the CMOS 0.18 process. It can be seen from this table the improvement of the design parameters compared with the required specifications listed in this table.

Table 5. Comparison between optimization technique and the analytical method.

Topology	Performance requirements	Optimization method	Analytical method
Technology	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm
Frequency	2.4 GHz	2.4 GHz	2.4 GHz
Noise Figure(dB)	< 3	0.823	1.16
Current (I_{d1})	< 8 mA	4.5 mA	6 mA
The power gain (S_{21})	> 10	18.6	8
Output return loss (S_{22})	< -10	-10	-2.5
Input return loss(S_{11})	< -10	-20	-2.6
Revers isolation(S_{12})	< -10	-21.7	-29
Power consumption(mW)	< 15	8.6	12.36
Source/load impedance(Z_i/Z_o)	50 Ω	50 Ω	50 Ω

8 Comparison between the optimization technique of ADS and other existing literature

A comparison is accomplished between optimization and other analytical methods [9], [10] shown in Table 6. It can be seen that the improvement in the design using optimization comparing with the references is obtained [9], [10].
From the comparison in Table 6 shown, the proposed 0.18um of Single-ended LNA (cascode inductive source degeneration), has low noise figure (NF), low power consumption and high power gain as compared to [9], [10] LNA.

Table 6. Comparison between the results of this work and other design techniques [9], [10] of LNA.

Parameters	[9]	[10]	[11]	Proposed Work
Technology	0.25um	0.18um	0.090um	0.18um
Supply Voltage	3.3V	1.8	1.5	1.8V
Frequency (GHz)	2.4	2.4	2.4	2.4
S_{21}(dB)	21.63	4.5	20	18.6
S_{11}(dB)	-13.4	-15.6	-24	-20
S_{22}(dB)	-18.3	-23.4	-22	-10
S_{12}(dB)	NA	-13	NA	-21.7
Noise Figure (dB)	1.8	2.77	1.3	0.823
Power Consumption (mW)	12.5	18	15	8.6

9 Design simulation

The proposed circuit design is optimized and simulated using an ADS simulator in the 0.18um CMOS process. From Figures 3 to 7, it can be seen that the algorithm design satisfied the performances and the required specifications for LNA. The forward power gain (S_{21}) is 18.6 dB at 2.4 GHz that shown in Figure 3. Figure 4 shows low noise figure (NF) of 0.823 is achieved at 2.4 GHz. The S-parameters (S_{11}, S_{22}) of the LNA are illustrated in Figure 5 and Figure 6 respectively. The S_{11} shows a good input match of -20dB. Moreover, the value of S_{22} shows a good output match which achieves -10dB. As shown in Figure 7, the S_{12} is -21.7dB at 2.4GHz.

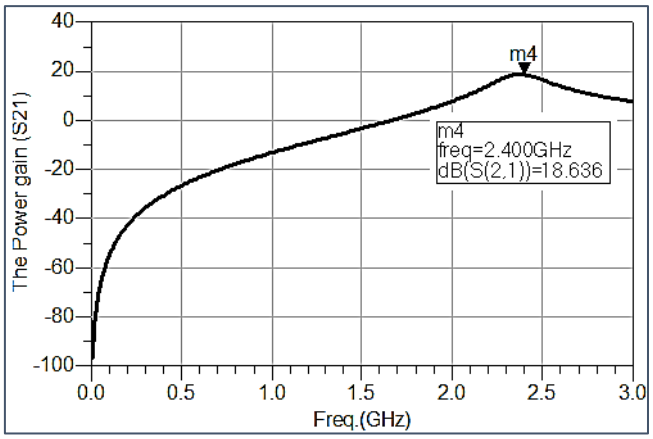

Fig. 3. The power gain (S_{21}).

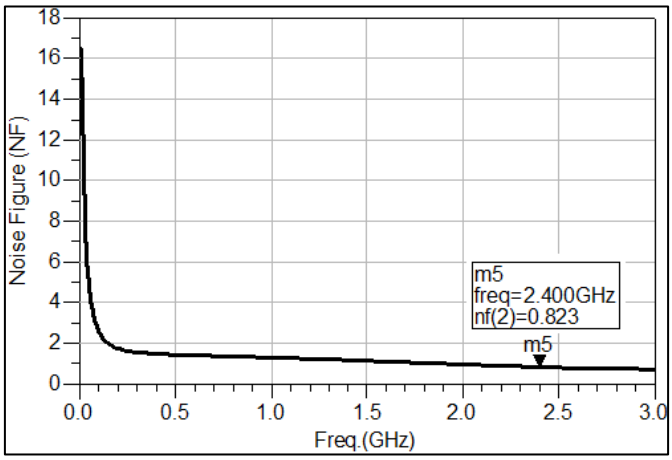

Fig. 4. The noise figure (NF).

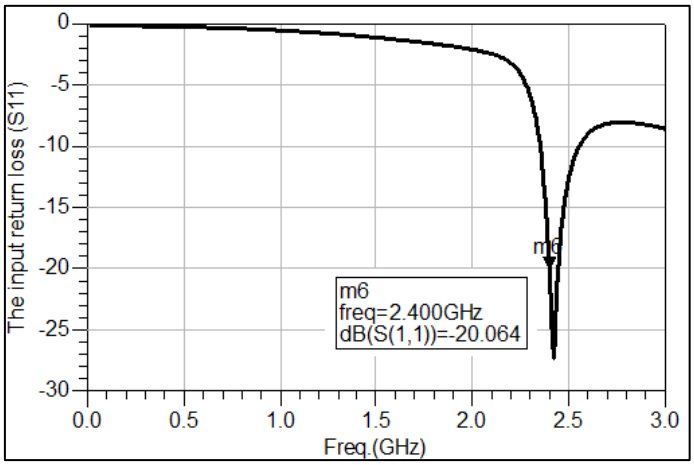

Fig. 5. The input return loss (S_{11}).

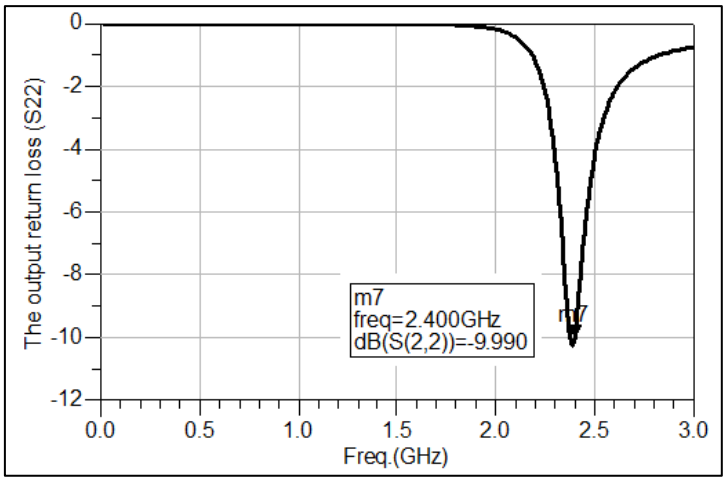

Fig. 6. The output return loss (S_{22}).

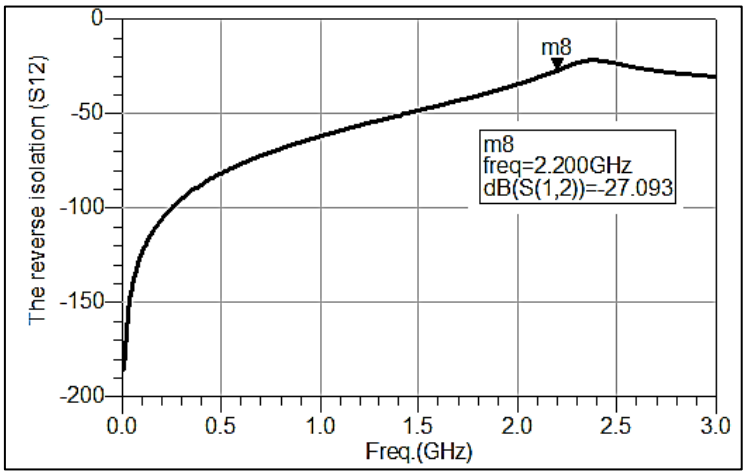

Fig. 7. The reverse isolation (S_{12}).

10 Conclusions

This paper illustrates the application of optimization algorithms that exist in ADS RF simulator as an optimization method for the design of 2.4GHz LNA. Inductive source degeneration topology was used to obtain a minimum noise figure and minimum power consumption. An ADS RF simulator based on optimization algorithms has been used for analysis and satisfied the design specifications. A comparison of this work is done with an available analytical method and other existing technology. It was shown, the resultant noise figure and power consumption obtained by applying optimization technique are minimized.

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