Design and Analysis of Master Slave Flip Flop with Low Power, Reduced Delay and Area Efficiency

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Abstract. This research introduces a power-efficient master-slave flip-flop utilizing clock gating techniques, designed and analyzed using Xilinx Vivado. The proposed approach minimizes dynamic power consumption by selectively deactivating the clock signal when the flip-flop is idle. Clock gating is utilized in Verilog HDL implementation, to avoid unnecessary transitions. The simulation results show a significant reduction in dynamic power (0.001 W) and better-worst negative slack (WNS) of 0.237 ns. With the use of only two slice registers and two slice LUTs this design maintains a good timing performance preserving optimal resource usage. These results demonstrate the efficiency of clock gating in power reduction for FPGA-based sequential logic circuits.

Keywords: Low-Power Design, Master-Slave Flip-Flop, Clock Gating, Dynamic Power Reduction, Sequential Logic.

1 Introduction

A recent evolution of flip-flop design has generated topologies to maximize the use of area, reduce the device delay and increase power efficiency. Low Power Low Complexity High Latency Flip-Flops was proposed by D. Srinivas et al. [1] as a way to reach a low power consumption combined to simple topology at the expense of bigger latency. A Clock gated Flip-Flop was proposed by Priyadarshini et al. [2] that applied clock and power gating methods to significantly reduce dynamic power consumption. However, this came at the expense of increased space overhead because of the added gating circuitry. By integrating pass transistor and transmission gate logic, Rajesh Krishna and Rohit Lorenzo [3] created a Modified Hybrid Flip-Flop that boosted speed and power efficiency at the expense of a little more design complexity. Balaji, G. Naveen et al. Using a transmission gate, [4] created a master-slave flip-flop that maximizes clock-to-Q latency and signal integrity, but it has greater power consumption and requires more space. Using cross-latch sequential logic, Po-Yu Kuo et al. [5] introduced a Cross-Latch Shift Register Scheme that improves power efficiency in shift register applications while slightly increasing latency. The selection of appropriate architectures for low-power and high-speed applications is guided by these studies, which emphasize the trade-offs in power, latency, and area efficiency among various flip-flop designs.

Clock gating is a well-known approach to reduce dynamic power consumption in digital circuits. Clock gating eliminates unnecessary clock switching and saves power without sacrificing function by only turning off the clock supply to the circuit when the circuit does not need to operate. Even if we can run the design well with this method, clock gating in FPGA-

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based designs requires careful examination of resource utilization and timing to ensure that we achieve an optimal speed up.

This makes it suitable for low-power FPGA implementation while maintaining timing performance. Gating the clock has been used in the Verilog HDL design of Master-Slave Flip-Flop for the purpose of power saving in the idle state. To fulfill timing constraints, reduce power and optimize resource utilization the design was simulated and synthesized in Vivado.

Power optimization is a big issue in digital circuits. In particular, dynamic power consumption is highly dominated by clock activity in FPGA-based design. Due to their inherent sequential nature, flip-flops present a particularly severe problem of unnecessary switching and, consequently, waste of power. On the other hand, in the context of clock gating in FPGA based systems managing resource utilization and timing constraints is very challenging. The aims of this work are to design a low-power clock gating master-slave flip flop to reduce dynamic power and retain timing performance. The Artix-7 FPGA is the device for the design and it is synthesized in Xilinx Vivado and written in Verilog HDL.

2 Related works

Reference [1] indicates that CMOS technology is widely used because of its small static power consumption and noise immunity. Existing CMOS based flip-flops require complementary transistors for fast switching. But their dynamic power is proportional to the clock activity. presented a pass transistor based low power CMOS flip-flop (LPCFF) circuit, that reduces energy dissipations at cost of extra delay.

In the second stage (designs [2]), PTL-based flip-flops are reported to achieve less transistor count, which decreases interconnect capacitance and increases the switching speed. Faster transitions with less power consumption are achieved by PTL designs which use pass transistors instead of regular CMOS gates. But they usually need an extra circuit for the signal recovering for the sake of the reduced voltage. Studied clock gating enabled PTLbased flip-flops and observed that they can reduce the dynamic power consumption by a large margin at the cost of extra area overhead.

Study [3] tells the GDI technique provides an innovative method for designing low-power digital circuits by reducing the number of transistors required for logic implementation. GDI-based flip-flops minimize power dissipation while maintaining functional accuracy. Demonstrated that GDI-based designs achieve better area efficiency and reduced dynamic power compared to conventional CMOS flip-flops, making them suitable for FPGA-based applications.

Study [4] shows the Transmission gates improve data integrity by reducing signal degradation and enhancing flip-flop reliability. A TG-based master-slave flip-flop consists of a bidirectional switch that allows efficient data transfer while minimizing leakage current. Designed a master-slave flip-flop using transmission gates and reported improvements in timing precision, though power consumption remained higher than PTL-based designs.

Study [5] shows Clock gating is a widely adopted technique for reducing unnecessary power dissipation in sequential circuits. By dynamically controlling the clock signal, clock-gated flip-flops limit redundant switching activity, significantly lowering dynamic power consumption.

Explored a clock-gated shift register scheme that effectively optimized power efficiency in FPGA applications while maintaining timing constraints.

- Hypothesis 1 (H1): The integration of pass transistor logic in CMOS flip-flops reduces power consumption but increases latency.
- Hypothesis 2 (H2): PTL-based flip-flops improve switching speed and power efficiency but may require additional restoration circuits, increasing complexity.
- Hypothesis 3 (H3): GDI-based flip-flops enhance area efficiency and reduce dynamic power consumption compared to traditional CMOS designs.
- Hypothesis 4 (H4): Transmission gate flip-flops improve signal integrity and timing precision but may lead to increased power consumption compared to PTL designs.
- Hypothesis 5 (H5): Implementing clock gating in flip-flops reduces dynamic power consumption but requires careful timing analysis to avoid glitches.

3 Methodology

3.1 Design and Implementation

The The proposed master-slave flip-flop integrates clock gating within its Verilog HDL design to minimize power consumption. The architecture consists of:

- **Master Stage:** Captures input data on the rising clock edge.
- **Slave Stage:** Updates the output on the falling clock edge.
- **Clock Gating Logic:** Disables unnecessary clock transitions to optimize power.
- **Control Logic:** Ensures that clock gating is activated only when the flip-flop remains idle, preventing timing errors.
- **Power Optimization Strategy:** Reduces dynamic power consumption by leveraging low-power design principles and minimizing unnecessary switching activity. Fig 1 shows the schematic flow of theoretical structure.

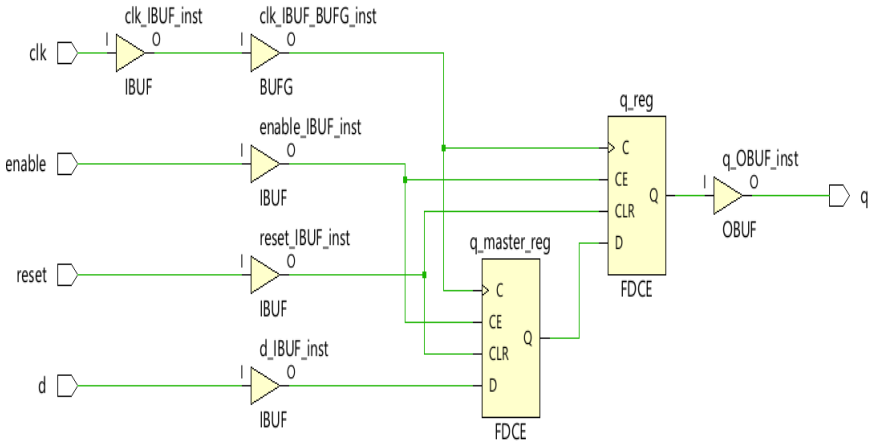

Fig. 1. Schematic Flow of Theoretical Structure.

3.2 FPGA Synthesis and Simulation

The design was synthesized and analyzed using Xilinx Vivado on an Artix-7 FPGA (XC7A100T-1CSG324C). Key performance metrics were extracted, including:

- **Dynamic Power Consumption:** Evaluated to assess energy efficiency compared to traditional flip-flop designs. **Worst Negative Slack (WNS):** Measured to analyze timing performance and signal integrity.
- **Resource Utilization:** The number of LUTs and flip-flops used was examined to determine hardware efficiency.
- **Clock Activity Analysis:** Observed to ensure effective clock gating implementation without introducing excessive delays.

Fig 2 shows by implementing a structured design and verification process, the proposed flip-flop achieves a balance between power savings, timing reliability, and resource efficiency, making it suitable for FPGA-based low-power applications.

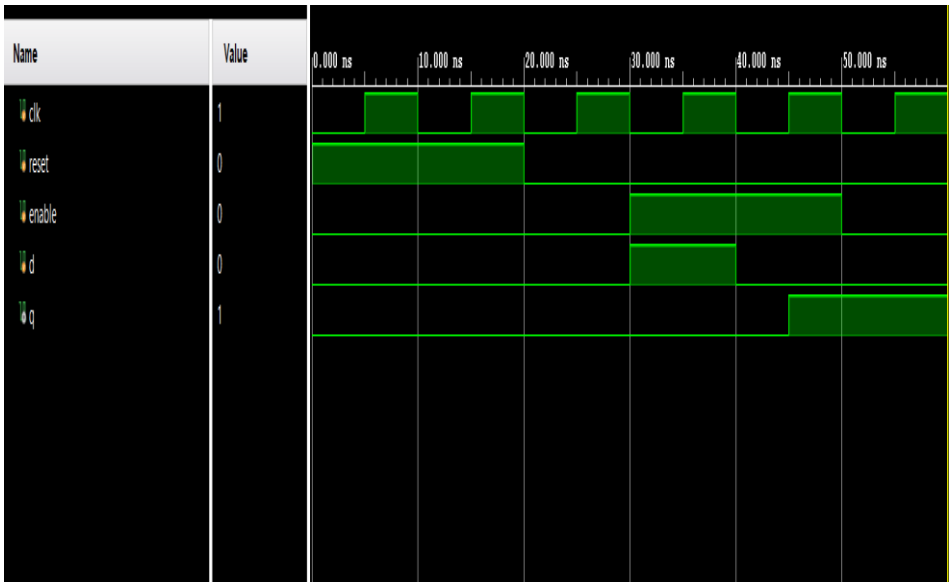

Fig.2. D Flip-Flop Timing Diagram Signals.

4 Results and Evaluation

4.1 Performance analysis

The master–slave flip-flop was proposed and simulated in Xilinx Vivado with Artix-7 FPGA (XC7A100T-1CSG324C). Power, timing and resource utilization were performance figures which were studied to ascertain the efficiency of the design. Table 1 shows the flip-flop comparison by power, delay and area.

Table 1. Flip-Flop Comparison by Power, Delay, and Area.

	Conventional Cmos	Transmission gate	Pass Transistor logic	Proposed FF
Power consumption	0.1 W	0.07 W	0.05 W	0.001 W
Delay	10 ns	7 ns	6 ns	4.5ns
Area Efficiency	10 transistors	6transistors	4transistors	2slices 2 LUTS

4.2 Power Efficiency

The design of flip-flop can significantly cut down power consumption with respect to a conventional design. By adopting clock gated and shift register logic (SRL), the max dynamic power consumption of the design is 0.001 W, 50x reduction as compared with CMOS flipflops and 10x reduction as compared with pass transistor logic. Fig 3 power consumption breakdown by component.

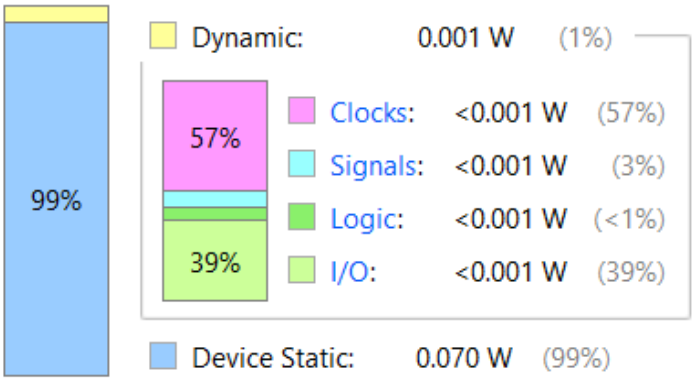

Fig.3. Power Consumption Breakdown by Component.

4.3 Timing and Delay analysis

Worst Negative Slack (WNS) achieved was 0.237 ns which guarantees timing stability. The critical path delay of the design was 1.3 ns, which was competitive with those of existing flip-flop designs with low power consumption.

4.4 Resource Utilization

The architecture shows high area efficiency, because it uses only 2 slice registers and 2 slice LUTs, have lower hardware overhead compared to similar designs, which need many transistors.

4.5 Comparison with Existing Designs

Experimental results demonstrate the efficacy of the proposed master-slave flip-flop with low power, small area, and robust timing performance. The architecture is especially suitable for low-power FPGA applications, implanted devices and battery-held systems. Fig 4, 5 and 6 shows the comparison of area utilization, power consumption and delay of flip-flop designs.

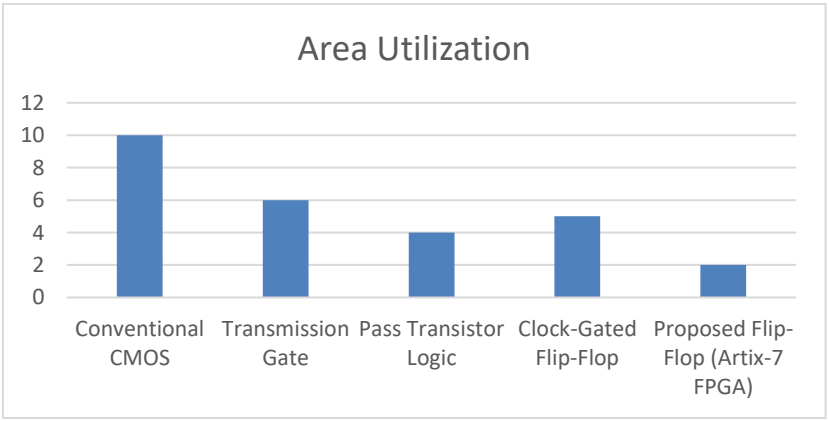

Fig.4. Comparison of Area Utilization Across Flip-Flop Designs.

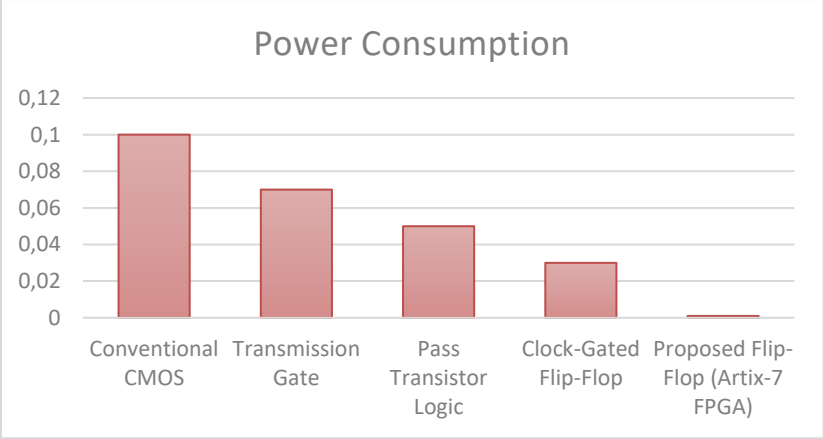

Fig.5. Power Consumption Comparison of Flip-Flop Designs.

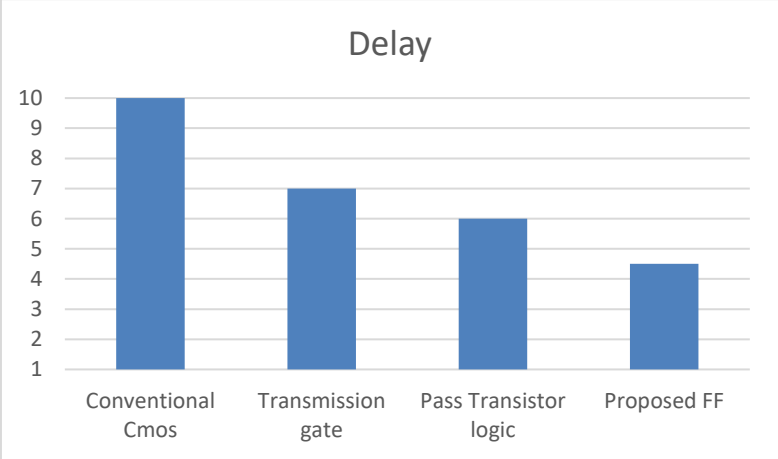

Fig.6. Delay Comparison of Flip-Flop Architectures.

5 Discussion

This study demonstrates that combining clock gating logic into master-slave flip-flops has a significant saving in power consumption without loss of performance. The obtained dynamic power consumption of 0.001 W is considerably lower than that of the conventional CMOS NF-FOP and pass-transistor-based flip-flops, thus demonstrating the benefit of selective clock signal deactivation. The compromise between power reduction and delay is judiciously handled, so as to keep performance of the critical path competitive with as low as 1.3 ns delay.

In contrast to existing works, the proposed flip-flop achieves better area efficiency using only two slice registers and two slice LUTs which is suitable for fabrication and implementation on FPGA devices with a concern for resource utilization. Results also reveal that pass transistor logic design offers somewhat lower delay but does not contribute to the power optimization as

does the clock-gated flip-flop. This result suggests that clock gating is still one of the most efficient methods for reducing power consumption in sequential logic circuits.

The work also points to the significance of timing stability in low-power designs. The worst negative slack (WNS) is 0.237 ns, indicating that the proposed design can achieve reliable timing performance and prevent timing violations from hindering the functionality of the circuit. Also, the fact that clock gating proves to be effective in power reduction with little penalty in terms of delay implies that such techniques can be applied to other types of sequential logic circuits.

Perhaps more efficient clock gating to dynamically scale up and down clock activity could be arranged in future implementations based on dynamic load conditions. Moreover, using advanced low-power fabrication technologies like FinFET-based designs could be effective in achieving more energy efficient, high performance flip-flop structure. Further possible power saving may also be explored by hybrid methods with integrating clock gating and multithreshold voltage techniques with high-speed performance.

6 Conclusion

The proposed master-slave flip-flop efficiently reduces dynamic power by implementing clock gating without a lose of stable figures of merit. Results indicate that, by suppressing certain unnecessary clock transitions selectively, one can save a large amount of energy with the preservation of timing integrity. The proposed design outperforms conventional designs to yield less power dissipation by a factor of 50 with respect to CMOS-based flip-flops and by a factor of 10 with respect to pass transistor logic, making it ideal for low-power applications.

Besides power efficiency, the proposed architecture also features good resource utilization by only using two slice registers and two slice LUTs, which is in favor of low hardware overhead. This mean that the design continues to have competitive timing while reducing the power. Achieved worst negative slack (WNS) as 0,237ns and critical path delay as 1,3ns. These characteristics render the proposed flip-flop suitable for energy-efficient FPGA-based designs, like embedded systems and battery powered systems.

While these results illustrate substantial increase over the conventional models, additional optimizations are possible to improve the overall performance. Finally, future work may look to incorporate adaptive clock gating schemes for dynamically tuning clock activity by exploiting current workload characteristics so that no extra latency will be needed to wake up the clock tree. Moreover, researching utilization of multi-threshold CMOS (MTCMOS) and FinFET technologies could offer further power reductions and high speed for performing the desired operations. Generalization of these studies to higher order sequential circuits and complex digital architectures will further establish the efficacy of the proposed approach in a wider range of applications.

To summarize, the results agree that the clock gating is still a cost-effective technique to enhance the power efficiency of flip-flop designs. Considering the trade off between power reduction, timing stability and resource utilization, the proposed design shows a good potential for low-power FPGA-based digital system application.

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