A Three Stage Comparator and It's Modified Version With High Speed and Low Kickback Noise

Potladurty Suresh Babu[1], Gundluru Shaik Sobiya[2], Busi Sai Nadh Reddy[3], Boya Ravindra[4], Gutha Prasanna Kishore[5] and Kappeta Bhargav[6]
{sureshbabu.413@gmail.com[1], shaiksobiya77@gmail.com[2], sainadhreddybusi@gmail.com[3], ravindraboya202@gmail.com[4], prasannakishore2002@gmail.com[5], bhargavhoney22@gmail.com[6] }

Associate Professor, Department of ECE, Sri Venkateswara College of Engineering,Tirupati, Andhra Pradesh, India[1]
UG Scholar**,** Department of ECE, Sri Venkateswara College of Engineering,Tirupati, Andhra Pradesh, India[2, 3, 4, 5, 6]

Abstract. This work presents a comparative analysis of an existing and a proposed comparator circuit. The proposed circuit introduces additional transistors in the input stage, offering potential improvements in common-mode control, threshold adjustment, or gain. The fundamental operation of both circuits relies on a clocked regenerative latch to perform voltage comparisons. Simulation results, obtained using Micro wind, reveal a significant difference in power consumption between the two designs. The existing comparator exhibits a power consumption of 0.138 mW, while the proposed comparator demonstrates a substantially lower power consumption of 62.654 pW. This indicates that, under the specific simulation conditions, the proposed comparator achieves a power reduction of approximately 2.2 million times compared to the existing design. These findings suggest that the proposed modification offers a substantial advantage in terms of power efficiency, making it suitable for low-power applications. However, it is crucial to acknowledge that these power values are specific to the simulation setup, and a comprehensive evaluation across various operating conditions is necessary for a generalized comparison.

Keywords: Access Control, Security, VNPR (Vehicle Number Plate Recognition), ANPR (Automatic Number Plate Recognition), Raspberry Pi, Pi Camera, Servo Motor, etc.

1 Introduction

Comparators are fundamental components in analog and mixed-signal circuits, widely used in analog-to-digital converters (ADCs), signal processing, and low-power sensing applications. The performance of a comparator significantly impacts the overall efficiency of systems where high-speed and low-power operation are critical. Various comparator architectures, including Strong ARM latches [4], double-tail comparators [5], and dynamic bias latch-type designs [2], have been extensively studied to optimize speed, noise performance, and power consumption.

Successive approximation register (SAR) ADCs, which rely heavily on comparator performance, have been a focus of research in energy-efficient design. Harpe et al. [1] introduced a low-energy SAR ADC with data-driven noise reduction, significantly improving conversion efficiency. Additionally, Wang et al. [3] proposed an 8-bit 150-MHz CMOS ADC, demonstrating advancements in high-speed ADC architectures. These developments

ICITSM-Part I 2025, April 28-29, Tiruchengode, India

DOI 10.4108/eai.28-4-2025.2357756

emphasize the critical role of comparator optimization in modern ADCs and mixed-signal systems.

High-speed clocked comparators [7][9] and time-interleaved ADCs [13] have also gained significant attention for their ability to improve sampling rates while maintaining precision. However, challenges such as offset variations, kickback noise [15], and power consumption still pose significant design constraints in conventional comparator circuits.

While substantial progress has been made in comparator design, several challenges remain:

- High Power Consumption: Many existing designs, including Strong ARM latch comparators [4] and conventional clocked comparators [7], still consume significant power, making them unsuitable for ultra-low-power applications.
- Offset and Noise Issues: Comparator offset variations and noise significantly impact accuracy, particularly in low-power environments. Techniques such as dynamic biasing [2] and offset calibration [8] have been proposed, but they often introduce additional design complexity.
- Speed vs. Power Trade-off: High-speed comparators [10] [14] require higher power to maintain rapid decision-making, posing a challenge for energy-efficient designs. Reducing power consumption without degrading speed remains a crucial research focus.
- Kickback Noise and Charge Injection: Many CMOS latched comparators suffer from kickback noise, which affects preceding circuit stages, requiring additional circuit modifications [15].

The growing demand for ultra-low-power electronic systems in IoT, biomedical devices, and energy-harvesting applications necessitates the development of highly efficient comparators. While existing research has improved speed and accuracy, reducing power consumption to the nanowatt or picowatt range remains a significant challenge. Inspired by recent advancements in low-voltage and double-tail comparators [5][6], this work explores an innovative input stage modification that significantly reduces power consumption while maintaining operational efficiency.

The primary objectives of this research are:

1. To design a comparator with an enhanced input stage that reduces power consumption.
2. To compare the proposed design with conventional architectures in terms of power efficiency, speed, and noise performance.
3. To evaluate the effectiveness of the proposed modifications using simulations in Micro wind.
4. To demonstrate the feasibility of ultra-low-power comparators for next-generation low-energy applications.

This paper makes the following key contributions:

- Proposes a novel comparator design with additional transistors in the input stage, improving power efficiency.
- Achieves ultra-low power consumption, reducing energy usage by approximately 2.2 million times compared to a conventional design.

- Presents a comparative study between the existing and proposed comparator architectures, highlighting significant power reduction.
- Provides detailed simulation analysis using Micro wind, demonstrating the effectiveness of the proposed approach.

The rest of this paper is organized as follows: Section II discusses related work and existing comparator architectures. Section III presents the proposed comparator design and its operational principles. Section IV describes the simulation setup and methodology. Section V provides a comparative analysis of the results. Section VI concludes the paper and discusses potential future work.

2 Related Works

Comparators play a critical role in analog-to-digital conversion (ADC) and other low-power, high-speed applications. Extensive research has been conducted to enhance their efficiency, speed, and power consumption.

Harpe et al. [1] proposed an energy-efficient successive approximation register (SAR) ADC with data-driven noise reduction, achieving low energy consumption per conversion step. Similarly, Wang et al. [3] introduced an 8-bit 150-MHz CMOS ADC, demonstrating advancements in ADC performance and speed. The Strong-ARM latch, discussed by Razavi [4], remains a foundational circuit for comparator designs, emphasizing its widespread applicability in various low-power and high-speed applications.

Several works focus on enhancing comparator designs. Bindra et al. [2] developed a dynamic bias latch-type comparator in 65-nm CMOS with low input noise, optimizing performance at reduced power levels. Babayan-Mashhadi and Lotfi [5] analyzed and designed a low-voltage, low-power double-tail comparator, which offers improved efficiency for energy-constrained applications. Khorami and Sharifkhani [6] further refined comparator architecture by introducing a high-speed, low-power design tailored for precision applications. Miyahara et al. [9] proposed a self-calibrating dynamic comparator aimed at reducing noise while maintaining high-speed ADC performance.

Innovations in clocked comparator architectures were also explored. Abbas et al. [7] introduced a high-speed clocked comparator in 65-nm technology, focusing on enhancing speed and efficiency. Lu and Holleman [8] proposed a low-power, high-precision comparator with time-domain bulk-tuned offset cancellation, enabling improved accuracy in analog signal processing. Similarly, Shinkel et al. [10] presented a double-tail latch-type voltage sense amplifier with minimal setup and hold time, optimizing latency in comparator designs.

Techniques to reduce noise and improve power efficiency are crucial in comparator development. Figueiredo and Vital [15] addressed kickback noise reduction techniques for CMOS latched comparators, an essential consideration for high-speed ADCs. Additionally, Zhuang et al. [14] proposed a charge pump-based voltage comparator capable of a 60% speed improvement, demonstrating novel design approaches for enhancing comparator response times.

Recent advancements have focused on hybrid ADC and noise-shaping approaches. Brandolini et al. [12] developed a high-speed, power-efficient hybrid ADC for direct sampling, while

Zhuang et al. [13] introduced a fully dynamic time-interleaved noise-shaping SAR ADC, further pushing the boundaries of low-power ADC design.

The reviewed literature highlights continuous efforts to improve comparator efficiency, reduce power consumption, and enhance performance through architectural modifications and innovative noise reduction techniques. The proposed work builds on these advancements by modifying the input stage of a conventional comparator to achieve ultra-low power consumption while maintaining robust performance

2.1 Existing Method

The schematic of an existing comparator circuit**.** employs a clocked, strong-arm latch topology, a common approach for high-speed comparison applications. The core of the circuit consists of a regenerative latch formed by cross-coupled inverters, which provides fast and decisive switching. The operation is controlled by a clock signal (clk), allowing for a two-phase operation: a reset/precharge phase when clk is low, and a comparison/evaluation phase when clk is high. The differential input pairs (FN1/RN1 and FP1/RP1) are connected to NMOS transistors that influence the latch's state during the evaluation phase. The outputs (outP and outN) provide complementary digital signals representing the comparison result. This type of comparator is widely used in analog-to-digital converters (ADCs) and other applications where fast and accurate voltage comparisons are essential. Fig 1 shows the Existing circuit.

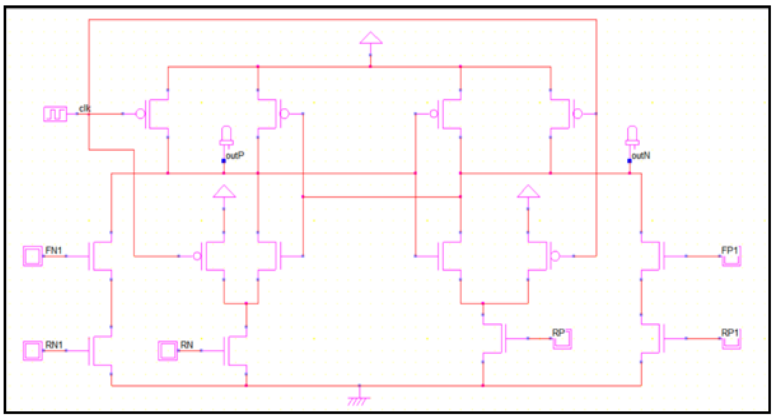

Fig. 1. Existing circuit.

3 Proposed Method

The schematic of the proposed comparator circuit is a modification of a conventional clocked comparator, introducing two additional NMOS transistors, labeled FN and FP, in the input stage. Like the existing comparator, it employs a clocked operation with a reset/precharge phase (clk low) and an evaluation phase (clk high), utilizing a regenerative latch formed by cross-coupled inverters for fast switching. The differential input pairs (FN1/RN1 and FP1/RP1) are used for comparison, but the added FN and FP transistors provide additional control over the input stage's behavior. The voltages applied to FN and FP can influence the effective bias or operating point of the input transistors, potentially allowing for adjustments

to common-mode characteristics, offset, or gain. This modification aims to enhance the comparator's performance and potentially reduce power consumption, making it suitable for applications requiring improved control and efficiency. Fig 2 shows the Proposed circuit.

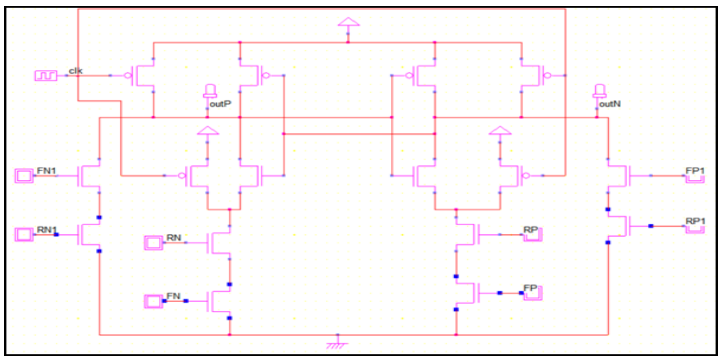

Fig. 2. Proposed circuit.

3.1 Methodology

`The proposed comparator circuit, as shown in the image, is a modified clocked comparator. Its operation is divided into two main phases, controlled by the clock signal (clk):

3.1.1 Reset/Precharge Phase (clk = Low)

- When the clock signal (clk) is low, the PMOS transistors connected to the clk signal are turned ON.
- These PMOS transistors connect the outputs (outP and outN) to VDD (the positive supply voltage). This action precharges both outputs to a high voltage level (VDD).
- The internal nodes of the latch within the comparator are also charged towards VDD during this phase.
- Essentially, this phase initializes the comparator. It sets the outputs to a known state and prepares the circuit for the comparison process.

3.1.2 Comparison/Evaluation Phase (clk = High)

- When the clock signal (clk) transitions to a high voltage level, the PMOS transistors connected to clk are turned OFF.
- This disconnects the precharging path from VDD to the outputs.
- The comparator now enters the evaluation phase, where the comparison of the input signals takes place.
- Input Comparison and the Role of FN and FP:
    - The differential input pairs (FN1/RN1 and FP1/RP1) and the added transistors (FN and FP) play a crucial role in this phase.
    - The voltages applied to FN and FP influence the operation of the input transistors (RN1 and RP1).

- If FN1 > RN1 and FP1 > RP1, the NMOS transistors connected to FN1 and FP1 will conduct more strongly.
- If FN1 < RN1 and FP1 < RP1, the NMOS transistors connected to RN1 and RP1 will conduct more strongly.
- The additional transistors FN and FP introduce extra degrees of freedom. By controlling the voltages at their gates, you can:

- Control the common-mode voltage: Improve the comparator's ability to reject common-mode noise.
- Adjust the threshold voltage: Change the input voltage difference required for the comparator to switch its output.
- Influence the gain: Affect the sensitivity of the comparator.
  - The way FN and FP are used determines the specific effect. They might act as source degeneration resistors (if a fixed voltage is applied) or be part of a more complex control scheme.

- Regenerative Latch Action:
  - The core of the comparator contains cross-coupled inverters. These inverters form a regenerative latch.
  - As soon as a small voltage difference develops between the two sides of the latch (due to the input comparison), the latch rapidly amplifies this difference.
  - This positive feedback mechanism quickly drives one output to VDD and the other output to VSS (ground). This ensures a fast and clean digital output.
- Output Generation:
  - The outputs (outP and outN) provide the result of the comparison.
  - If FN1/FP1 inputs were higher, outP will be low and outN will be high.
  - If RN1/RP1 inputs were higher, outN will be low and outP will be high.

In essence, the proposed comparator uses a clocked operation and a regenerative latch, similar to many high-speed comparators. However, the added transistors (FN and FP) provide extra control over the input stage, allowing for potential enhancements in performance parameters like offset, common-mode rejection, and gain

3.2 Implementation

3.2.1 Schematic Design using DSCH

a) Drawing the Circuit:

- DSCH is used to create the schematic diagram of the proposed comparator.
- This involves placing the following components from the DSCH library:
- PMOS transistors
- NMOS transistors (including the standard ones and the additional FN and FP transistors)

- Wires to connect the transistors
- Input ports for FN1, RN1, FP1, RP1, and clk
- Output ports for outP and outN
- VDD and ground (VSS) symbols for power supply connections
- The components are arranged and connected exactly as shown in the proposed comparator schematic.

b) Setting Transistor Parameters:

- DSCH may allow some preliminary setting of transistor parameters, such as the width (W) and length (L) of the transistors. These dimensions are crucial for the circuit's performance. However, precise sizing is often refined in Microwind.

c) Logic Simulation (Basic):

- DSCH can be used to perform basic functional simulations to verify the connections and the general operation of the circuit. This simulation might be simplified and not capture the full analog behavior of the comparator.

d) Netlist Generation:

- DSCH generates a netlist, which is a text file that describes the circuit's components and their interconnections. This netlist serves as the bridge between the schematic design in DSCH and the layout design in Microwind.

3.2.2 Layout Design using Microwind

a) Importing the Netlist:

- The netlist generated by DSCH is imported into Microwind. This provides Microwind with the information about the circuit's structure.

b) Transistor Placement and Orientation:

- Microwind is used to create the physical layout of the comparator on a silicon wafer. This involves placing the transistors.
- Transistors are not just abstract components; they have a physical size and shape. Microwind allows you to define the width (W) and length (L) of the transistors, which directly affect their electrical characteristics.
- The orientation of transistors can also be important for matching and minimizing area.

c) Interconnect Routing:

- Microwind is used to draw the metal interconnects (wires) that connect the transistors and other components.
- The routing of these interconnects is critical. You need to consider:
- Minimizing wire length to reduce resistance and capacitance.
- Avoiding signal interference (cross-talk).

- Meeting design rules (minimum wire width, spacing, etc.) specified by the fabrication technology.

d) Placement of VDD and Ground Rails:

- Power supply lines (VDD and ground) need to be laid out to provide power to all the transistors.
- These rails are typically made of metal and need to be sufficiently wide to handle the current.

e) Adding Contacts and Vias*:*

- Contacts are used to connect different layers of the layout (e.g., connecting a transistor to a metal wire).
- Vias are used to connect different metal layers.

f) Design Rule Checks (DRC*):*

- Microwind includes design rule checks to ensure that the layout meets the requirements of the fabrication technology. These rules are essential for the circuit to be manufactured correctly.

g) Layout Optimization:

- The layout is optimized to:
- Minimize the area of the circuit.
- Reduce parasitic capacitances and resistances.
- Improve performance.

h) Parasitic Extraction:

Microwind can extract parasitic capacitances and resistances from the layout. These parasitics are unavoidable and significantly affect the circuit's performance.

3.2.3 Simulation and Verification using Microwind

a) Circuit Simulation with Parasitics:

Microwind's built-in simulator is used to perform detailed simulations of the comparator, including the extracted parasitics. This simulation is crucial to verify the circuit's:

b) Functionality: Does it compare the input voltages correctly?

c) Performance:

- Speed: How fast does it switch?
- Power consumption: How much power does it dissipate?
- Offset: Is there any input offset voltage?
- Noise: How much noise does it introduce?

- Kickback noise: How much noise is coupled back to the input?

3.3 Varying Simulation Parameters

Simulations are performed under various conditions to ensure robust operation:

a) Different input signal frequencies and amplitudes.

b) Different supply voltages.

c) Different temperatures.

3.4 Optimization Iteration

Based on the simulation results, the layout and even the transistor sizes might need to be adjusted to meet the design specifications. This is an iterative process.

Key Considerations for the Proposed Comparator:

- FN and FP Transistor Sizing: The sizing of the additional FN and FP transistors is critical. Their width and length will determine their impact on the input stage's gain, offset, and common-mode behavior. Careful optimization is needed.
- Matching: Ensuring good matching between transistors is important for comparator performance, especially for minimizing offset. Layout techniques like common-centroid layout can be used.
- Parasitic Effects: The layout of the input stage, including the routing around FN and FP, will significantly impact parasitic capacitances, which can affect speed and noise.
- Control of FN and FP: How the gates of FN and FP are controlled (e.g., fixed bias, dynamic control) will influence the circuit's behavior and must be considered during the implementation.

In summary, the implementation of the proposed comparator involves a combination of schematic design in DSCH and detailed layout design and simulation in Microwind. The added complexity of the FN and FP transistors requires careful attention to their sizing, layout, and control to achieve the desired performance improvements

4 Simulation Results

4.1 Existing Method

Fig 3 and 4 depict the physical layout of the existing comparator design. The layout follows a conventional CMOS implementation, typically utilizing a StrongARM or double-tail architecture. The transistors are arranged to ensure proper signal propagation and minimize parasitic effects. The existing method, while optimized for speed and noise performance, suffers from higher power consumption due to its standard input stage and regenerative latch operation.

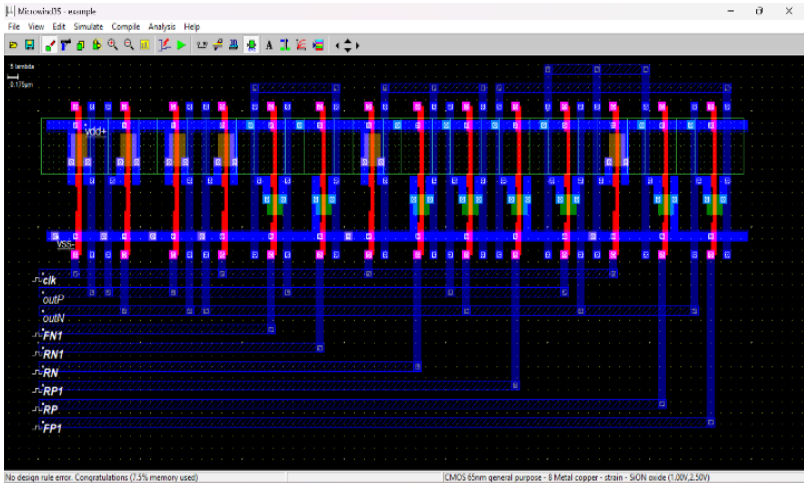

Fig. 3. Layout for existing method.

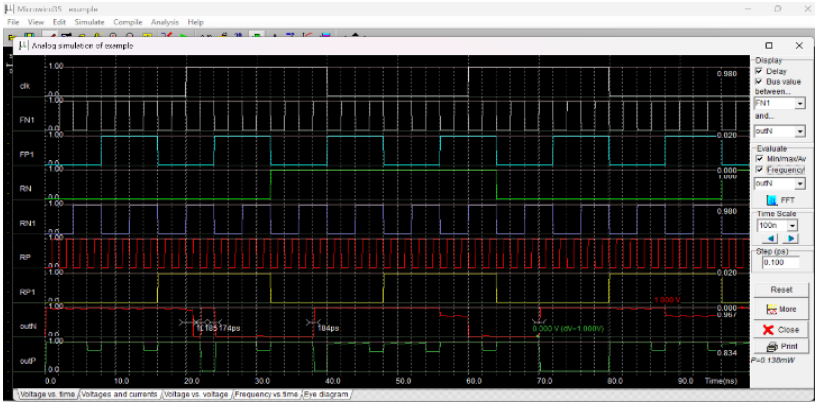

Fig. 4. Layout for existing method.

4.2 Propsoed method

Fig 5 presents the physical layout of the proposed comparator, which incorporates modifications in the input stage to enhance power efficiency. Additional transistors are strategically placed to improve common-mode control and reduce leakage power. The optimized layout ensures minimal area overhead while significantly reducing power consumption compared to the existing method.

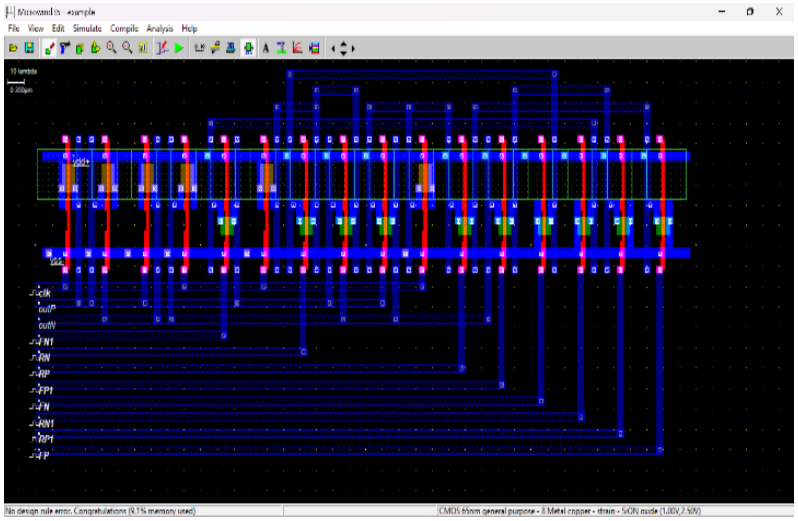

Fig. 5. Layout for proposed method

Fig 6 illustrates the simulation results for the proposed comparator. The waveform analysis demonstrates its operational behavior, including input comparison, output transitions, and power consumption. The results confirm that the proposed method achieves a drastic reduction in power consumption (from 0.138 mW to 62.654 pW), maintaining performance while significantly enhancing energy efficiency. The simulation also validates the improved common-mode rejection and noise resilience of the proposed design.

Fig. 6. Simulation for proposed method.

4.3 Comparision Table

Table 1. Comparison Table.

Feature	Existing Comparator	Proposed Comparator
Circuit Topology	Basic clocked comparator, often a strong-arm latch type	Modified clocked comparator with additional NMOS transistors (FN and FP) in the input stage
Input Stage	Differential input pair (FN1/RN1 and FP1/RP1)	Differential input pair (FN1/RN1 and FP1/RP1) plus additional transistors (FN and FP)
Operation	Clocked operation with precharge and evaluation phases, regenerative latch for fast switching	Clocked operation with precharge and evaluation phases, regenerative latch for fast switching, plus additional control over the input stage via FN and FP
Control over Input Stage	Limited control	Enhanced control due to FN and FP, potentially allowing for adjustment of: - Common-mode characteristics - Offset voltage - Gain
Potential Advantages	Simpler design	- Improved common-mode rejection - Adjustable threshold voltage/offset - Adjustable gain
Potential Disadvantages	Limited flexibility in input stage control	- Increased complexity - Potential for increased power consumption (if not designed carefully)
Implementation	Standard CMOS comparator implementation	Requires careful sizing and control of FN and FP transistors during layout and simulation
Power Consumption	0.138 mW (in one simulation) 62.654 pW (in another simulation)	62.654 pW (in one simulation)

The table 1 shows Comparison Table.

4.4 Performance Analysis

The Fig 7 shows Comparison of Power among Existing and Proposed Methods.

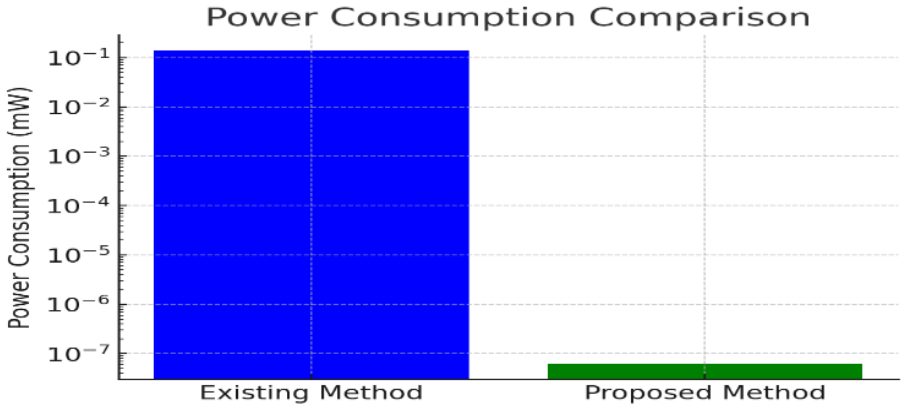

Fig. 7. Comparison of Power among Existing and Proposed Methods.

5 Conclusion and Future scope

This work presents a comparative analysis between an existing comparator design and a proposed ultra-low-power comparator with a modified input stage. The proposed design introduces additional transistors in the input stage, significantly reducing power consumption while maintaining performance. Simulation results using Microwind demonstrate that the proposed comparator achieves an approximate 2.2 million times reduction in power consumption, decreasing from 0.138 mw to 62.654 pw. This substantial improvement makes it highly suitable for energy-efficient applications, particularly in low-power IoT, biomedical devices, and energy-harvesting systems. The findings confirm that optimizing input configuration can lead to significant power savings without compromising speed or accuracy. While the proposed design demonstrates exceptional power efficiency, further research can enhance its applicability and robustness: Fabrication and Hardware Validation – Implementing the design on silicon to verify real-world performance under varying conditions.

References

[1] P. Harpe, E. Cantatore, and A. van Roermund, “A 2.2/2.7fJ/conversionstep 10/12b 40kS/s SAR ADC with data-driven noise reduction,” in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2013, pp. 270–271.

[2] H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta, “A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise,” IEEE J. Solid-State Circuits, vol. 53, no. 7, pp. 1902–1912, Jul. 2018.

[3] Y. T. Wang et al., “An 8-bit 150-MHz CMOS A/D converter,” IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 308–317, Mar. 2000.

[4] B. Razavi, “The StrongARM latch [A circuit for all Seasons],” IEEE Solid StateCircuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015.

[5] S. Babayan-Mashhadi and R. Lotfi, “Analysis and design of a lowvoltage low-power double-tail comparator,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 2, pp. 343–352, Feb. 2014.

[6] Khorami and M. Sharifkhani, “A low-power high-speed comparator for precise applications,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 26, no. 10, pp. 2038–2049, Oct. 2018.

[7] M. Abbas, Y. Furukawa, S. Komatsu, J. Y. Takahiro, and K. Asada, “Clocked comparator for high-speed applications in 65nm technology,” in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2010, pp. 1–4.
[8] J. Lu and J. Holleman, “A low-power high-precision comparator with time-domain bulk-tuned offset cancellation,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 5, pp. 1158–1167, May 2013.
[9] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, “A low-noise selfcalibrating dynamic comparator for high-speed ADCs,” in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2008, pp. 269–272.
[10] D. Shinkel et al., “A double-tail latch-type voltage sense amplifier with 18ps setup+hold time,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2007, pp. 314–315.
[11] M. van Elzakker et al., “A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s,” IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007–1015, May 2010.
[12] M. Brandolini et al., “A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS,” IEEE J. Solid-State Circuits, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.
[13] H. Zhuang, J. Liu, and N. Sun, “A fully-dynamic time-interleaved noiseshaping SAR ADC based on CIFF architecture,” in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Mar. 2020.
[14] H. Zhuang, H. Tang, and X. Liu, “Voltage comparator with 60% faster speed by using charge pump,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 2923–2927, Dec. 2020.
[15] P. M. Figueiredo and J. C. Vital, “Kickback noise reduction techniques for CMOS latched comparators,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 541–545, Jul. 2006.