FPGA Design and Optimization Implementation of GPS Positioning Algorithm

Wei He[1], Zhi Jiang[2], Zengshan Tian[3], Mu Zhou [4], Shuai Lu[5]
{hewei@cqupt.edu.cn[1], 1455830611@qq.com[2], tianzs@cqupt.edu.cn[3], zhoumu@cqupt.edu.cn[4], lushuai.139@163.com[5]}

School of Communication and Information Engineering, Chongqing University of Posts and Telecommunications, Chongqing 400065, China

Abstract. Propose a parallel data processing framework method based on field programmable gate array (FPGA). In this paper, the complexity analysis of GPS classic localization algorithm is carried out. Within the scope allowed by hardware logic resources, the FPGA hardware implementation framework is designed with the idea of area exchange rate, that is, a large number of pipeline operations are used in Verilog language programming to improve system processing speed. The experimental results show that FPGA achieves highprecision positioning, in the WGS-84 coordinate system, the error of the X-axis about 5m, and the error of the Y-axis and the Z-axis is about 2m.

Keywords: field programmable gate array; parallel data processing; pipeline

1 Introduction

GPS pseudo-range single-point positioning is widely used in various vehicles, ships for navigation and monitoring, and field surveys due to its advantages such as fast speed, no ambiguity in the whole cycle, and cheap signal receivers [1, 2, 3]. Especially when the accuracy is not high and the geographical environment is more complicated and dangerous, the pseudo-point single-point positioning can greatly reduce the difficulty of the operation and exert its maximum effect.

At present, a large number of algorithms have been studied for GPS pseudo-range single-point positioning. Reference [4] quoted an iterative extended Kalman filter algorithm to analyze GPS ephemeris data, and simulation results show that the method achieves the effect of improving positioning accuracy. Reference [5] adopted two different improvement strategies for the random noise of the TEC time series in the ionospheric delay and the limitation of the Klobu-char model parameter setting. Reference [6] performed spherical fitting with multiple positioning coordinates solved by multiple sets of satellites in three-dimensional space, which improved the utilization rate of satellite data and the accuracy of satellite positioning. Reference [7] established a dual-mode system through the combination of Beidou system and GPS system to achieve multi-system positioning, which improved the superiority and reliability of the system. At the same time, the realization of GPS pseudo-range single-point positioning algorithm is also one of the main contents of current research. Reference [8] realized the GPS pseudo-range single-point positioning by programming on the eclipse platform using Java language. Although this is only implemented on the PC side, it has certain reference value for the hardware implementation of the algorithm.

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Reference [9] built a system from GPS data acquisition to positioning processing through the DSP processor. The reliability and stability of the system are verified through actual measurement. Reference [10] based on ARM plus FPGA platform2 realized phase smooth pseudo-range differential positioning, which is beneficial to improve the positioning accuracy.

At present, the research on GPS pseudo-range single-point positioning algorithm has matured. Most of the researches are mainly focused on the hardware implementation of the algorithm. The mainstream hardware implementation platforms mainly include FPGA and DSP, FPGA and ARM, or directly through the PC. DSP has unique advantages in processing digital signals, but the serial processing mode of DSP cannot meet the requirements of high real-time performance. The same problem still exists in ARM. Considering that the parallel processing method adopted in FPGA can realize high-speed signal processing, and the repeatable programming feature can ensure that the system can achieve online debugging. Therefore, this article designs a set of FPGA-based parallel pipeline architecture system scheme. Compared with the traditional DSP or ARM serial processing mode, the FPGA's operating mode reduces the delay of data processing and improves the speed of the entire positioning system. Makes the system highly scalable and better versatile.

2 Analysis of pseudorange positioning algorithm

2.1 Pseudo-range positioning principle

GPS measurement errors can be roughly divided into three aspects according to different sources: (1) errors related to satellites; (2) errors related to signal propagation; and (3) errors related to receivers. Considering that the magnitude of the deviation has a certain stability, the deviation value can be predicted by direct measurement or mathematical models. In this paper, three major error sources are corrected through classic modeling: ionospheric error, tropospheric error, and satellite clock error.

2.2 Pseudo-range positioning principle

As shown in figure 1, the geometric distance between the receiver and the satellite in a certain epoch is $r^{(\mathrm{n})}$. Where $x=[\mathrm{x,y,z}]^T$ is the unknown receiver position coordinate vector and $x^{(\mathrm{n})}=[\mathrm{x}^{(\mathrm{n})},\mathrm{y}^{(\mathrm{n})},\mathrm{z}^{(\mathrm{n})}]^T$ is the position coordinate vector of satellite n.

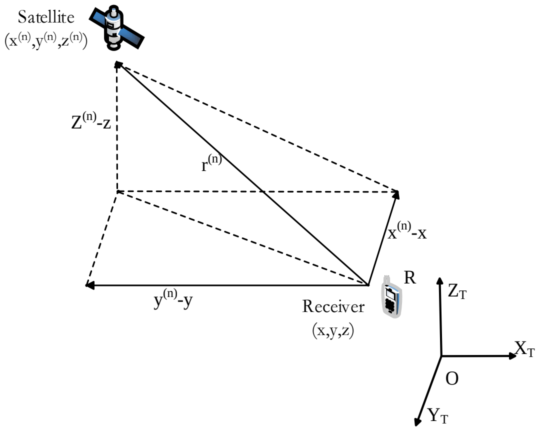

Fig. 1. Observation vector from receiver to satellite

The geometric distance from the receiver to the satellite can be expressed as:

$$r^{(\mathrm{n})}=\left\|\mathrm{x}^{(\mathrm{n})}-x\right\|=\sqrt{\left(\mathrm{x}^{(\mathrm{n})}-x\right)^2+\left(\mathrm{y}^{(\mathrm{n})}-y\right)^2+\left(\mathrm{z}^{(\mathrm{n})}-z\right)^2} \tag{1}$$

The pseudo-range observation equation of the receiver and the satellite at time t is:

$$p^{(\mathrm{n})}=r^{(\mathrm{n})}+\delta t_u-\delta t^{(\mathrm{n})}+I^{(\mathrm{n})}+T^{(\mathrm{n})}+\varepsilon_p{}^{(\mathrm{n})} \tag{2}$$

Where $n=1,2,\cdots,N$ is the temporary number of the satellite or satellite-measurement, $p^{(\mathrm{n})}$ is the pseudo-range observation, and $r^{(\mathrm{n})}$ is the geometric distance from the receiver to the satellite. δt_u 、 $\delta t^{(\mathrm{n})}$ 、 $I^{(\mathrm{n})}$ and $T^{(\mathrm{n})}$ are the receiver clock difference, satellite clock difference, ionospheric error, and tropospheric error, respectively, and $\varepsilon_p{}^{(\mathrm{n})}$ are noise measurements for pseudorange.

3 FPGA processing of positioning algorithm

Based on the analysis of the characteristics of the pseudo-range single-point positioning algorithm, this paper designs a hardware architecture for multi-floating-point arithmetic based on the pipeline structure for parallel computing. This makes full use of the characteristics of parallel processing of data within the FPGA. A trade-off between speed and area is achieved on hardware resources.

3.1 Cordic algorithm for complex operations

The pseudorange positioning algorithm involves not only simple arithmetic operations, but also complex operations such as trigonometric functions, inverse trigonometric functions, exponential functions, and logarithmic functions. From the perspective of hardware implementation, this article chooses the CORDIC (Coordinate Rotation Digital Computer) algorithm that only requires addition and subtraction to implement these complex operations.

As shown in Fig. 3, the vector V1 is obtained by rotating the angle V2.

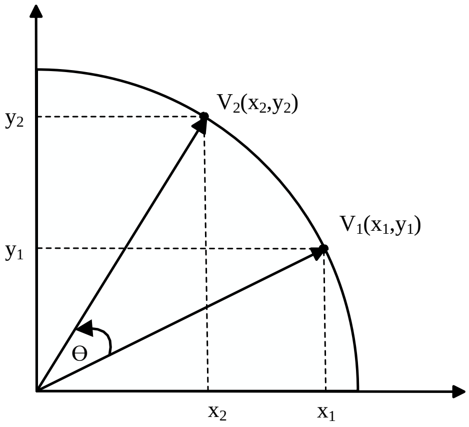

Fig. 2. Vector rotation in a circular coordinate system

The mathematical relationship from vector V1 to vector V2 is:

$$\begin{cases} x_2 = \cos\theta(x_1 - y_1 \tan\theta) \\ y_2 = \cos\theta(y_1 + x_1 \tan\theta) \end{cases} \tag{3}$$

The core of the CORDIC algorithm is the rotation angle θ . The algorithm divides a lot of different angle values θ^i that have been specified. So for each value θ that needs to be rotated, it can be obtained by n iterations of the value θ^i , among which there are $\tan\theta^i = 2^{-i}$, so get the CORDIC algorithm formula:

$$\begin{cases} x(\mathrm{n}) = \prod_{i=1}^{N} (\sqrt{1+2^{(-2\mathrm{i})}}(x_0 - \mathrm{d}_i \times y_0 \times 2^{-i})) \\ y(\mathrm{n}) = \prod_{i=1}^{N} (\sqrt{1+2^{(-2\mathrm{i})}}(y_0 + \mathrm{d}_i \times x_0 \times 2^{-i})) \end{cases} \tag{4}$$

In the formula, $[x(\mathrm{n}), y(\mathrm{n})]$ is an arbitrary point in the circumferential coordinate system, and d_i is a judgment factor for determining the rotation direction. In the circular rotation mode, the values of sin(x) and cos(x) can be directly calculated using the CORDIC algorithm, and more functions can be calculated by rotating in different coordinate systems (hyperbolic coordinate system, linear coordinate system,etc.).

3.1 Cholesky factorization for matrix operations

Matrix operations include transpose, multiplication, and inversion. The FPGA implementation of matrix inversion is mainly introduced here. In this paper, matrix inversion is implemented by matrix decomposition. This method can not only reduce the amount of calculations, but also is easy to implement in hardware. Commonly used matrix factorization methods include Cholesky factorization, LU factorization, and QR factorization. Based on Cholesky factorization, it is suitable for conjugate symmetric positive definite matrices. The matrix inversion module mainly includes three main parts: Cholesky decomposition, triangular matrix inversion and matrix multiplication. The specific processing flow is shown in Figure 5.

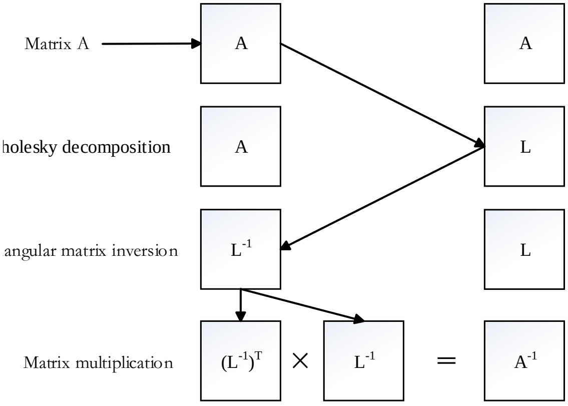

Fig. 3. Matrix inversion flowchart Matrix inversion flowchart

The matrix A is first decomposed by Cholesky to decompose the matrix into the product of the lower triangular matrix L and its transpose L^T , that is $A = L \times L^T$, then the inverse matrix L of the lower triangular matrix L^{-1} is obtained by backward transpose; finally the product of the inverse matrix of the lower triangular matrix and its transposition is realized ,which is $(L^{-1})^T \times L^{-1} = A^{-1}$. In the FPGA design, the Cholesky decomposition function module includes two memory blocks and two processing modules. One of the memory blocks is used to store the data of the input matrix. The data of the input matrix is loaded into the module line by line, and the other memory block is used. To store the matrix data being processed. For the triangular matrix L obtained by using the Cholesky decomposition module, the inverse matrix L^{-1} is calculated using the triangular matrix inversion algorithm. Finally, the multiplier of FPGA is used to design the product of the inverse matrix of the lower triangular matrix and its transpose, and the data of the resulting matrix is output row by row. Considering that the positioning algorithm requires high time sensitivity, this paper uses more multipliers and dividers in the implementation of Cholesky decomposition. It is necessary to consume more hardware resources on the premise of greatly improving the operation speed.

4 Algorithm verification and error analysis

4.1 Procedure analysis steps

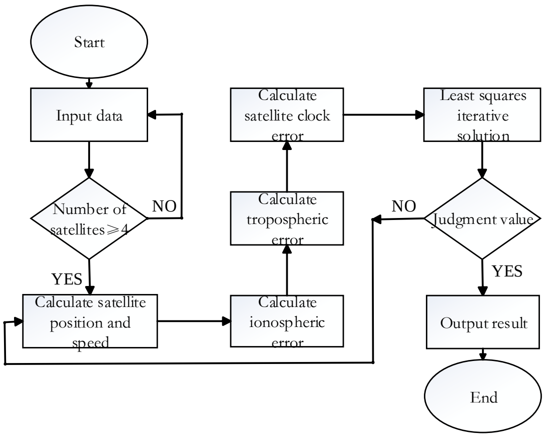
Start
Input data
Number of satellites≥4
NO
YES
Calculate satellite position and speed
Calculate ionospheric error
Calculate tropospheric error
Calculate satellite clock error
Least squares iterative solution
Judgment value
NO
YES
Output result
End

Fig. 4. Analysis steps of pseudo-range single-point positioning algorithm program

The analysis steps of the pseudo-range single-point positioning algorithm program are shown in Figure 6. The first step is to determine the number of satellites that have received information after preprocessing the input data. Positioning can only be performed when the number of satellites is greater than or equal to four. The second step is to calculate the position and operating speed of each satellite observed, as well as the ionospheric error, tropospheric error, and clock clock error of each observation satellite. The third step is to use the least squares method to iteratively solve the nonlinear equations and judge the operation results. If it is less than the set convergence value, it is judged to be convergence. The updated value is used as the position value of the receiver. The steps are complete.

4.2 Positioning error analysis

In order to ensure the correctness of the FPGA processing data, a new GNSS hardware platform OEM617D newly developed by Canada's NovAtel Corporation is selected for verification. The board can simultaneously use GPS, GLONASS and BDS dual-frequency signals for measurement and positioning. The positioning results can be directly configured and output, and it also provides carrier phase measurement accuracy of up to 0.5mm.

This paper makes a static measurement of the fixed position on the roof of the Yifu Building of Chongqing University of Posts and Telecommunications, and uses the precision positioning results of the OEM617D board as a reference to analyze the errors of the FPGA calculation results. Analysis of one of the received satellite data, where Figures 7, 8, and 9 are the Verilog calculations for ionospheric error correction, tropospheric error correction, and clock clock error correction, respectively, and Table 1 also shows the FPGA and Comparison of correction error results calculated by OEM617D boards.

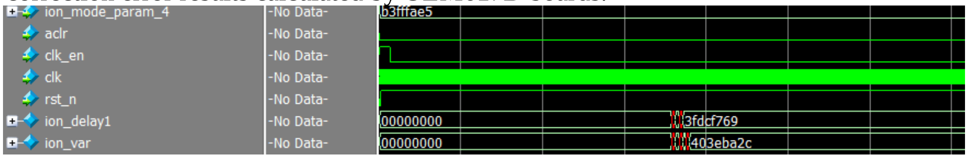

Fig. 5. Actual calculated value of ionospheric correction term in FPGA

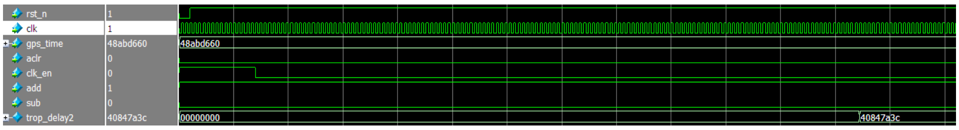

Fig. 6. Actual calculated value of tropospheric correction term in FPGA

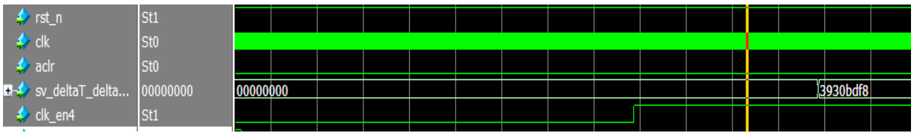

Fig. 7. Actual calculated value of clock clock offset correction term in FPGA

The error result calculated by FPGA is a single-precision floating-point number expressed by the IEEE754 standard. According to the calculation results given in Table 1, the ionospheric correction value, tropospheric correction value, and clock clock correction value calculated by FPGA and the OEM617D board error value are small, and the positioning requirements are not high Not much impact.

The least square method is a commonly used method to solve the nonlinear equations in the pseudo-range positioning algorithm, and judging the convergence of8 the final result is one of the important indicators to improve the precision of the pseudo-range positioning. This article determines whether the value x is as small as a preset value. Threshold to determine convergence. In section 4.2, the error correction items of the errors of the ephemeris data are analyzed and compared. It is found that the error of the result value calculated by the FPGA is small. Because this section will use the least squares solution, which involves mathematical iterations and matrix operations, this is the main cause of errors in FPGA calculation results. Figure 8 shows the FPGA implementation results of the Cholesky algorithm, and Figure 9 shows the actual calculation of the positioning results in the FPGA.

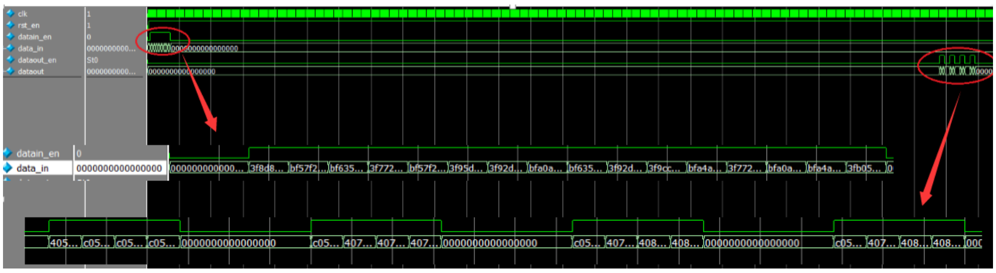
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Fig. 8. FPGA implementation of Cholesky algorithm

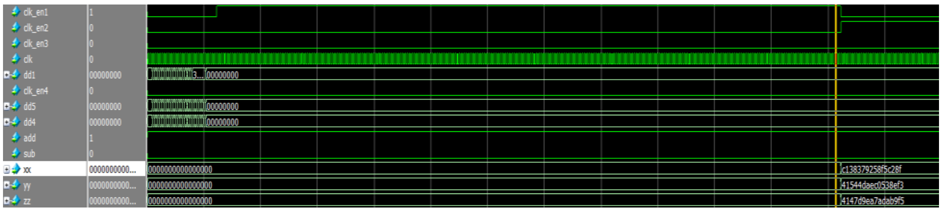

Fig. 9. The actual calculated value of the single-point positioning result in FPGA

Table 1 shows the comparison of the positioning results. In this paper, through static data analysis of 200 epochs, it can be found from the table that in the WGS-84 coordinate system, the error of the X axis is about 5m, and the error of the Y axis and the Z axis is about 2m. The main reasons for the error analysis are divided into two points. The first is because of the errors caused by the correction model used in the ionospheric error correction, tropospheric error correction, and clock correction. The second is that the NovAtel board output is the result of carrier phase double difference positioning. In this paper, pseudo-range data is used for positioning. Although the tedious solution process of the ambiguity is subtracted, there is a lack of accuracy.

Table 1. Comparative statistics of pseudo-range single-point positioning

	OEM617D board output value	FPGA actual calcu-lated value	Absolute error
X-axis of WGS-84 coordinate system(m)	-1587095.8437	-1587090.3475	5.4962
Y-axis of WGS-84 coordinate system(m)	5322424.3856	5322427.0051	2.6195
Z-axis of WGS-84 coordinate system(m)	3126226.1455	3126228.9598	2.8143

5 Concluding remarks

Pseudo-range single-point positioning technology has simple calculation steps and can achieve fast positioning, which has great application prospects in civil applications. This paper analyzes the basic principle of the pseudo-range single-point positioning algorithm, and selects an error correction model suitable for hardware implementation. When hardware resources allow, choose and improve algorithms such as CORDIC and Cholesky decomposition that are easy to implement in hardware to achieve complex arithmetic operations. Through Verilog programming and modelsin simulation, comparing FPGA and OEM617D board results shows that in the WGS-84 coordinate system, the error of the X axis is about 5m, and the error of the Y axis and the Z axis is about 2m.

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