High speed linear array CCD image data acquisition system based on machine learning

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Abstract: A high speed linear CCD (Charge Coupled Device) image data acquisition system based on machine learning was designed to solve the problem of poor signal stability of traditional high speed linear CCD image data acquisition system. Set up the overall system architecture. On this basis, complete the system hardware design through CCD sensor, A/D converter, CCD drive controller, RAM (Random Access Memory) read-write controller and PC; Through the CCD driver module, CCD signal processing module, image information reading module, image cache module, image information conversion mode and image information display module, the system software design was completed. Thus, the design of high-speed linear array CCD image data acquisition system based on machine learning was completed. Compared with the traditional high-speed linear CCD image data acquisition system, the experimental results show that the proposed high-speed linear CCD image data acquisition system based on machine learning has higher signal stability.

Key words: machine learning; CCD; Image data acquisition system;

1 Introduction

With the progress of science and technology, digital image acquisition and processing technology has been more and more applied in various fields. Traffic monitoring, dynamic target tracking and capture, robot navigation and other applications have also promoted the rapid development of real-time image processing technology. There are many methods to scan and identify the shape of high-speed moving objects. These methods firstly use CCD, CMOS (Complementary Metal Oxide Semiconductor) and other array photodetectors to image the objects, and then combine different data processing methods to process the collected images and store the data, so as to obtain relevant information of the measured objects [1-3]. With the advent of the information age, image sensors are increasingly used in scientific research and production. Among many image sensors and thermoelectric image sensors, CCD image sensor is widely used in high-precision measurement, detection, image analysis, spectrum detection and other fields for its excellent performance. CCD sensor has the characteristics of high precision, high resolution, stable performance, low power consumption, long life and self-scanning function, etc., and has been widely used in automatic and precise measurement [4-6].

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As a new artificial intelligence technology, machine learning algorithm can analyze and store massive data and make intelligent decisions on complex problems for reference of technicians. Machine learning algorithms can simulate the process of human thinking, learning and creation. Deep learning method is the latest method in the field of machine learning. Based on artificial neural network, this new feature learning method uses deep (multi-layer) neural network structure to build models. In combination with effective parameter adjustment and optimization methods, it has achieved very good data processing results [7]. This kind of machine learning model and algorithm with multi-layer network structure is called deep learning method.

Image recognition is an early application of deep learning and a major breakthrough has been made [8]. In deep learning approach, there is a model for a multidimensional data such as image pattern recognition has excellent performance, around the connection of multilayer neural networks, this structure makes it easier to training and has better generalization performance, this is the convolutional neural network, its main characteristic is the network structure contains a large amount of convolution and pooling layer, through multiple convolution and pooling layer overlay in turn, can carry on the step by step to the complex data of feature extraction, combined with abstraction, thus learn more conducive to classification of high-level character description.

Based on the above analysis, a high speed linear array CCD image data acquisition system based on machine learning is designed.

2 High speed linear array CCD image data acquisition system based on machine learning

2.1 Overall system architecture

The overall architecture of the high-speed linear array CCD image data acquisition system based on machine learning is shown in Figure 1.

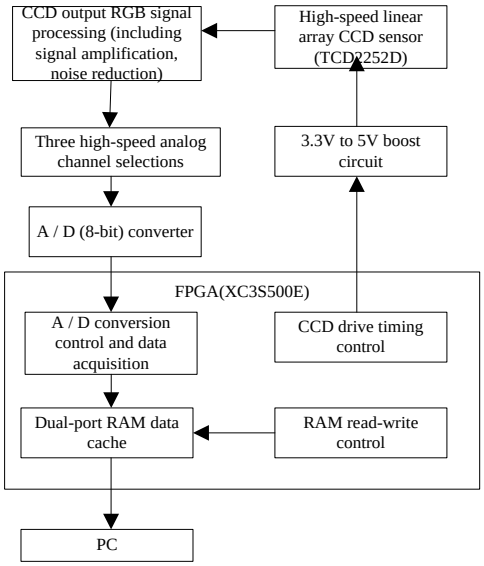

Fig. 1 Overall system architecture

According to the overall architecture of the system, the hardware part and software part of the system are designed.

2.2 System hardware design

The hardware design of high-speed linear array CCD image data acquisition system based on machine learning is shown in Figure 2.

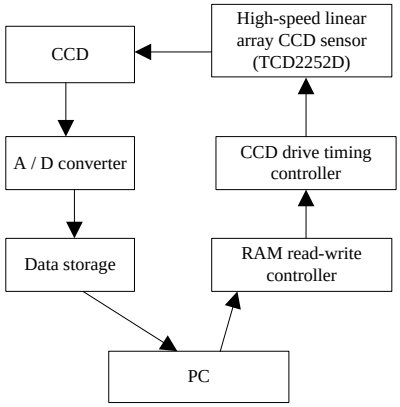

Fig. 2 Hardware structure of high-speed linear array CCD image data acquisition system based on machine learning

In the whole hardware system shown in Figure 2, firstly, the optical system images the detected object contour information on the image sensitive surface of the CCD, and the linear CCD receives the optical information from the front end and converts the optical signal into an

electrical signal that is convenient for processing [9-10]. Xilinx's FPGA (Field Programmable Gate Array) chip generates CCD driver timing pulses to generate, store, transfer and output the signal charge, and the light intensity distribution detected by the CCD will be reflected in the video signal output by the CCD. The output video signal of the linear tcd252d contains not only the effective charge signal, but also various noise clutter invalid signals. Three signal processing circuits are designed, including signal amplitude amplification, noise suppression and negative polarity reversal. Linear CCD outputs three parallel and independent analog video signals. A high-speed data acquisition system composed of three-channel high-speed analog channel selection, analog-digital conversion unit, dual-port RAM data cache unit, logic control unit and Xilinx integrated logic analyzer Chipscope Pro is designed to realize the acquisition, transmission and display of CCD output signals.

In the whole CCD data acquisition system, there is little need for FPGA I/O, and only the logical unit and block RAM storage capacity is required to meet the collected video data. Therefore, on the premise of meeting system requirements, low-cost chips are selected as far as possible. The FPGA used in this system is the low-cost XC3SSOOE programmable logic device of Xilinx company's spartan-3 E series. On-chip clock manager (DCM) provides advanced clock control functions for FPGA applications. Level standard: 4 I/O Banks, nuclear power voltage: 1.2v, port voltage: 3.3v, 2.5v, 1.2v; Support for 18 single-ended and differential I/O standards; Driving current up to 16mA; Support DDR storage interface, transmission rate can reach 622Mbit/s: support Xilinx Platform, BPI Flash(multi-boot), SPI Flash, JTAG configuration.

In order to make the light intensity of the object detected by CCD image better on the sensitive surface, it is necessary to add an optical lens or imaging objective lens in front of CCD to greatly improve the imaging quality. The imaging objective has a combination of fixed focal length, zoom, manual diaphragm and automatic diaphragm. In order to detect the object information, the user can calculate the focal length of the lens according to the distance and size of the detected object, so the appropriate CCD imaging objective lens should be selected according to the actual application environment. Image sensor is the core device of the whole image data acquisition system, which directly determines the performance of the system. TCD2252D is a kind of high sensitivity, low dark current three-wire, two-phase, double-channel color linear CCD camera device, with color filter inside, signal sharing, green and blue output, is a DIP22 packaging form of double-line directly inserted device. Each pin parameter setting is shown in Table 1.

Table 1 Pin parameter setting

Pin	Symbol	Function description	Pin	Symbol	Function description

number			number		
1	OS2	Signal output (blue)	12	SS	Ground
2	OS3	Signal output (red)	13	φ_{1A1}	Clock 1 (first phase)
3	SS	Ground	14	SH1	Transfer gate 1
4	NC	not connected	15	φ_{2A1}	Clock 1 (second phase)
5	$\overline{RS}$	Reset gate	16	V_{DD}	Power (digital)
6	φ_{2B}	Last stage clock (second phase)	17	φ_{1B}	Last stage clock (first phase)
7	SS	Ground	18	$\overline{CP}$	Clamp grid
8	φ_{2A2}	Clock 2 (second phase)	19	$\overline{SP}$	Track-and-hold
9	SH3	Transfer gate 3	20	OD	Power (analog)
10	φ_{1A2}	Clock 2 (first phase)	21	SS	Ground
11	SH2	Transfer gate 2	22	OS1	Signal output (green)

Inside the pin is a photosensitive diode containing 3 rows of 2700 effective pixels. The minimum pixel size is 8 m, the total length of the photosensitive array is 21.6mm, and the spacing between adjacent photosensitive columns is 64m. The device works under the condition of SV drive pulse and 12V power supply. The typical clock pulse frequency is 0.5mhz and the maximum drive frequency can reach 2MHz. At room temperature, typical sensitivity values of the three RGB arrays are 7.0v /lx·s, 9.1v/lx·s, and 3.2v/lx·s, respectively. The saturation exposure is 0.35lx·s. The typical saturation output voltage is 3.2V, which is composed of photodiode array, phase-shifting grid sh, two-phase CCD shift register, drive pulses (U 1, u 2) and output mechanism. In the camera area of the device, it has 2,700 effective photosensitive elements, carrying effective information, and 62 masked photodiodes are used to obtain dark current and other information for effective signal processing. D0-d12, which is not shown in the figure, is an imaginary unit, that is, no physical units exist, but there are 13 groups of corresponding units in the shift register. On both sides of the camera area are CCD shift registers, which are not sensitive to light, but only accept the transferred charge packet from the camera area and are separated from the photosensitive array. The two are

separated or communicated by the transfer pulse SH added to the transfer gate. At this point, complete the system hardware design.

2.3 System software design

On the basis of hardware facilities, the system software is designed. The software design diagram of high-speed linear array CCD image data acquisition system based on machine learning is shown in Figure 3.

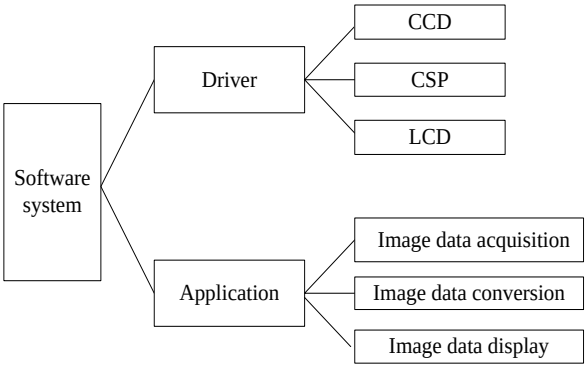

Fig. 3 System software block diagram

In the software system, the CCD driver module: the CCD module mainly realizes the image information collection and obtains the image simulation information. The CCD control driver performs this function by controlling and operating the CCD controller to drive the CCD chip. Since the main control logic of the CCD chip is implemented by the CCD controller, the CCD driver only needs to complete the simple initialization of the CCD controller. The initialization of CCD controller is divided into two aspects: sampling clock setting and moving pulse SH interrupt setting. CCD device converts charge signal into discrete voltage signal output, which includes a lot of noise from different places, including the noise caused by power supply and the noise generated in the acquisition process. The purpose of noise signal processing is to reduce noise and interference, improve signal-to-noise ratio, get high quality pixel signal and improve the detection accuracy. The output noise of CCD is analyzed and studied, and the analog signal of CCD output is denoised, and then the signal is output to ADS805 chip for analog-to-digital conversion. Uses a piece of drive to provide such a load current, using a transistor constant current source and op-amp composition, through the control the size of the output current in the collector of a transistor, according to the size of the R24 resistance to change the size of the transistor current to control the CCD output side of the collector is connected OS current, provide output signal OS need to load current.

CCD signal processing module: the output noise of CCD mainly consists of two parts, one is the noise generated by the photoelectric conversion inside the chip, and the other is the interference noise generated by the output process. Here are some common noises:

Firstly, granular noise. The process of the signal charge generated by the CCD device receiving the light is a random process. The signal charge generated by CCD device fluctuates up and down in a certain value in unit time, resulting in particle noise. However, in the actual use process, the scattered noise is inevitable, and can not be filtered out through subsequent improvement, so the scattered noise plays a decisive role in the size of the limit noise of CCD device.

Secondly, dark current noise. CCD devices can not receive photons or there is no other way to charge injection case, there will still be charge generation, thus forming a dark current, its generation process is also random. Dark current noise is mainly affected by temperature. For every 5-6 ℃ rise in temperature, the thermally excited noise will double. The existence of dark current noise reduces the dynamic range and sensitivity of CCD devices.

Thirdly, transfer noise. The transfer noise refers to the noise interference caused by the residual charge in the potential well transfer of the charge in the CCD potential well on the transmission of the next charge packet. Now the charge transfer efficiency of the CCD device is very high, basically reaching 99.99%, so the influence of the transfer noise on the signal noise can be ignored in general.

Fourthly, output noise. Output noise refers to the noise generated by the reset timing of the output circuit in the process of CCD photoelectric conversion. In the process of signal output, due to the reset pulse RST arrived ahead of schedule, the floating capacitor charging and discharging, waiting for the output charge transfer to the output side, in the case of CCD working frequency, capacitor charging and discharging speed to keep up with, cause incomplete discharge, which affects the output signal, the noise and called the reset noise, reset noise in the signal phase with reset signal is synchronized.

In view of the above noise, it is treated separately. CCD noise processing mainly deals with transfer noise and output noise. In order to suppress noise and interference, the following measures are taken:

In order to reduce the noise of DC power supply, two 10 frequency f and 0.1 frequency f filter capacitors are added to the input and output of the power supply, respectively, in order to reduce the noise generated during the transmission of DC power supply. In circuit design, the analog and digital ground is separated and connected by a single magnetic bead to reduce the interaction between digital noise and analog signal.

The simplest way to deal with the output noise is to use a low-pass filter for filtering. However, due to the limitation of its effect, the correlation double-sampling method is usually used to filter the output noise. Correlated double sampling is to like yuan signal sampling and reset noise, reset noise sampling is ahead of time, after the reset pulse signal pixels, sampling is in the charge packet arrival time, because the two sampling reset noise has always been there, in the two sampling results transformation, make a difference reset noise will be greatly weakened. When the CCD is reset, the clamping signal is set to a low level. When the CCD begins sampling, the output signal is kept at a low level for a short time before the CCD signal is output. The sampling clock of the box sampling method is related to the sampling interval of the CCD device and the phase of the reset signal, which makes the method more suitable for the processing of CCD output noise.

Image information reading module: in this module, the convolutional neural network degree in machine learning is used to extract image features. The multi-scale convolutional neural network is composed of three CNN model architectures in parallel. Each CNN model architecture consists of three stages. In the first two stages, a convolution kernel group is respectively included to generate a dense feature map, and a point-to-point nonlinear mapping is also included. In addition, after each feature map, a spatial pooling operation is connected for lower sampling. The final stage consists of only one set of convolution nuclei to produce the final set of feature graphs. The convolution kernel used in the model is also a weight matrix, which will be obtained by training. Each convolution kernel is applied to the input feature graph by using 2-dimensional convolution operation, and local features can be detected at all positions of the input. The convolution kernel groups vary as much as the input, but the rest of the network remains unchanged. The input of the multi-scale convolutional neural network is different images in the multi-scale pyramid, and the multi-scale hierarchical feature is expressed by connecting the output of all CNN networks f. A linear classifier is added to the model to learn the features and guide the training process of feature extraction, so that the multi-scale convolutional neural network can correctly predict the classification of all pixel positions in the image through the multi-scale hierarchical feature expression extracted after training. The sampling information reading program is mainly responsible for reading the image digital information output by CCD image processing chip. The image sampling information output by CSP chip AD9822 is written into the data cache module FIFO in high and low bytes. When the data stored in the cache reaches half of the cache capacity, the data cache module will notify the Nios II processor to read the data in the cache module by means of interrupt triggering through the output half-full control signal halffull. Therefore, image information reading is realized by FIFO interrupt processing.

Image cache module: Initialize the FIFO interrupt. The interrupt initialization of FIFO of cache module completes the two parts of interrupt initiation and interrupt registration. The interrupt open call function alt_irq_enble(AD9822_ALFFULL_IRQ), AD9822_HALFFULL_IRQ is the interrupt number allocated for the cached half-full signal.

In addition, the interrupt initialization of FIFO also calls the PIO register operation functions IOWR_ALTERA_AVALON_PIO_EDGE_CAP(AD9822_HALFFULL_BASE, 0x0) and IOWR_ALTERA_AVALON_PIO_IRQ_MASK(AD9822_HALFFULL_BASE,0xff) to clear the interrupt flag in the edge capture register and open the interrupt enable bit in the interrupt mask register. Interrupt registration call function Alt ir}register(AD9822_HALFFULL_IRQ, 0, handle_fifo_interrupt), where handle_fifo_interrupt is an interrupt service program that reads the cached image information in FIFO.

Then, through FIFO interrupt service program to realize the main program of image information reading. Figure 4 shows a flowchart of interrupt service program processing.

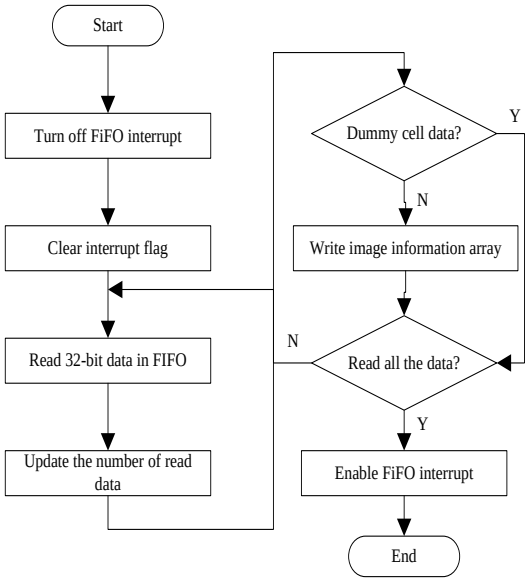

Fig. 4 Flow chart of interrupt service program processing

The FIFO interrupt handler first closes FIFO and clears the break flag to avoid nested calls to the FIFO interrupt service program. The image data in the FIFO is then read, four bytes at a time. In the process of reading, update the statistics of the read data, and determine whether the current data is a dummy unit, if so, discard it, otherwise write the globally defined image information array in order. When all valid data in FIFO are read out (28*4=1024 bytes),

the operation of image information reading is finished. Finally, start the FIFO half-full interrupt and exit the FIFO interrupt service program.

Image information conversion module: the main function of the image information processing program is to convert the read image data into LCD display format. When the CCD completes a round of image information collection, and the processor also transfers the effective image data to the image information array, the program will call the image information processing program to convert the data in the image information array. The conversion of image information data mainly considers the number of LCD horizontal or vertical display units and CCD effective image data. LCD adopts horizontal display to output the collected image data, so the number of display units per row is 320. Now it is necessary to output 10800 valid data collected by CCD to LCD display. In order to ensure uniform display of acquisition information, 320 pixel information is selected from 10800 valid data at an interval of 10800/32 points for display. After the data in the image information array is processed, it is stored in the global display information array.

Image information display module: image information display includes two parts: image statistics display and image data display. The image statistics display mainly displays the number of frames and the number of image data that have been collected. The image data display mainly transfers the data in the display information array to the LCD for display. Void LCD_Display_OneLine(unsigned char* lineLCDDate, int line), where lineLCDDate represents the starting address of the display row data, and line represents the line number displayed. The flowchart of its line display function is shown in Figure 5.

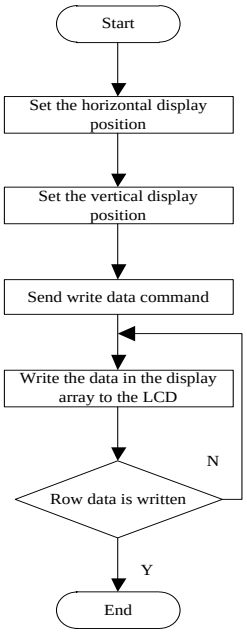

Fig. 5 Shows the flow chart of the function

Figure 5 describes the flow of the line display function LCD_isplay_OneLine(). Before writing data, the row display function first adjusts the current row/field display position, which is set to the line start address HSA set at initialization, and the field address to the line number line. After setting the display location, the row display function writes the lineLCDDate data in turn to the GDDRAM inside the LCD until it fills a line with hea-hsa +l. After displaying one line of sampled data, the image information display function will update the current line number, and wait for the next line to display the new display data after processing.

So far, according to the overall framework of the system, through hardware design and software design, the design of high-speed linear array CCD image data acquisition system based on machine learning is completed.

3 Experiment

The proposed high speed linear array CCD image data acquisition system based on machine learning is compared with the traditional high speed linear array CCD image data acquisition system to verify whether the proposed high speed linear array CCD image data acquisition system based on machine learning has more stable performance.

3.1 Experimental process

In order to ensure the reliability of the system drive signal, in addition to observing the simulation waveform, we should also check the actual output waveform in the oscilloscope.

Where, the actual driving signals of RS, CP and SP have the same frequency, and there is a certain phase difference between the three pulse signals, which conforms to the requirements of TCD2252D for these three driving signals. In general, the driving signals generated by FPGA all meet the requirements of TCD2252D for driving signals.

After debugging the system successfully, the stability of the signal of the proposed high-speed linear CCD image data acquisition system based on machine learning is compared with that of the traditional high-speed linear CCD image data acquisition system.

3.2 Analysis of experimental results

The signal stability comparison results of the proposed high-speed linear array CCD image data acquisition system based on machine learning and the traditional high-speed linear array CCD image data acquisition system are shown in Figure 6.

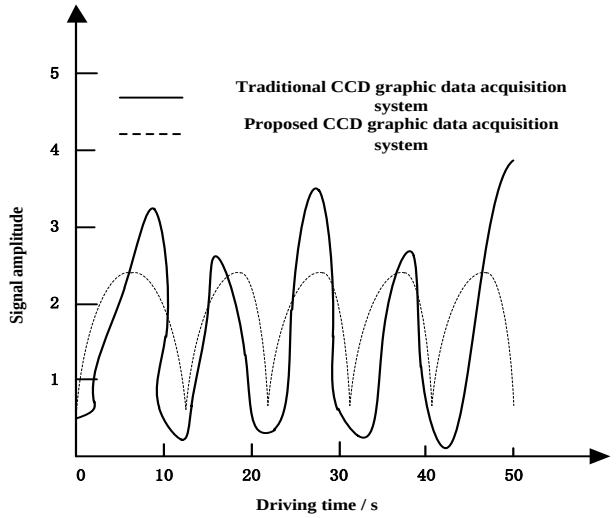

Fig. 6 Comparison results of signal stability

As can be seen from Figure 6, with the change of driving time, the fluctuation range of the signal amplitude of the traditional high-speed linear array CCD image data acquisition system is unstable, indicating that its signal is unstable. The wave amplitude of the high speed linear array CCD image data acquisition system based on machine learning is stable, indicating that the acquisition signal is stable. Through analysis, it is found that the proposed high-speed linear CCD image data acquisition system based on machine learning, based on machine learning, improves the system performance stability, compared with the traditional high-speed linear CCD image data acquisition system, its signal has higher stability.

4 Conclusions

A high speed linear array CCD image data acquisition system based on machine learning is designed to solve the problem of unstable acquisition signal in traditional high speed linear array CCD image data acquisition system. Compared with the traditional high-speed linear CCD image data acquisition system, the experimental results show that the signal stability of the proposed high-speed linear CCD image data acquisition system based on machine learning is higher, which is expected to provide certain reference value for the research of high-speed linear CCD image data acquisition system. However, there is still a long time for signal acquisition in this system. In the next research, we will focus on improving the acquisition system and improving the system efficiency.

5 Fund projects

science and technology plan of Qinghai province(Key Research&Development and conversion plans 2019-GX-170)

project name:Development of resource library of duixiu art Image digital protection in Huangzhong County, Qinghai Province

References

[1] Yiqian, C. Yang, X. Mingliang, W. et al.: Design and experimental study on online sowing quantity monitoring device of rapeseed drill seedmeter based on linear array CCD. Journal of Hunan Agricultural University(Natural Sciences). Vol. 45, no. 03, pp. 327-331 (2019)

[2] Weiwei, Z. Haiyan, L. Xiu, W. et al.: Experimental study on sub-pixel subdivision location of linear CCD based on gray weighted centroid algorithm. Optical Technique. Vol. 44, no. 04, pp. 476-479 (2018)

[3] Yuanjiong, L. Tongju, Z. Xingdong, W. et al.: High precision pose calibration method of multi-line camera system. Journal of Huazhong University of Science and Technology(Nature Science Edition, pp. Vol. 46, no. 11, pp. 81-86 (2018)

[4] Jian, Z. Mingyong, H. Min, L. et al.: Positioning method of dual wavelength laser focusing spot based on CCD image processing. Chinese Journal of Quantum Electronics. Vol. 36, no. 03, pp. 317-323 (2019)

[5] Suting, C. Ziye, G. Yanyan, Z.: Matching method of large array CCD aerial images based on local hashing learning. Journal of Applied Optics. Vol. 40, no. 02, pp. 259-264 (2018)

[6] Shaolin, L. Yongmei, W. Jinghua, M. et al.: Test for pixel non-uniformity of scientific optical CCD. Infrared and Laser Engineering. Vol. 48, no. 04, pp. 247-25 (2019)

[7] Fan, W. Jianguo, C. Yueming, G. et al.: Design of gene chip scanner based on LED induction and CCD collection. Journal of Electronic Measurement and Instrumentation. Vol. 32, no. 05, pp. 68-73 (2018)

[8] Youliang, Y. Aixu,L. Cuihong, M. et al.: Analysis of infrared temperature measurement model of

molten steel based on infrared CCD. Laser Technology. Vol. 42, no. 04, pp. 562-566 (2018)
[9] Zhibu, S. Limei, Q. Changjiong, X. et al.: Research on Combined Metrology System Based on CCD. Journal of Sanming University. Vol. 35, no. 02, pp. 56-62 (2018)
[10] Xiaofei, L.: Optimum Simulation of Power Consumption Information Collection Operation And Maintenance under Big Data Analysis. Computer Simulation. Vol. 35, no. 07, pp. 438-442 (2018)