The design of high speed multiplex data transmission system based on single chip microcomputer

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Abstract: In view of the high packet loss rate in the use of the original high-speed multi-channel data transmission system, the original data transmission system is optimized by using single-chip microcomputer, and the high-speed multi-channel data transmission system based on single-chip microcomputer is designed. The hardware of the main control chip, memory and data channel of the system is designed, and installed in the original system hardware framework to complete the hardware design of the system. According to the requirements of data transmission, data storage format and data source are set, and fuzzy processing calculation is used to complete data preprocessing. Construct data frame structure and complete data transmission. So far, the design of high-speed multi-channel data transmission system based on single chip microcomputer has been completed. By comparing the packet loss rate, it is verified that the designed system can effectively reduce the packet loss rate and improve the integrity of data transmission results.

Key words: Data acquisition; Singlechip; Data transmission; Data comparison;

1 Introduction

With the development of industry and agriculture, data transmission system has been widely used. In order to adapt to this trend, research in related fields is becoming more and more important. In scientific research, the use of data transmission system can obtain a large number of dynamic information, which is one of the important means to obtain scientific data and generate knowledge. No matter in which application field, data processing and transmission will directly affect work efficiency and economic benefits. Data transmission technology is a practical electronic technology. It is widely used in signal detection, signal processing, instrumentation and other fields. In recent years, with the continuous development of digital technology, data transmission technology also presents the development trend of faster speed, more channels and more data [1]. In the process of using the original data transmission system, the system often runs out of control due to the large amount of data information, resulting in the collapse of the data transmission system. In view of the above problems, a high-speed multi-channel data transmission system based on MCU is designed.

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Single chip microcomputer is short for single chip microcomputer, which has the characteristics of small size, high integration, fast calculation, economy, etc., so it is widely used in the fields of industrial automation, information collection, home appliance control, etc. In this design, single-chip microcomputer can effectively improve the data load capacity of the system and ensure the normal use of the system performance. Moreover, the single-sided machine is small in size and convenient in installation, which will not cause too much influence on the hardware framework of the system. This paper will be completed by two parts: first, the high-speed multi-channel transmission of information will be realized by single side computer; then, the performance difference between the original system and the designed system will be obtained by system test. Next, this paper will analyze and discuss the hardware design and software design of the high-speed multi-channel data transmission system of single chip microcomputer.

2 The hardware design of high speed multiplex data transmission system based on single chip microcomputer

The hardware design of the high-speed multi-channel data transmission system of single-chip microcomputer consists of three parts: the main chip design, the data channel hardware design and the memory design. In a strict sense, the design of data transmission hardware of single-chip microcomputer should be a system that can automatically detect or patrol the multi-channel data controlled by computer, and can store, process, analyze and calculate the data, and extract the available information from the detected data for display, recording, printing or description [2]. The whole data acquisition and transmission system is controlled by single chip microcomputer. The signal acquisition channel is selected through the control of channel data selection module and A/D conversion circuit module, so as to realize data acquisition and transmission. The system implementation block diagram is shown in Fig. 1.

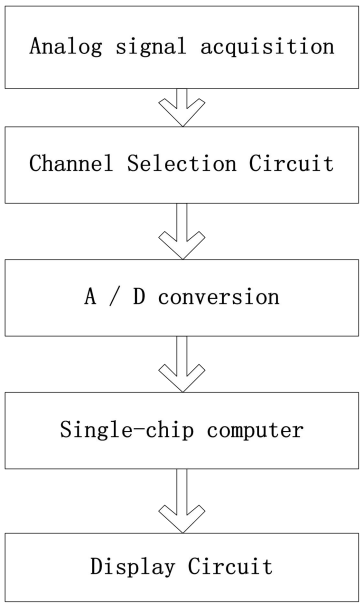

Fig. 1 Hardware design framework of high speed multiplex data transmission system

The above framework is used as the basis and control scheme of hardware framework design to ensure the order and controllability of hardware design and improve the process of system design.

2.1 Design of main control chip

The high-speed multiplex transmission system of single-chip microcomputer mentioned in this paper takes the acquisition and transmission of the relevant parameters of single-chip microcomputer as the main task and the single-chip microcomputer as the core controller. The overall structure of the system is shown in Fig. 2.

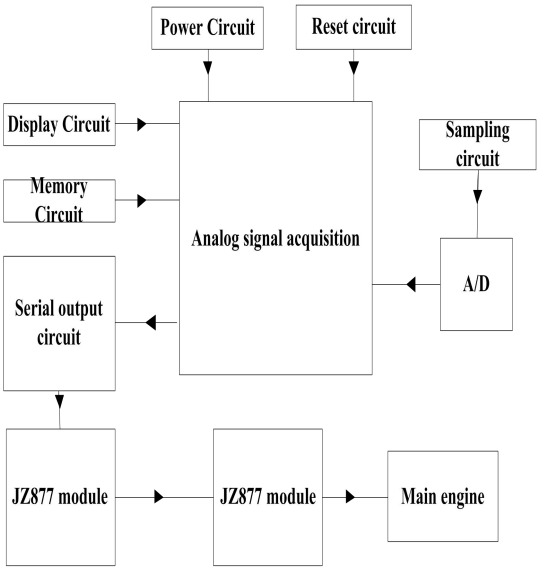

Fig. 2 The overall hardware structure of high speed multiplex data transmission system

There are many kinds and models of single-chip microcomputers available on the market, and the performance of single-chip microcomputers produced by each company is also different. According to the corresponding hardware requirements in this design, c8051f000 series single-chip microcomputers produced by Cygnal company are widely used, and the development tools are relatively perfect, and the product instruction systems of many companies are compatible with this. In addition to the choice of brand, we should consider the performance of SCM. In order to achieve high-speed multi-channel data transmission, the design uses a wide data bus to achieve the performance of the system [3]. The wider the known data bus width, the stronger the function. There are 4-bit computers, 8-bit computers, 16 bit computers and even 32-bit single chip computers. In order to ensure that the design system can run smoothly on the micro computer, 32-bit computer is more suitable. 32-bit computer has high cost performance in price and performance. Considering the internal resources of the single chip microcomputer, the basic units of the single chip microcomputer are as follows: central control unit (CPU), timer / counter, I / O interface, serial communication interface, interrupt response system, internal memory, data bus and address bus for system expansion, etc. [4]. Through the above settings, the design of the main control chip is completed. The specific main control chip is shown below.

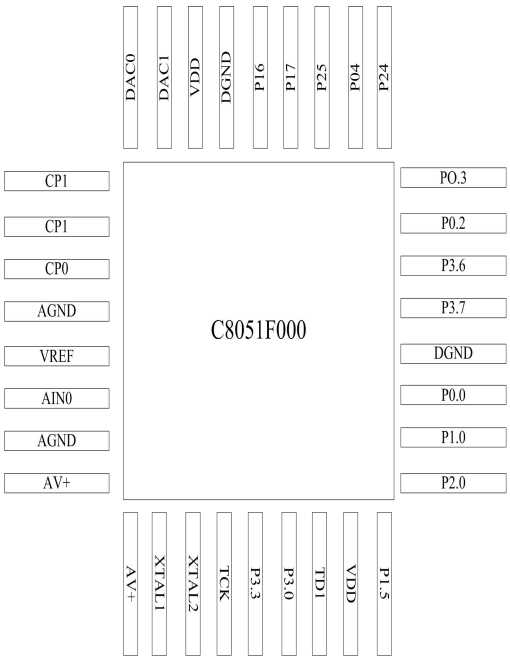

Fig. 3 Main control chip design results

The main control chip designed above is introduced to the control host of the original system, which is the hardware control center of this design.

2.2 Hardware design of data channel

In this article, the single-chip high-speed multiplexing system is designed to collect 32 data channels, while traditional single-chip microcomputers can collect up to 8 A/D signals. Select, then use the 74LS139 decoder as a chip selection of four 8-channel data selectors, and send the 32-channel data signals to the single-chip microcomputer for storage four times, and then analyze and process them [5]. In this way, the data of the 32-channel analog signals can be completely selected and collected by the single-chip microcomputer control, thereby performing high-speed multiplex transmission of the single-chip microcomputer. Data channel selection is shown in Fig. 4.

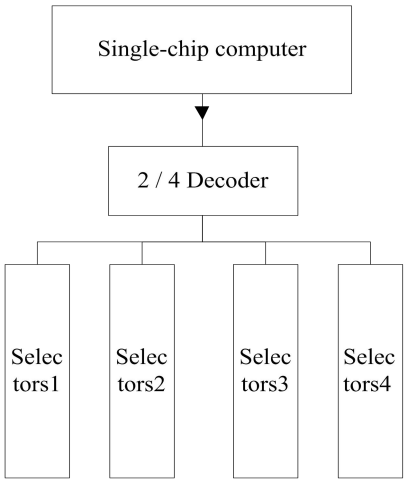

Fig. 4 System data channel selection structure

According to the above structure, the selection and design of the data channel hardware is completed, and it is connected to the main control chip.

2.3 Memory design

The function of data storage in this design system is mainly to temporarily store data, and it has the function of data caching. When the collected data reaches a certain amount, it will be transmitted to the upper computer at one time, which will help improve the data transmission efficiency and the efficiency of storage in the upper computer. All configurations in the memory are transmitted to the nRF905, SIP interface through the SPI interface, which can be set by the SPI instruction. When the nRF905 is in idle mode or shutdown mode, the SPI interface can remain in working state. 256 KB serial electrically erasable programmable read-only memory AT24C256 is used to control the information receiving port of the memory. Fig. 5 is the connection diagram of memory AT24C256 and 89C52P1 port.

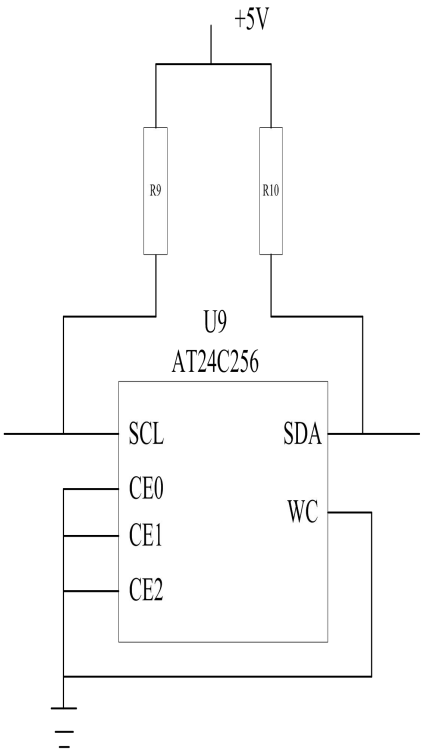

Fig. 5 Memory diagram

It can be seen from the image that this memory only occupies two I / 0 ports of the microcontroller. CEO, CE1 are address selection inputs, all are grounded, and WC is a write-protected input pin. When connected to ground, write operations are allowed [6]. SCL is a serial clock input pin, which is connected to P1.3 of 89C52. It writes SDA to the memory on its rising edge and reads out data and sends it to SDA on its falling edge. SDA is a bidirectional serial data input and output port. It is connected with P1.4 and exchanges data with the single-chip microcomputer. The figure above is a simplified diagram of the memory design. Through this diagram, the memory is connected to other hardware designed in the article and referenced to the original hardware framework. Then, the optimized hardware framework was used as the development environment for this software design.

3 System software design

In order to realize the use effect of the single-chip microcomputer in the high-speed multi-channel data transmission system, the software design part is divided into three links, which are data acquisition, data preprocessing, and data transmission. Data acquisition and data transmission are the program of the single-chip microcomputer sender and the program of

the upper computer receiver [7]. The program on the sender side mainly includes data collection and transmission, and the program on the receiver side mainly receives and processes the data, and realizes the high-speed data transmission performance of the system.

3.1 Data collection

In view of the problem that the packet loss rate of the original system is too high in use, the big data calculation is used to complete the data collection work and ensure the integrity and effectiveness of the data at the data source [8]. The collected data is stored in the designated database in the form of data table. In order to ensure the integrity of data in the transmission process, the same compression method can be used to expand the processing. The format of data table is set as follows.

Table 1 Data table format setting

Serial number	Field	Form
1	data sources	int
2	User name	varchar
3	User number	varchar
4	Data source No	varchar
5	Data acquisition equipment	varchar
6	Data collection time	varchar
7	Whether to deal with	varchar
8	Storage location	varchar
9	Usage situation	double
10	data type	double
11	Remarks	double

Use the above data table to sort out and store the collected data, so as to ensure the effective processing and transmission of the collected data.

3.2 Data preprocessing

Taking the collected data as the data base of the system design, the data can be integrated

into a variety of transmission formats through fuzzy algorithm.

According to the research on the calculation of multi-channel information transmission in Colleges and universities, the mean fuzzy algorithm combined with preprocessing criteria is used to complete the information processing process. Set the data information to be processed as matrix, name it as A, set the dimension of information vector as $B_i(i=1,2,...,n)$, and n as the number of vectors. After the data is initialized, it can be seen that the mean value area is Z_i, and then there are:

$$\sum_{i=1}^{A} Z_i = 1 \quad (1)$$

If the fuzzy center is o and the information number is m, then there are:

$$o_i = ((\sum_{i=1}^{A} Z_i)^m B_i) / ((\sum_{i=1}^{A} Z_i)^m) \quad (2)$$

The data information processing center is obtained by formula (2), and the data information processing is completed and the processing results are obtained by using this as the reference point. If the processing information is set as Q and P as the frame length of the image information, there are:

$$Q=\{(\frac{1}{P^2(B_i,o_i)})^{\frac{1}{m-1}}\}/\{\sum_{i=1}^{w}(\frac{1}{P^2(B_i,o_i)})^{\frac{1}{m-1}}\} \quad (3)$$

The collected information is calculated by the above set algorithm until the final value does not drop. This completes the process. In order to improve the efficiency of large-scale data processing, we set the data in advance and complete the convergence from the local to the center.

3.3 Set data frame structure to complete data transmission

After data pre-processing, the processed data is generated into a data frame structure as shown in Table 2. The main task of data transmission is to package the sampled data and set it to an appropriate format to complete the data transmission. Set the standard protocol to complete the communication channel setting during data transmission. The establishment of a standard protocol link usually results in excessive delay, and excessive feedback will increase the complexity of the interconnection between the two [9]. Therefore, in this design, the

high-speed multiplexing of data is realized by high-speed serial transmission between the analog-to-digital converter and the FPGA, and a unidirectional point-to-point serial differential transmission protocol based on SERDES is designed to realize the analog-to-digital on the same circuit board There are four channels between the converter and the FPGA, and the single-channel 4Gb / s serial transmission rate is set. The clock deviation between the two is not considered. The 8B / 10B codec is not selected. The system operating clock is set to .250MHz. Stream mode transmission, with data frames as the basic unit of the protocol [10]. The specific data frame structure is designed as follows.

Table 2 Data frame structure table

Serial number	structure	Field length
1	BIT[64:57]	Header (8 bit MSB first)
2	BIT[56:45]	Data1 (12 bit MSB first)
3	BIT[44:33]	Data2 (12 bit MSB first)
4	BIT[32:21]	Data3 (12 bit MSB first)
5	BIT[20:9]	Data4 (12 bit MSB first)

6	BIT[8:1]	ECC (8 bit MSB first)

With the above settings, the data is encapsulated into frames, so that the receiver can correctly identify the start and end of data transmission, so as to control and detect the data transmission and facilitate the expansion of protocol functions. In response to the requirements of this article, the content of the protocol needs to be defined: synchronization sequence, data frame structure. The synchronization sequence is used to synchronize the system between the high-speed ADC and FPGA. The data frame consists of the frame header (SF), data (D), and frame end (EF). The line code stream for designing a custom protocol is shown below.

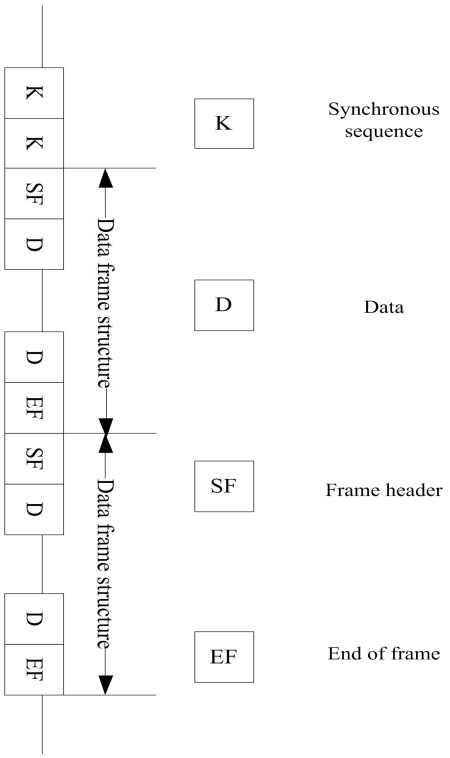

Fig. 6 Schematic diagram of the line code of the custom protocol

The line code stream of the custom protocol is used to complete the efficient multiplexing of data. The above software modules are combined with the hardware designed in this paper. So far, the design of high-speed multi-channel data transmission system based on single chip microcomputer has been completed.

4 Data acquisition system test

Combined with the above hardware design results and software module design, the design of high-speed multi-channel data transmission system based on single chip microcomputer is completed. In order to ensure the effectiveness of the design, the test link of the construction system is used to compare the performance difference between the original encryption and decryption system and the encryption and decryption system designed in this paper.

4.1 Design of system test platform

In order to verify the performance difference between the design system and the original system, the design system and the original transmission system are tested in the same platform. The experimental environment is set up by two parts, namely, hardware environment configuration and software environment configuration.

Hardware environment configuration: Intel CPU series chip, frequency is 6.0GHz, memory capacity is 20.00GB, hard disk is 2TB.

Software environment configuration: The experiment uses SQL software design, the programming environment is SQL2013, and the test environment is configured as a 64-bit Windows 10 operating system.

According to the above hardware and software, the experimental environment is established, and the experimental object is set as the packet loss rate in the transmission process. The set data test sample is shown below.

Table 3 System test sample

Test sample No	Sample data volume	Data form
1	500	TEXT
2	1000	TEXT
3	2500	TEXT
4	5000	TEXT
5	10000	TEXT

Using the above system test samples, the calculation process of the packet loss rate of the original system and the designed system is completed.

4.2 Analysis of test results

Through the above design, the system test process is completed, and the specific system test results are as follows.

Table 4 Comparison of system test results

Test sample	Packet loss	Packet loss

No	rate of original system/%	rate of the system designed in this paper/%
1	5.23	2.15
2	6.45	2.20
3	6.24	2.56
4	6.30	3.04
5	5.68	2.15

According to the above experimental results, the packet loss rate of the designed system is significantly lower than that of the original system. The highest packet loss rate of the designed system is 3.04%, and the lowest packet loss rate of the original system is 5.23%. Through the data comparison, we can intuitively feel that the design system in this paper is obviously superior to the original system. At the same time, compared with the original system in the same amount of data, the transmission speed of the designed system is faster. Therefore, the transmission performance of the designed system is better than the original system. In conclusion, the design system is better than the original system.

5 Concluding remarks

The high-speed multi-channel data transmission system introduced in this paper can collect, analyze, process and transmit multi-channel data signals in real time. Compared with the traditional data acquisition system, it not only records the multi-channel acquisition data, but also records the sampling time. It overcomes the shortcomings of the traditional data acquisition system, such as unable to record the sampling time, inconvenient to display and analyze the data, and it is conducive to the user to accurately understand and grasp the status of the transmission process. The hardware and software structure of the system is reasonable. It can collect and transmit parameters, and display the collected data in real time. After simulation debugging, the error of acquisition parameters of the system is within the design requirements, the system is stable and reliable, the operation process is easy to grasp, the acquisition accuracy and speed meet the actual use requirements, with high practical value. It gives full play to the advantages of single chip microcomputer, such as powerful function, high reliability, good flexibility, easy development and easy expansion. On the basis of the system introduced in this paper, users can expand the data processing and analysis part on the single-chip microcomputer according to the actual needs, increase the corresponding output channel, thus increasing more practical application functions. Because this paper does not consider the data security problem in the process of data transmission, in the future research

will focus on the data encryption method to ensure the security of data transmission.

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