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Comparative Study on Power Gating Techniques for Lower Power Delay Product, Smaller Power Loss, Faster Wakeup Time.

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Abstract

The power gating is one of the most popular reduction leakage techniques. We make comparison among various power gating schemes in terms of power delay product, energy loss, and wake-up time using the 45-nm Predictive Technology Model. In my conclusion, the Dual-Switch Power Gating (DSPG) shows lower power delay product, smaller energy loss, faster wake-up time than the other power gating schemes such as the Single-Switch and Charge-Recycled Power Gating schemes. Based on these advantages, the DSPG is suggested in this paper as a viable candidate suitable to a fine-grain leakage control scheme, where logic blocks go in and out very frequently and shortly between the active and sleep modes.

Keywords: low-leakage; power gating; sleep transistor; fine-grain leakage control; crossover time; wake-up time.

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1. Introduction

As CMOS size continues to be scaled, transistor density increases, and power consumption becomes a very important constraint in very-large-scale integration (VLSI) design. Power dissipation comes from two sources including static power and dynamic power. Dynamic power is calculated when system is in active mode. The static component is power as no signals are changing their value. The dynamic power consists of switching power and short circuit power. Switching power is caused by charging and discharging of load capacitance. Short circuit power is caused by charging of internal nodes. The main sources of static power are sub-threshold leakage, gate leakage, gate induced drain leakage, oxide tunneling and junction leakage [1]. As device scaling goes on, these leakage current sources are more and more increasing that is as much as a third of total power [2].

The leakage current is particularly important in mobile devices, where the battery lifetime is decided by their leakage during sleep time. To mitigate the leakage current, a number of low-leakage techniques have been developed for many years [3-6]. Among them, power gating techniques have been used widely for many years, where leakage current can be cut off by an NMOS header or PMOS footer with high threshold voltage [7]. At wake-up moment, the header or footer that was off, becomes turned on, and a logic block powered by the header or footer goes to an active mode from a sleep mode.

The new power gating schemes with charge recycling technique have been introduced [8-9] where an amount of switching energy which should be lost in turning on and off power switches can be lowered. This energy saving comes from the charge sharing which happens between a virtual V_{DD} and V_{SS} lines, at both a sleep-in and wake-up moment. Here, virtual V_{DD} and V_{SS} lines are connected to real power supply and ground supply through the PMOS switch and NMOS switch, respectively. When the sleep time is very

short, however, the charge-recycled power gating can lose more energy than the conventional power gating schemes without charge sharing. Moreover, the charge-recycled power gating needs more time in equalizing its virtual V_{DD} and V_{SS} lines. Thereby, its wake-up time is longer. This large energy loss and slow wake-up may prevent the charge-recycled power gating from being used particularly in a fine-grain leakage control scheme, where the logic blocks go in and out between the active and sleep modes very frequently and shortly.

Thus, the sleep time of fine-grain leakage control scheme is likely much shorter than a coarse-grain leakage suppression scheme [10-12]. To be useful in the fine-grain leakage reduction scheme, a power gating circuit should be able to awake the logic block as fast as possible at the wake-up moment [13-14]. And, also, an energy loss due to this power gating has to be as small as possible.

Recently, dual power gating has been re-visited in results of low leakage consumption compared to the conventional power gating and the charge recycling power gating (CRPG) with same timing constraint [15]. Here, three schemes are analysed in scenario of 10% or 20% timing overhead. We can realize that to make the same timing constraint, overhead switch area of dual power gating technique should increase four times compared to the conventional power gating and charge recycling power gating at least. It means that cost will be increased in case of dual power gating to achieve lower leakage consumption in high speed applications. In term of low cost, low leakage consumption, the dual power gating is analysed by comparison with the other two schemes in this paper. A solution with low cost, low power delay product, fast wake-up time and small energy loss consumption in a reasonable speed can be very helpful in applying this technique, for example, in wireless sensor network systems.

In this paper, we extend my work to prove more advantage of the proposed leakage reduction technique [16]. We continue to compare three power gating schemes which are the Single-Switch Power Gating (SSPG) which can be regarded as the conventional power gating technique, Charge-Recycled Power Gating (CRPG) [8-9], and Dual-Switch Power Gating (DSPG), respectively, in terms of energy loss due to power gating, power delay product, wake-up time, so on. The comparison tells us that the DSPG has the lowest energy loss regardless of how long the sleep time is, among 3 schemes. Moreover, the DSPG can wake up faster than the CRPG because it does not need any more time in charge sharing. And, we need to mention the ground bounce noise which becomes more significant with supply voltage being scaled down, as IR drop and di/dt noise that are introduced by abrupt change of virtual power lines increase [17]. The ground bounce noise in the DSPG has been known better than the other two due to its small voltage swing and small rush current on power lines [17-18]. Based on the comparison, we suggest in this paper that the DSPG with smaller energy loss, smaller power delay product and faster wake-up is more suitable to the fine-grain leakage control scheme than the others. Thus, this paper shows the advantages of DSPG than the others and based on these advantages, we suggest the DSPG as a viable candidate suitable to the fine-grain leakage control scheme.

2. Various power gating schemes

Figures 1(a), (b), and (c) show 3 power gating schemes which are the SSPG, CRPG, and DSPG, respectively. Firstly, Figure 1(a) illustrates the SSPG scheme that has two logic blocks, L_0 and L_1, which are made of low threshold voltage (low V_{TH}) transistors with large leakage current. To cut off the leakage during the sleep time, the L_0 and L_1 are powered by the header, MP_0 and the footer, MN_0, respectively, which are made of high threshold voltage (high V_{TH}) transistors. Here the V_{SSV} and V_{DDV} are virtual V_{SS} and V_{DD} lines, respectively, which are connected to real V_{SS} and V_{DD} line when the header and footer are turned on. On the contrary, when the MP_0 and MN_0 are off, the V_{SSV} is raised up to V_{DD} and V_{DDV} is lowered to V_{SS}. Here, the PGN and PGP mean enable signals for the MN_0 and MP_0, respectively. Figure 1(b) shows the CRPG scheme, where the V_{SSV} and V_{DDV} which are controlled by the MN_0 and MP_0, respectively, are connected each other through the MN_1 and MP_1 that constitute a transmission gate. This transmission gate is turned-on at both sleep-in and wake-up moments in which charges are shared each other between the V_{SSV} and V_{DDV}. The TGN and TGP turn on the transmission gate at both the sleep-in and wake-up. The DSPG is shown in Figure 1(c), where the L_0 and L_1 are powered by both the header, MP_0 and footer, MN_0. To cut off leakage, both the header and footer need to be off simultaneously.

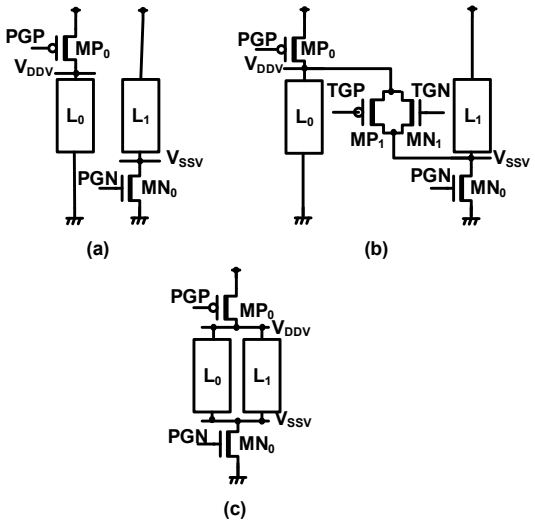

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Figure 1. (a) The Single-Switch Power Gating (SSPG) scheme (b) The Charge-Recycled Power Gating (CRPG) scheme (c) The Dual-Switch Power Gating (DSPG) scheme.

Figure 2 compares the V_{SSV} and V_{DDV} waveforms of 3 schemes. Here, the sleep-in and wake-up happen at the t_0 and t_3, respectively, and the t_{sleep} means the sleep time. The PGN is a control signal for the footer and the TGN is a control signal for the transmission gate in the CRPG.

At the both sleep-in and wake-up, the transmission gate should be turned on for a short time of the t_1-t_0 and the t_3-t_2, as shown in Figure 2. We can see the V_{DDV} of SSPG, firstly. When the sleep time is long in Figure 2, the V_{DDV} has a voltage swing as large as the ΔV_0 at the wake-up time of t_3.

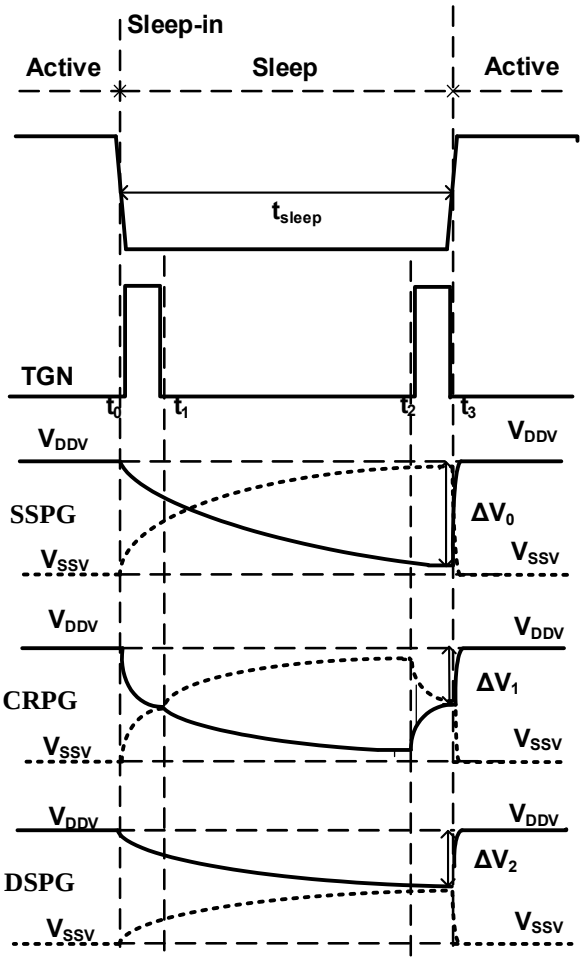

Figure 2. Waveforms of the SSPG, CRPG, and DSPG when a sleep time is long.

Thus, the SSPG loses a large amount of switching energy at this moment. When a sleep time is short, ΔV_0 has a small voltage swing, thus SSPG only loses a small amount of switching energy at this wakeup moment. Next, for the CRPG, the V_{SSV} and V_{DDV} are equalized during the t_1-t_0, then, they start to decay toward the real V_{DD} and V_{SS}, respectively. The V_{SSV} and V_{DDV} are equalized again during the t_3-t_2, and they are restored to the real V_{SS} and V_{DD} at the t_3, respectively. At time of t_3, the CRPG in Figure 2 has a voltage swing as large as the ΔV_1 on its V_{DDV}. Comparing the CRPG with the SSPG, we can realize that the CRPG has larger voltage swing on its V_{DDV} than the SSPG at the wake-up when the sleep time is short. It means that the CRPG is not effective in saving energy when the sleep time is short. Unlike the SSPG, the ΔV_1 of CRPG are almost the same regardless of the sleep time. This is because that the V_{DDV} and V_{SSV} of CRPG are equalized every the sleep-in and wake-up moment, thus their voltage swings being about half V_{DD} regardless of the sleep time.

Finally, the DSPG is considered, its V_{DDV} swing is as small as the ΔV_2. With a short sleep time, the DSPG's swing voltage is like the SSPG. When a sleep time becomes longer, the ΔV_2 becomes larger but it does not exceed half V_{DD} unlike the SSPG. For this long sleep time, its voltage swing is almost the same with the ΔV_1, of the CRPG.

3. Simulation results

Figure 3 shows analysis results of 31-stage ring oscillator at temperature of 27°C. The simulation is done using the 45-nm Predictive Technology Model (PTM) [19] with various voltage supplies. Here, the DSPG uses both PMOS and NMOS switches to cut off power lines, thus drop voltage on these switches is a little bit larger than SSPG which uses only NMOS switch. Consequently, delay of DSPG is slightly higher than that of SSPG as shown in Figure 3 (a). However, power delay product is a metric related to efficiency energy measuring energy consumed per switching event. The power delay product of DSPG is 7% smaller than that of SSPG as shown in Figure 3 (b) indicating that the DSPG has higher energy efficiency even in the active mode.

Figure 4(a) shows the comparison of 3 schemes in terms of energy loss. The logic block used here is composed of 50% INVs, 25% NANDs, and 25% NORs. Here the power switch's channel width used in this paper is 10% of the total channel width of logic block. The power-gating energy loss is defined by an amount of energy which is lost between the sleep-in and wake-up moment. For a certain sleep time, if the energy loss due to power gating is smaller than the active leakage energy which is expected to dissipate during the sleep time, we can save some amount of energy using power gating scheme. On the contrary, if the energy loss is larger than the active leakage energy, we had better not to use the power gating. A sleep time when the energy loss of power gating becomes the same with the active leakage energy is defined as a crossover time. This crossover time is very important when we try to apply a power gating technique to the fine-grain leakage control circuits, where

logic blocks are subject to transit between the active and sleep modes very frequently and shortly. In Figure 4(a), when the sleep time is short, the SSPG needs power-gating energy loss smaller than the CRPG. As mentioned earlier, this is due to that the SSPG has smaller voltage swings on its V_{DDV} and V_{SSV} than the CRPG when its sleep time is short. As the sleep time becomes longer, the CRPG begins to have smaller voltage swings on the V_{DDV} and V_{SSV} than the SSPG thus needing smaller energy loss of power gating thereby some amount of energy being able to be saved.

Among these 3 schemes, the DSPG shows the smallest power-gating energy loss when a sleep time is either short or long. For the short sleep time, the V_{DDV} and V_{SSV} of DSPG change as small as the SSPG thus minimizing its energy loss as small as the SSPG. Comparing with the CRPG, the DSPG can reduce the energy loss by 85% for the sleep time=10ns and 27°C. And, for the long sleep time=10µs, the DSPG can save 30% than the SSPG. This saving is caused from that the V_{DDV} and V_{SSV} swing of DSPG is only about half of the swing of SSPG, as shown in Figure 2. One more thing to

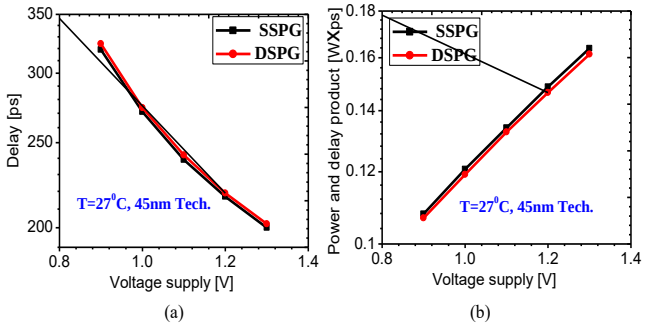

Figure 3: A 31-stage ring oscillator (a) delay vs. voltage supply (b) power and delay product vs. voltage supply.

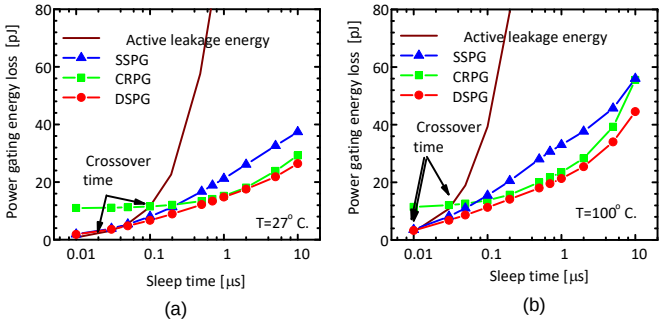

Figure 4. (a) Power gating energy loss comparison of the SSPG, CRPG, and DSPG with varying a sleep time at 27°C using the 45-nm PTM, V_{DD}=1.1 V, and W_{PG}/W_{Logic}=10% (b) Energy loss comparison of the SSPG, CRPG, and DSPG at 100°C.

note is that the DSPG does not lose any amount of energy in equalizing the V_{DDV} and V_{SSV} thereby being able to save more energy than the CRPG, as shown in Figure 4(a). The crossover time can be extracted from Figure 4(a). The SSPG, CRPG, and DSPG have 35ns, 100ns, and 30ns, respectively. Figure 4(b) shows the energy loss of power gating at a temperature of 100°C. Comparing Figures 4(a) with (b), we can notice that the crossover times of 100°C are shorter than those of 27°C.This is because sub-threshold leakage at 100°C is larger.

One more concern in the CRPG is an equalizing time which is defined by the t_1-t_0 and t_3-t_2 in Figures 2. The CRPG needs this time for the transmission gate to equalize the V_{DDV} and V_{SSV} resulting in a longer wake-up time than the SSPG and DSPG. If this equalizing time is not long enough to equalize the V_{SSV} and V_{DDV} fully, an amount of energy loss of the CRPG can be increased. Figure 5(a) shows that the power gating energy loss can be changed in the CRPG with varying the equalizing time. When the equalizing time becomes shorter, the CRPG has larger energy loss. For the SSPG and DSPG, their energy loss has nothing to do with the equalizing time. To achieve the energy loss as low as around 30pJ, the equalizing time should be longer than 250ps. This equalizing time is added to the wake-up time. This slow wake-up may prevent the CRPG from being used in a fine-grain leakage control scheme, where a short wake-up time is demanded not to degrade the active-mode performance. Figure 5(b) compares

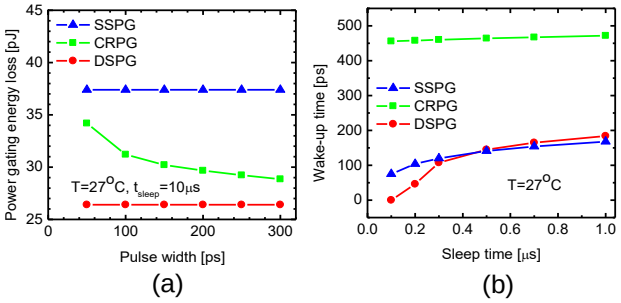

Figure. 5. (a) Power gating energy loss vice versa pulse width of the TGN using the 45-nm PTM, V_{DD}=1.1 V, W_{PG}/W_{Logic}=10%, and t_{sleep} =10µs. From this figure, we can notice that power gating energy loss of the CRPG begins to saturate when the pulse width becomes as long as 250ps. (b) Wake-up time vice versa sleep time for the SSPG, CRPG, and DSPG using the 45-nm PTM, V_{DD}=1.1 V, and W_{PG}/W_{Logic}=10% than 27°C thus the crossover time being much shorter than 27°C.In Figure 4(b), the SSPG, CRPG, and DSPG have the crossover times of 17ns, 35ns, and 12ns, respectively, indicating that the DSPG can be the most suitable to the fine-grain leakage control demanding a short crossover time.

the wake-up times of SSPG, CRPG, and DSPG with varying a sleep time. As expected, the wake-up time of CRPG is the longest among 3 schemes due to the equalizing time. For the SSPG and DSPG, their wake-up times become longer and saturate with a sleep time increasing. Here the wake-up time is defined by a time when the V_{SSV} and V_{DDV} are restored to 90% of their final values of V_{SS} and V_{DD}. We also investigated the layout overhead of SSPG, CRPG, and DSPG. The SSPG and DSPG have the same layout area as long as their power switches have the same size. The CRPG, however, needs a larger area for its transmission gate as shown in Figure 1(b). To equalize the V_{DDV} and V_{SSV} in a short time, we need to increase the width of MP_1 and MN_1 in Figure 1(b) more thereby the area overhead being larger.

Table 1: 32-bit input vectors applied to the 32-bit carry-look-ahead adder.

Input Vector	Input A	Input B
V_0	00000000	00000000
V_1	00000000	FFFFFFFF
V_2	FFFFFFFF	00000000
V_3	0000FFFF	0000FFFF
V_4	0000FFFF	FFFFFFFF
V_5	FFFFFFFF	FFFFFFFF

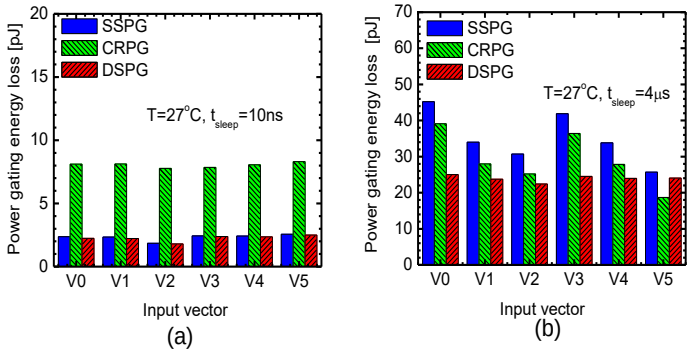

Figure 6. (a) Power-gating energy loss of the 32-bit Carry-Look-Ahead adder when the sleep time is as short as 10ns for the 45-nm PTM, V_{DD}=1.1 V, and W_{PG}/W_{Logic}=10%. The DSPG consumes almost the same energy with the SSPG, but its energy loss is much smaller than the CRPG by as much as 72% on average. This result is consistent with Figure 4(a). (b) Power-gating energy loss of the 32-bit Carry-Look-Ahead adder when the sleep time is as long as 4µs. The DSPG consumes smaller energy than the SSPG and CRPG by as much as 32% and 18% on average, respectively. As expected from Figure 2, the SSPG and DSPG show the largest and smallest energy loss, respectively.

In this paper, the width of the transmission gate in Figure 1(b) is half of the width of power switches, thus the area penalty of CRPG being as large as 15% compared with the penalty of SSPG and DSPG as small as 10%.

The three power gating schemes are applied to a 32-bit Carry-Look-Ahead (CLA) adder to compare the energy loss due to power gating. The 32-bit adder is implemented using the 45-nm PTM, at V_{DD}=1.1V and 27°C. Figures 6(a) and (b) show the energy loss of 32-bit CLA adder when a sleep time is 10ns and 4µs, respectively. The simulated input vectors of 32-bit adder are shown in Table 1. In Figures 6(a) for the sleep time=10ns, the CRPG shows the largest energy consumption which is caused by the $\Delta V_{1,S}$ larger than the SSPG and DSPG, respectively. From this figure, the SSPG, CRPG, and DSPG have average energy loss of 2.3pJ, 8pJ, and 2.25pJ, respectively. When the sleep time is as long as 4µs, the SSPG seems to lose the energy on average as much as 35.2pJ compared with the CRPG of 29.2pJ and DSPG of 23.9pJ. Among 3 schemes, the DSPG loses the smallest energy for its power gating, making the DSPG the most suitable to the fine-grain leakage controlled VLSIs.

ISCAS-85 Benchmark circuits, that are C432, C449 and C880, are verified to show that DSPG is better than others in term of leakage power consumption. The normalized leakage power is compared at 27°C and 100°C as shown in Table 2 and Table 3 respectively.

Table 2: Comparison the normalized leakage power loss in ISCAS-85 benchmark circuits when sleep time is from 0.01µs to 5µs at 27°C.

Sleep time (µs)	C432			C499			C880		
	SSPG	CRPG	DSPG	SSPG	CRPG	DSPG	SSPG	CRPG	DSPG
0.01	1.04	11.76	1	1.05	16	1	1.05	12.15	1
0.1	1.12	1.65	1	1.14	1.66	1	1.14	1.62	1
1	1.37	1.11	1	1.44	1.14	1	1.41	1.1	1
5	1.56	1.16	1	1.58	1.004	1	1.55	1.34	1

Table 3: Comparison the normalize leakage power loss in ISCAS-85 benchmark circuits when sleep time is from 0.01µs to 5µs at 100°C.

Sleep time (µs)	C432			C499			C880		
	SSPG	CRPG	DSPG	SSPG	CRPG	DSPG	SSPG	CRPG	DSPG
0.01	1.05	4.22	1	1.05	5.22	1	1.05	4.21	1
0.1	1.2	1.21	1	1.24	1.22	1	1.23	1.19	1
1	1.53	1.2	1	1.49	1.14	1	1.47	1.13	1
5	1.65	1.38	1	1.43	1.1	1	1.56	1.49	1

4. Conclusion

Among various power gating technique, we have compared 3 power gating schemes in terms of power delay product, energy loss, wake-up time using the 45-nm Predictive Technology Model. The comparison results show that the DSPG is smaller energy loss, lower power delay product, faster wake-up time than the other power gating schemes. Based on these advantages, we suggest the DSPG as a viable candidate suitable to a fine-grain leakage control scheme, where logic blocks go in and out very frequently and shortly between the active and sleep modes.

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