Mismatch Analysis and Calibration Techniques in Modern CMOS: From Current Mirror to SAR ADC

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Abstract. This paper systematically reviews the mismatch response framework from underlying physical principles to upper-level system architecture. The study first analyzes the mismatch mechanism based on the Pelgrom model, then explores the impact of threshold voltage mismatch in the current mirror on the output current, and the mismatch problem between the capacitor array and the dynamic comparator in SAR ADC. The paper focuses on reviewing the evolution of calibration techniques, including chopper stabilization, dynamic component matching, digital pre-distortion, noise shaping, and the latest machine learning-assisted calibration technologies. Research shows that the design approach of co-designing digital algorithms and circuits can more effectively suppress mismatch compared to traditional pure circuit design, offering significant advantages in cost and flexibility. However, it still faces challenges in terms of increased circuit complexity in the analog domain and computational resource consumption in the digital domain.

Keywords: Analog integrated circuits, Device mismatch, Current mirror, SAR ADC, Digital calibration.

1. Introduction

In the continuous advancement of semiconductor manufacturing processes towards submicron and nanometer nodes, integrated circuit design is facing unprecedented physical challenges. Although the miniaturization of chip size has greatly improved the computing speed and integration scale of digital circuits, for analog circuits that are highly dependent on the precise proportional matching between devices, the evolution of the process has instead caused more serious performance deviation problems. The root cause of this phenomenon is the discrete effect of the statistical characteristics of micro-particles. In the early long-channel process, due to the large number of impurity atoms inside, its electrical performance follows the law of large numbers, and the statistical error is effectively averaged on a macroscopic level, with negligible impact on circuit accuracy. However, when the transistor size is miniaturized to the nanometer scale, the total number of impurity atoms in the channel is drastically reduced, causing random

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doping fluctuations and line edge roughness to evolve from minor perturbations into decisive factors that determine device characteristics[1]. This miniaturization of geometric size directly exacerbates the non-uniformity of electrical parameters, such as threshold voltage in spatial distribution, causing analog circuit design to lose its original deterministic basis, forcing designers to seek a path to build a reliable signal processing system in the face of extremely strong uncertainty. This shift from deterministic design to statistical design is the core of the current focus of academia and industry on mismatch analysis and calibration techniques. Regarding solutions to mismatch problems, academia is undergoing a profound transformation from physical hardware compensation to digital algorithm collaboration. Early research was mainly based on the Pelgrom model [2], which believes that mismatch is mainly caused by the randomness of manufacturing process and tends to increase device area at the expense of bandwidth and cost in order to achieve matching accuracy. However, as processes entering the nanoscale era, mainstream research pointed out that due to the increasing complexity of short-channel and stress effects, the traditional strategy of simply increasing area not only had weakened returns but also introduced huge parasitic capacitances and increased chip costs, making it unsustainable in modern high-speed, low-voltage designs [3]. Therefore, contemporary research has shifted towards utilizing inexpensive and efficient computing power under advanced processes to assist in solving analog mismatch problems. The technological path has evolved from initial physical layout optimization such as common centroid placement, pseudo-cell technology, circuit-level automatic zeroing, and correlated double sampling technology[4], to advanced algorithms such as dynamic component matching, digital predistortion, and noise shaping. The latest research results have begun to introduce machine learning, and use more advanced algorithms to perform blind calibration of complex nonlinear mismatches, which has shown great potential in terms of cost, flexibility and long-term stability. In order to systematically address the mismatch problem under modern technology, study aims to establish a complete analysis framework from the underlying physical mechanism to the upper system architecture, and to conduct a comprehensive review of the mismatch problem under modern technology. This paper adopts a progressive analysis logic: First, the most basic current mirror mismatch problem in analog circuits is taken as the starting point of the research. In-depth analysis of its current mirror mismatch correction principle is an important prerequisite for understanding the accuracy bottleneck of most complex back-end circuits. Subsequently, the research focus will be extended to SAR ADC. SAR ADC is not only the preferred solution for modern Internet of Things and wireless communication, but also a representative of active comparator mismatch and passive capacitor array mismatch due to its accuracy matching degree with DAC capacitor array and input offset voltage of dynamic comparator[5]. The goal of study is to explore how to achieve a balance between high precision, high speed and low power consumption in advanced process technologies by comparing various optimization methods such as front-end and back-end calibration, error shaping and on-chip sorting algorithms, so as to provide theoretical and technical support for the future shift to a new design approach which combines digital algorithms and circuits.

2. Optimization of current mirror and DAC mismatch

2.1 Chopper stabilization and dynamic element matching

Kyeongsik Nam and others have combined chopper stabilization with dynamic element matching [6] and have used it to improve current mirrors in transimpedance amplifiers and control amplifiers. Chopper stabilization works by modulating low-frequency noise into high frequencies which are then filtered by a low-pass filter to minimize input-referred noise. Conversely, dynamic element matching is used in gain-enhanced cascode current mirrors in which errors caused by process mismatches are reduced by periodically switching and averaging transistor arrays. The novelty of this technique is that the same 125 kHz frequency can be used as both the chopper clock and the DEM clock, thus eliminating the intermodulation distortion due to harmonic interactions between square waves of different frequencies. The experimental findings show that this design does not only guarantee the quality of the signal, but allows using a low-pass filter with a higher cutoff frequency, which leads to the reduction of input reference noise and economy of chip area.

2.2 Non-binary weighting and digital predistortion

Ramin Babaee et al. presented one solution to combine non-binary weight design with digital predistortion [7]. Conventional current-steering DACs operate on integer weights, which makes it hard to attain optimal error distribution when it comes to random mismatches. The originality of this approach would be the introduction of statistically optimized non-binary weights, which, in combination with digital pre-distortion, mathematically minimizes the effect of amplitude mismatch-induced nonlinearity and partially reduces timing errors. The tests prove that this approach is effective in improving DAC linearity, and offers a different design paradigm than traditional binary weights in terms of mismatch optimization in high-speed current-steering DACs.

2.3 Nearest-value-substitution and digital pre-distortion

In order to eliminate the random mismatch of current sources in a high-speed DAC, Lulu Wang et al. suggested a nearest-valued substitution digital pre-distortion scheme. Most of the conventional methods tend to use fixed calibrations or averaging schemes that cannot be optimized to perform optimally in real time conditions of operation. The novelty of this approach lies in measuring the actual values of mismatch of each current cell in advance and storing them in a LUT. At runtime, these combinations are dynamically selected by the digital logic to select the current source combination with the minimum mismatch error to synthesize the output based on the input codeword. This real-time optimal matching technique[8] is very effective in suppressing nonlinear errors caused by random mismatches, increases the spurious-free dynamic range of the DAC, and is adaptable in nature to work at high speeds.

3. Mismatch mitigation strategies for SAR ADC

To address the distortion and noise issues caused by capacitor mismatch in high-resolution SAR ADC, Chen Wang et al. [9] proposed a system-level solution centered on error shaping. Its key innovation lies in transforming the traditional approach of relying on high-precision matching

or complex background calibration into actively reconstructing the mismatch error spectrum through a collaborative mechanism of Mismatch Error Shaping (MES) and digital prediction compensation. Specifically, the authors introduced MES into the second-order noise-shaping SAR loop, which modulates and pushes the nonlinear error caused by DAC capacitor mismatch out of band, and reducing in-band distortion from a mechanism perspective. In response to the input range loss caused by MES, a digital prediction method was proposed for compensation in advance, thereby restoring the dynamic range without additional simulation calibration. The essential innovation of this combination is realizing mismatch noiseification and reversible digital domain compensation, avoiding strong dependence on high-precision capacitor matching. In terms of power consumption and implementation complexity, the paper further proposes a Coarse Fine Comparison (CFC) strategy, which decomposes the high power consumption problem of multi-input dynamic comparators into two stages: coarse decision and fine decision. While maintaining the noise shaping function, the comparator power consumption is significantly reduced. At the same time, a completely asynchronous control logic is adopted, which only relies on the sampling clock to drive the entire SAR and NS loop, eliminating the power consumption and timing pressure brought by the traditional high-speed external clock. The experimental results show that the ADC achieves 81.54 dB SNDR (13.25 bit ENOB) with OSR=25 and 100 kHz bandwidth, and the total power consumption is about 305 μW [9], proving that high resolution performance can be obtained without analog calibration. This work strongly demonstrates important trends that compared to simply improving capacitor matching accuracy, shifting the mismatch error spectrum out of band via MES is a more effective approach for high-resolution SAR ADC; and that digital prediction can effectively compensate the signal swing loss caused by error shaping and by combining CFC and fully asynchronous control, noise-shaped SAR can achieve high ENOB without incurring significant power consumption costs. In conclusion, this design demonstrates a mismatch-tolerant paradigm with error shaping as its core and digital assistance as its support, providing a representative systematic path for the subsequent implementation of high-precision, low-power SAR ADC in weakly matched processes.

To address the non-monotonicity and linearity degradation caused by capacitor mismatch in high-resolution SAR ADC, Hua Fan et al. [10] proposed a mismatch tolerance scheme based on bubble sorting. Unlike traditional methods that rely on high-precision capacitor matching or complex analog background calibration, this work shifts the focus from avoiding mismatch to reconstructing mismatch errors in the digital domain". Its core innovation lies in introducing bubble sorting logic on-chip to reorder the capacitor array weights online, thereby restoring the monotonicity and effective weight accuracy of the DAC at the system level. Essentially, this is an approach that transforms static component mismatch into a digitally processable sorting problem, significantly reducing the dependence on absolute capacitor matching accuracy. Specifically, the authors detect bubble codes in the sub-DAC output and perform digital reordering, so that the code sequence error caused by capacitor mismatch is corrected in realtime in the digital domain without introducing additional analog calibration loops or high-precision reference adjustment. The key value of this method lies in two aspects.Firstly, it can directly address the monotonicity failure problem, which is the most sensitive issue for SAR ADC; secondly, the digital implementation has good process scalability and low power consumption characteristics. Test results show that the linearity of the ADC is significantly improved after bubble sorting calibration, and achieved high-resolution performance, verifying the effectiveness and engineering feasibility of this method in high-precision SAR architectures.

This work further reinforces an important trend in modern SAR ADC design: improving the system's tolerance to analog mismatch through digital post-processing. Compared to methods that rely solely on capacitance matching or analog background calibration, bubble sorting technology achieves direct repair of non-monotonic errors with lower complexity, making it particularly suitable for situations where capacitance matching continuously deteriorates under deep submicron processes. Meanwhile, this scheme is mainly designed for static weight sorting errors and has limited ability to suppress random noise or dynamic mismatch. In high dynamic accuracy applications, it still needs to be used in conjunction with other error shaping or calibration techniques.

To address the performance degradation caused by device mismatch and PVT fluctuations in high-speed pipelined-SAR ADC, Chao Wu et al. [11] proposed a structure and calibration co-optimization scheme. Its core innovation is not a single circuit technique, but rather actively weakening the influence path of mismatch through system architecture reconstruction.First, the authors introduced a split-capacitor loop-unrolled architecture in the first-stage SAR and physically separated the SAR sampling array from the MDAC sampling array, so that the SAR capacitance scale was changed from noise constraint to matching constraint, thereby reducing the dynamic weight error caused by top plate parasitism and comparator load coupling from the source.Experimental and simulation results show that this structure can shorten the DAC setup time by about 60%, effectively alleviating the non-ideal effects amplified by parasitism and mismatch during high-speed operation. Second, to address the long-standing bottleneck of the open-loop MDAC being extremely sensitive to PVT, the authors proposed a gain compensation mechanism based on DAC capacitance ratio adjustment, which transfers the amplifier gain error that is difficult to control precisely into a digitally adjustable capacitance ratio error, thereby achieving low-complexity foreground calibration. After calibration, the system THD improved from −58.2 dB to −76.4 dB, and the SNDR increased to 63.55 dB (10.26 bit ENOB) [11], indicating that the overall linearity bottleneck is indeed due to compensable gain error rather than uncontrollable noise sources. In addition, to address the potential mismatch of the dual-path time constant introduced by capacitor array separation, a 1-bit redundant window is used in the design to provide a fault tolerance space of $\leqslant 0.5$ LSB, avoiding excessive reliance on absolute matching accuracy.In summary, this work demonstrates that in high-speed SAR ADC, through the synergistic strategy of structural desensitization, adjustable parameter calibration, and redundancy fault tolerance, stable suppression of mismatch can be achieved with lower power consumption. Compared with the method of simply relying on high-precision capacitor matching or complex background calibration,it achieves a better balance between speed, energy efficiency, and feasibility.

To address the linearity degradation problem caused by capacitor mismatch and comparator non-ideals in medium-to-high resolution SAR ADC, He Yu et al. [12]proposed a digitally assisted compensation scheme centered on capacitor weight self-calibration. The key innovation of this work lies in reconstructing the traditional mismatch calibration process, which requires numerous iterations or external processing resources, into an on-chip, independently operable error quantization and weight correction mechanism. Specifically, the design quantizes the MDAC capacitor mismatch voltage by introducing a matched CDAC structure, and uses the proposed sign-aware two’s complement mapper to directly map the quantization result into a standard compensation code that can participate in digital computation, thereby achieving fast weight correction without multiple rounds of iteration. This approach essentially transforms the

problem of absolute capacitor accuracy into a problem of digital weight update, improving calibration convergence efficiency and area utilization while maintaining structural simplicity. At the circuit level, the authors further combined a three-segment capacitor array with a baseboard sampling strategy to reduce array size and input-related charge injection errors. The segmented structure reduces the total capacitance to approximately 1.2% of that of traditional arrays[12], alleviating the nonlinear stress caused by process mismatch and parasitics at the source. Simultaneously, a dynamic comparator with OOS is employed to compress the equivalent input offset to approximately 202 μV, reducing the limitation of comparator offset on high-resolution conversion. These measures complement digital self-calibration: the front-end structure reduces the error amplitude, while the back-end algorithm performs fine correction. Experimental results clearly demonstrate the effectiveness of this method. Under 0.18 μm CMOS and 3 MS/s conditions, the uncalibrated ADC exhibited a SNDR of 59.44 dB and an ENOB of 9.58 bits[12], with a significant S-shaped mismatch in INL. After introducing self-calibration, the SNDR improved to 72.09 dB and the ENOB reached 11.68 bits, with the maximum DNL/INL improving to 0.42 LSB/0.54 LSB[12], significantly restoring linearity and monotonicity. More importantly, the calibration module area occupied only about 30%, significantly lower than some solutions that require external LMS or large-scale digital resources, verifying its high area efficiency. This work demonstrates that in medium-speed, medium-precision SAR ADC, high linearity can be recovered without over-reliance on capacitance matching by directly measuring and digitally compensating for capacitance weight errors. Secondly, symbol-aware two's complement mapping provides a low-complexity data path implementation for on-chip self-calibration, enabling calibration results to be seamlessly embedded into the normal conversion process. Furthermore, structural desensitization, such as segmented arrays, base plate sampling, OOS comparison, and digital self-calibration, are designed in a collaborative manner that is more engineering-efficient than simply relying on optimization of either side. Overall, this design demonstrates a high area-efficiency mismatch compensation path for resource-constrained SoCs, but it mainly targets static capacitance weighting errors and has limited support for dynamic mismatch and noise shaping requirements in high-speed scenarios. Therefore, it is more suitable for applications of medium-speed, high-precision SAR ADC.

To address the nonlinear performance degradation caused by multiple non-idealities in high-speed SAR ADCs, Sumukh Bhanushali et al. [13] proposed a circuits-informed supervised machine-learning technique for blind open-loop digital calibration. Unlike conventional calibration schemes that require individual error sources, such as capacitor mismatch, comparator offset, sampling noise, or reference ripple, to be identified and modeled separately, this method learns the overall conversion error directly from the input-output behavior of the ADC. In this context, “blind” means that the calibration algorithm does not require prior knowledge or explicit mathematical modeling of the internal error mechanisms, rather than indicating an unsupervised or reference-free learning process. The core innovation of this work lies in using a low-speed reference ADC to train a shallow two-layer neural network. When the sampling instants of the high-speed ADC and the reference ADC coincide, their digital outputs are compared to generate supervised training data. The trained neural network then estimates the conversion error of the high-speed ADC, and the estimated error is subtracted from its output in the digital back-end. Because the reference ADC operates at a substantially lower sampling rate, it is only required to provide intermittent reference samples and does not need to process every high-speed conversion result, thereby reducing the speed and power requirements of the

reference channel. Experimental results based on a 28 nm, 12-bit, 84 MHz SAR ADC show that the proposed neural-network calibration improves the SFDR by more than 38 dB while consuming approximately 25.8 fJ per conversion step [13]. These results demonstrate that a compact machine-learning model can compensate for the combined effects of several interacting ADC non-idealities without separately estimating every physical mismatch parameter. Compared with calibration methods based on fixed analytical models or single-error correction, this scheme provides greater flexibility in learning complex nonlinear error behavior and can be implemented as an open-loop digital back-end without modifying the normal SAR conversion loop. However, the method still requires a sufficiently accurate low-speed reference ADC and representative aligned samples for supervised training. Its performance also depends on the quality of the reference data and the ability of the trained neural network to track variations caused by process, supply voltage, temperature, and device aging. Therefore, circuits-informed machine-learning calibration provides a promising approach for improving the robustness of high-speed SAR ADCs, although further optimization is required to reduce reference-channel overhead, support continuous adaptation, and minimize the area and power consumption of the digital inference hardware.

4. Limitations and future prospects

Current research on device mismatch analysis and calibration techniques still faces multiple limitations and shortcomings. At the technical implementation level, analog domain calibration schemes mostly require the design of complex auxiliary circuits, which not only significantly increases chip area overhead and consumes valuable voltage margin, but also easily introduces additional clock phase, noise aliasing and timing errors. While digital domain calibration schemes have cost and flexibility advantages under advanced processes, they still inevitably consume on-chip computing resources and are not suitable for low-power, resource-constrained edge scenarios. At the theoretical modeling level, existing research has not yet established a quantifiable, universal mathematical model for device mismatch adapted to advanced process nodes, which can easily lead to over-design or yield losses in analog integrated circuit design. In terms of research universality and engineering application, current mainstream technologies are mostly designed and verified based on specific process nodes such as 180nm and 65nm, exhibiting strong process dependence and making direct migration to more advanced process nodes difficult. Furthermore, existing research largely focuses on the performance improvements brought about by mismatch calibration, lacking systematic quantitative analysis and comprehensive consideration of the impact on the power consumption of the calibration circuit itself, calibration convergence time, chip mass production yield, and energy efficiency optimization throughout the system's lifecycle.

In response to the continuous miniaturization trend of semiconductor processes, future research on device mismatch analysis and calibration technology will advance in three main directions: theoretical modeling, technology optimization, and engineering implementation. Firstly, this paper suggest deepening the research on the microscopic mechanisms of device mismatch at advanced process nodes, constructing quantifiable mathematical models of mismatch that adapt to nanoscale effects such as short-channel effects, random doping fluctuations, and line edge roughness, correcting and overcoming the accuracy limitations of traditional Pelgrom models, and providing accurate theoretical support for analog circuit design. Secondly, researchers

recommend continuing to promote the in-depth optimization of the co-design paradigm of digital algorithms and analog circuits. While reducing the computational overhead in the digital domain, researchers should focus on developing low-power, fast-convergence on-chip self-calibration, mismatch error shaping and noise shaping fusion technologies, deepen the research on intelligent blind calibration algorithms that combine circuit prior constraints and machine learning, solve the core problems of nonlinear mismatch modeling, labelless parameter estimation and real-time performance balance, and further expand the applicable boundaries of calibration technology in high-speed, high-resolution complex analog systems. Finally, study recommend strengthening the engineering application research of mismatch calibration technology, establishing a comprehensive evaluation system that considers calibration performance, chip area, power efficiency, and mass production yield, and quantitatively analyzing the impact of calibration schemes on the system's full-cycle energy consumption and yield. This will promote the efficient transformation of theoretical research results into practical industrial applications.

5. Conclusion

This paper systematically explores the physical mechanism of device mismatch in nanoscale CMOS technology and its evolution path in current mirrors and SAR ADCs.It constructs a complete framework from low-level statistical characteristic analysis to high-level digital-assisted calibration. The research shows that as semiconductor technology moves into the nanometer node, random doping fluctuations and line edge roughness have replaced geometry as the main factors determining matching accuracy. This has caused the traditional strategy of relying on increasing device area to satisfy the Pelgrom model to lose the balance between performance gain and chip cost. Through in-depth analysis of chopper stabilization, dynamic component matching, digital predistortion, and mismatch error shaping techniques, this paper confirms that the focus of calibration has shifted from early pure analog domain hardware compensation to digital algorithm co-design. In particular, cutting-edge methods such as noise shaping and machine learning-assisted calibration can significantly improve the system's SNDR and ENOB while effectively mitigating linearity degradation caused by process deviations. The significance of this study is clarifying the technical necessity of shifting from deterministic design to statistical mismatch-tolerant design, and providing a theoretical basis and system-level solution for realizing high-performance analog integrated circuits under weakly matched processes. Looking forward, research should focus on establishing quantifiable mismatch mathematical models adapted to nanoscale effects, and further exploring how to achieve multi-dimensional synergistic optimization of calibration algorithm convergence speed, energy efficiency, and mass production yield in resource-constrained scenarios. The design approach of trading area for matching faces the dual challenges of physical limits and performance costs at advanced process nodes, urgently requiring a shift towards new design approaches that combine digital algorithms and circuit collaboration. Calibration technology is undergoing a profound transformation from analog domain compensation, such as chopping and automatic zeroing, to digital domain intelligent correction, such as lookup tables, dynamic matching, noise shaping, and the latest machine learning. The latter, with the high computing power provided by advanced processes, has shown great potential in terms of cost, flexibility, and stability, especially in the typical application scenario of SAR ADC, the combined effects of capacitor

array mismatch and comparator mismatch can be effectively suppressed through front-end calibration, back-end calibration, error shaping, and on-chip intelligent algorithms, such as the aforementioned bubble sort and neural networks, allowing a balance between high precision, high speed, and low power consumption at higher process nodes. Further research will focus on establishing quantifiable mathematical models that adapt to the nanoscale effects of advanced processes, and exploring in depth how intelligent calibration algorithms can further optimize the yield and energy efficiency of the entire system lifecycle and meanwhile reducing digital computing overhead.

Authors contribution

All the authors contributed equally and their names were listed in alphabetical order.

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