Analysis of Performance-Influencing Factors and Optimization Strategies for Single-Stage Amplifiers

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Abstract. When semiconductor technology scales down steadily, single-stage amplifiers have significant difficulties in optimizing performance because of short-channel effects and parasitic parameters. This paper thoroughly looks into the important physical mechanisms constraining amplifier gain, with a focus on channel length modulation (CLM), the body effect, and the Miller effect. The study first finds out the theoretical effect of these factors on voltage gain, linearity, and bandwidth. To overcome these limitations, advanced device architectures like Gate-All-Around (GAA) and Fully Depleted Silicon-On-Insulator (FD-SOI) are studied, using their better electrostatic control to suppress CLM and the body effect. Precisely, a Cascode structure making use of active feedback (transistor T2) is proposed to remove the Miller effect. The research reveals that the combination of advanced process nodes and optimized circuit topologies is crucial for getting high gain and high bandwidth performance in modern analog integrated circuits.

Keywords: Effect, Parasitic Capacitance, Optimization Strategies .

1 Introduction

In modern electronic systems, single-stage amplifiers work as crucial elements at the front - end or core of signal chains. They are in charge of amplifying weak signals and doing signal conditioning. MOS transistors are the mainstream core devices for single-stage amplifiers as a result of their high input impedance, low static power consumption, easy adaptation to CMOS processes, and good thermal stability. They find wide application in precision measurement, radio frequency communication, medical electronics, industrial control, and portable smart devices. For precision measurement systems, MOS transistor amplifiers are needed to get distortion-free amplification of microvolt-level sensor signals. For radio frequency communication front-ends, the bandwidth and noise performance of MOS transistor amplifiers directly bear on signal reception sensitivity. Portable devices need low power consumption to make their battery life longer. For example, by taking up a single-acousto-optic single-stage amplification hybrid dual-channel scheme and using polarization separation, the problem of pulse envelope modulation caused by the interference of frequency-shifted light with different

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modulation frequencies in single-acousto-optic dual-channel transmission is effectively quelled [1].

As performance requirements become ever-more stringent, traditional bulk silicon processes and planar device architectures come across bottlenecks because of physical limitations. To conquer this difficulty, the academic and industrial fields are actively finding advanced solutions built on new device structures and process nodes. At the device physics level, Gate-All-Around (GAA) technology, which offers 360° superior electrostatic control, has become the mainstream way to suppress short-channel effects (like channel length modulation), effectively solving the output impedance degradation problem at the nanoscale. In the meantime, Fully Depleted Silicon-On-Insulator (FD-SOI) technology makes use of an ultra-thin silicon film and buried oxide layer to physically disconnect the body region from the substrate, presenting an ideal solution for getting rid of threshold voltage drift due to body effects. Furthermore, at the circuit topology level, to address bandwidth limitations induced by the Miller effect in high-frequency applications, the introduction of cascode structures or active feedback networks to disrupt the Miller multiplication mechanism has emerged as a key technological trend for enhancing the bandwidth and stability of transimpedance amplifiers.[2]

The intention of this paper is to comprehensively look into the crucial physical mechanisms influencing the gain of single-stage amplifiers and find corresponding optimization and improvement solutions. The study first theoretically works out the specific ways that channel length modulation (CLM), body effect, Miller effect, and parasitic capacitance affect amplifier gain, linearity, and bandwidth. Then, by using advanced Gate-All-Around (GAA) and Fully Depleted Silicon-On-Insulator (FD-SOI) device models in combination, the study verifies through simulation the considerable advantages of these new structures in suppressing short-channel and body effects. By comparing the circuit performance differences between traditional bulk silicon processes and advanced process nodes, this paper proposes a comprehensive circuit improvement scheme, aiming to achieve collaborative optimization of single-stage amplifier gain and bandwidth while ensuring low power consumption, providing a theoretical basis and practical reference for the design of high-performance analog integrated circuits.

2 Channel length modulation

When a MOSFET is in the saturation region, the effective channel length Leff shortens as the drain - source voltage VDS rises because the depletion region at the drain end expands. Once VDS is greater than VGS after subtracting VTH, the channel goes through "pinch-off" at the drain end. When VDS keeps rising, the pinch-off point moves a little bit in the direction of the source. This shortens the actual conductive channel length ΔL, so the drain current ID varies as the voltage changes. [3]

In the low - frequency small - signal analysis of a common-source amplifier, it find that the voltage gain Av is given as $Av = -gm \cdot Rout$. Rout is often the parallel combination of the load resistance (say RD or ro2) and the MOSFET's own output resistance ro. When the channel modulation effect is not considered, the MOSFET in the saturation region can be regarded as an ideal current source with a constant ID, leading to an infinite ro. But, on account of the variation of the drain current ID with voltage, the output resistance ro becomes finite. According to what the parallel resistance formula states:

$$\frac{1}{R_{\text{out}}} = \frac{1}{R_{\text{load}}} + \frac{1}{r_o} \tag{1}$$

When the total resistance goes down, the gain goes down too. Core formula:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2}$$

$$r_o = \frac{1}{\lambda I_D} \tag{3}$$

2.1 Analysis of improvement schemes

With semiconductor process nodes moving into the sub-3nm scale, traditional Fin-shaped Field-Effect Transistors (FinFETs) are faced with notable challenges due to their limited electrostatic characteristics. Since FinFETs can surround the channel from just three sides, they face problems in maintaining sufficient gate control as gate lengths keep getting shorter and shorter. Because of this physical limitation, Short Channel Effects (SCE) show a dramatic deterioration. And Channel Length Modulation (CLM) becomes a critical constraint on device output impedance and analog circuit gain. To overcome this technological difficulty, Gate-All-Around (GAA) technology, especially Multi-Bridge Channel Field-Effect Transistors (MBCFETs), has been made the widely - used device architecture for the post-FinFET [4]

2.2 Physical nature along with challenges of channel length modulation effect

The main mechanism of CLM consists of the no-ideal invasion of the drain electric field into the channel barrier. In traditional MOSFETs, when the drain-source voltage (VDS) rises, the drain depletion region expands towards the source, leading to an unanticipated decrease in the effective channel length. It makes the drain current (ID) increase linearly with the change of voltage in the saturation region. In analog circuits, this directly makes the transistor output impedance (ro) go down, seriously degrading the voltage gain (Av = gm·ro) of single-stage amplifiers. Even if FinFETs improve gate control by means of their three-dimensional fin structure, their lateral gate control ability remains insufficient under ultra-short channel circumstances, making it difficult to fully fend off drain electric field interference.

3 Upsides of electrostatic control for GAA architecture

GAA architecture deals with these challenges by means of a revolutionary geometric reconstruction. In comparison with FinFETs, GAA devices insert the channel (nanowire or nanosheet) completely into the gate dielectric layer, getting 360° all-around electrostatic control. This structure gives an unprecedented capacity for gate control. The gate electric field is able to penetrate the channel evenly from all directions, establishing a very stable conductive path. This tight coupling mechanism assures that the gate potential fully commands the channel potential distribution, effectively preventing the drain electric field from penetrating inside the channel.

4 Particular physical ways GAA uses to suppress CLM

GAA technology controls CLM by means of the following dual mechanisms[5]:

First of all, the all-around structure notably heightens the contact area between the gate and channel, substantially augmenting the gate's ability to modulate the channel potential. This causes difficulty for the drain electric field to change the channel pinch-off point position by going beyond the gate control range.

Secondly, GAA makes use of very thin channels (equal to or less than the depletion width), attaining full depletion in the off state. In this situation here, there is no neutral charge accumulation region in the channel, and changes in the drain electric field can't physically impact the channel length by changing the depletion width. So, even at high VDS conditions, the effective channel length remains very stable, bringing CLM to the least amount.

5 Improvement of device performance and future prospects

Compared to FinFETs, at the same dimensional scale, GAA transistors show higher output impedance and lower-level Drain-Induced Barrier Lowering (DIBL) effects. With analog circuits in mind, single-stage amplifiers based on GAA can reach greater levels of voltage gain and linearity. Though GAA technology faces troubles in manufacturing process complexity, its good performance in suppressing short channel effects makes it the required pick for the promotion of next-generation semiconductor devices.

6 Body effect

In integrated circuits, a potential difference is present between the source and the substrate. The reverse bias voltage across the source-substrate junction gives rise to an additional electric field within the depletion layer. This extra reverse bias voltage enlarges the depletion layer's width and raises the surface charge density. So, there is an increased quantity of fixed negative charges (acceptor ions) per unit area, labeled as QB. According to what the charge balance equation states

$$Q_G = Q_{dep} + Q_{inv} \tag{4}$$

Q_G is the gate charge, Q_{dep} is the depletion layer charge, Q_{inv} is an inverse layer charge. Because VSB is greater than zero, Qdep shows growth. In order to create the inversion layer (i.e. In order to create Qinv, the gate must give extra charge to offset this additional increase in depletion layer charge. This makes VTH change state, making it a function of the source potential VS.

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_S} - \sqrt{2\phi_F}\right) \tag{5}$$

While the gate bias voltage VG is kept fixed, the overdrive voltage VOV = (VG − VS) − VTH is compressed. As a result of the body effect coefficient γ, the variation of VTH with VS is in a

square - root relationship. This means that when the input signal (which brings about variations in VS) has a large amplitude, VOV varies non-linearly in response to the signal amplitude, leading to the magnitude of the transconductance gm fluctuating with the signal amplitude. It causes the appearance of nonlinear distortion and indirectly degrades the effective gain. [6]

To take on this challenge, Fully Depleted Silicon-on-Insulator (FD-SOI) technology, because of its particular device structure, shows fine electrostatic control capacity, making it an ideal means to suppress the body effect. FD-SOI devices adopt a three-layer architecture consisting of the top silicon layer, buried oxide layer, and substrate, where the thickness of the top silicon film (tsi) is typically controlled within 5–10 nm, significantly smaller than the characteristic depletion width (Wdep) of silicon.This physical design makes the complete depletion of the channel region in the off-state possible, indicating that there's no neutral body region within the whole silicon film. The fully depleted mechanism essentially cuts the electrical connection between the body and the substrate. It prevents source/drain potential changes from influencing the channel potential via the substrate, and fully gets rid of the threshold voltage drift caused by the traditional body effect [7].

Notably, FD-SOI technology heightens gate control over the channel by means of the electrical isolation provided by the buried oxide layer (BOX). This powerful gate control can effectively suppress other short-channel effects like drain-induced barrier lowering (DIBL). It also notably reduces the subthreshold swing (SS), making it nearer to the 60 mV/dec theoretical limit. For practical circuit functions, FD-SOI devices show lower leakage current, a higher on/off ratio, and good-looking noise margin. So, they are particularly appropriate for high-performance computing, RF communication, and ultra-low-power IoT applications.

Mahamudul Hasan et al.More proof was given to validate the advantages of FD-SOI in logic circuits. Their study found that, without altering the transistors' basic geometric structure, FD-SOI technology can markedly improve the energy efficiency of adiabatic logic circuits by optimizing device electrostatics. Simulation results showed that FD-SOI-based circuits beat traditional bulk silicon solutions in both power and energy consumption, mainly because of the efficient control of body effects and leakage current. The study underlined that FD-SOI technology is widely accepted in the industry because of its excellent process compatibility. It enables considerable performance improvements without the necessity of revolutionary modifications to current manufacturing processes [8].

Overall, FD-SOI technology suppresses the body effect physically by means of its fully depleted mechanism and buried oxide isolation structure, resolving the instability of the threshold voltage that traditional bulk silicon devices face during scaling. Its superior electrostatic control, low-power characteristics, and good process compatibility establish it as a key technological pathway for high-performance, low-power integrated circuit design in the post-Moore era, providing a solid technical foundation for future applications in analog/RF circuits, neuromorphic computing, and AI accelerators at advanced technology nodes.

7 Miler effect

In the real-life physical world, transistors contain a number of parasitic capacitances. The most key is the reverse transfer capacitance (Cgd), attached between the input and output terminals.

The capacitance links up the high-gain input and output nodes. When there is a change of ΔV in the input voltage, because of the amplifier's voltage gain Av, the output voltage changes in the reverse way by AvΔV. In view of this, the total voltage change across the inter-terminal capacitance Cf gets near to (1 + Av)ΔV. Based on the charge formula Q = C·V, the input terminal has to supply extra charge to charge or discharge this capacitance. This effect is the same as connecting a much larger capacitance at the input terminal.

Miller's Theorem formula

$$C_{in} = C_f(1 + A_v) \tag{6}$$

A dramatic increase in input capacitance comes about because of the Miller effect. For high - frequency AC signals, the large capacitance Cin takes on the role of a low-impedance path (short circuit). If the input is directly coupled to an ideal voltage source, this capacitance will "divert" all high-frequency current, preventing the input voltage from being formed. To stem this diverted current, a series resistance has to be there in the input path, that is. The equivalent drive resistance, which is possibly the source resistance, the resistance of the stage before, or the bias resistance. The Miller capacitance Cin and it jointly form a first-order low-pass filter (RC circuit). As the signal frequency goes up, the capacitive reactance of the Miller capacitance reduces. Furthermore, Rs and Cin form a voltage divider.At high frequencies, the impedance of Cin is a great deal smaller than Rs, leading to a large decline in the effective signal voltage applied to the MOS transistor input. Once the frequency goes over the cutoff frequency.

$$f_c = \frac{1}{2\pi R_s C_{in}} \tag{7}$$

The gain will ebb at a rate of -20 dB/decade. It shows that the greater the Rs or the Miller capacitance, the earlier the gain decline (the narrower the bandwidth). Improved Design Analysis:

The method by which transistor T2 suppresses the Miller effect and improves bandwidth.

The high-frequency response of circuits is critically limited by the Miller effect. The current design makes use of an nMOS transistor to replace the traditional feedback resistor Rf and form an active feedback network. In this structure, transistor T2 is introduced and arranged to be a cascode. Its main function is to suppress the Miller effect by breaking the conditions for its generation. This leads to a large-scale reduction in the equivalent parasitic capacitance at the input terminal and an increase in the bandwidth.

In traditional inverting amplifier configurations, the Miller effect is a result of the feedback capacitance (mostly the gate-drain capacitance Cgd) between the input and output nodes. According to Miller's theorem, for an amplifier with voltage gain Av, the capacitance C between the input and output nodes shows an equivalent input capacitance of C(1 + Av).

In single-stage amplifier circuits, if a single transistor is used as the active feedback element, the Miller effect will have a severe consequence on its gate-drain capacitance Cgd. Because transimpedance amplifiers generally need high-gain operation for accurate current-to-voltage

conversion, the high gain at the output terminal results in a dramatic growth of the equivalent input capacitance. This phenomenon makes the time constant τ of the input node larger. It then reduces the dominant pole frequency and seriously limits the amplifier's bandwidth, possibly bringing about stability problems [9].

The circuit structure includes transistor T2, and its main function is to reduce the Miller effect and improve bandwidth [10].

T2 works on the basis of the cascode principle.

T2 is arranged in series with the active feedback transistor. The gate of the lower transistor gets the input signal, and T2 is placed between the drain of the lower transistor and the output load.

For the fixed potential mechanism, a consistent bias voltage is put on T2's gate, making the source of T2 (i.e. (the drain of the lower transistor) to keep a virtual ground or fixed - level potential under AC small-signal conditions.

In relation to gain isolation, T2 separates the important node in the feedback path (the drain of the lower transistor) from the high - gain output node. So, the AC voltage gain at the drain of the lower transistor is close to zero, rather than the full open-loop gain of the amplifier.

The quantitative analysis of the Miller effect elimination by transistor T2 can be done using the mathematical expression of the Miller coefficient.

In the absence of T2, the fact that the Miller coefficient is (1 + Av) leads to a significant increase in the equivalent input capacitance.

When T2 is present, the AC gain at the drain of the lower transistor is reduced almost to zero because of T2's isolation effect. As a result, the Miller coefficient turns out to be (1 + 0) = 1, and the equivalent input capacitance is reduced to about Cgd.

This decrease in equivalent capacitance directly lowers the input time constant, making the dominant pole shift to a higher frequency and widen the amplifier's bandwidth.

In conclusion, adding transistor T2 in a Cascode setup effectively curbs the Miller effect. It does this by separating the feedback path from the high-gain output node, leading to a notable decrease in equivalent input capacitance and an increase in bandwidth. This mechanism offers a reliable solution to enhance the high-frequency performance of single-stage amplifiers in nanometer-scale processes. In the traditional structure where T2 is not put in, the equivalent feedback capacitance C_eq seen by the input node is:

$$C_{eq} = C_{gd}(1 + A_{total}) \tag{8}$$

A_{total} Is the full voltage gain of the amplifier, generally a very large value, bringing about a substantial increase in C_{eq}.

After the introduction of T2, given that the source follower gain Av2 is almost 1 and it isolates the high output gain, the effective voltage gain between the drain and gate of the lower transistor is considerably lessened in quantity. As a consequence, the Miller multiplication factor is dampened, and the equivalent input capacitance is about restored to the intrinsic gate-drain capacitance of the transistor.

$$C_{eq} \approx C_{gd} \tag{9}$$

By means of this mechanism, T2 effectively disrupts the influence path of output voltage swing on the input feedback node. The parasitic capacitance, magnified initially due to the Miller effect, is "neutralized", allowing for a marked increase in the pole frequency at the input node.

8. Bandwidth enhancement

The time constant of the feedback network mainly fixes the bandwidth of a transimpedance amplifier. Based on the knowledge of circuit theory, the relation between the bandwidth (BW), the feedback resistance Rf, and the total input capacitance CT is given by:

$$BW \approx \frac{1}{2\pi R_f C_T} \tag{10}$$

For this design, Rf is determined by the channel resistance of the nMOS transistor and needs to be large to obtain high transimpedance gain. In the lack of T2, CT takes in the large Miller-equivalent capacitance, bringing about an overly large denominator and a very narrow bandwidth. As T2 comes into play, CT is restored to a smaller value of intrinsic parasitic capacitance.

As such, while keeping high transimpedance gain (large Rf), the circuit gets a fundamental enhancement in bandwidth as a result of the notable reduction in CT. This design resolves the gain-bandwidth trade-off and enhances circuit stability, thus lessening dependence on extra phase compensation circuits.

9 Conclusion

The paper looks into the performance bottlenecks of single-stage amplifiers in nanometer-scale processes, with a focus on the limiting mechanisms of the channel modulation effect, body effect, and Miller effect on gain, linearity, and bandwidth. A complete improvement strategy merging advanced device architectures with optimized circuit topologies is proposed. By way of theoretical derivation and simulation analysis, the following main conclusions are drawn:

First, the physical factors giving rise to low-frequency gain limitations are shown. Under low-frequency running, channel length modulation (CLM) and body effect are found to be the main factors that restrict DC gain and linearity.

Regarding the channel modulation effect, as technology gets smaller, non-ideal drain field's intrusion into the channel makes the effective channel length change as VDS changes, bringing finite output impedance ro. It directly weakens the ideal current source behavior in saturation, leading to a linear growth of the drain current with voltage and a major reduction in voltage gain.

About body effect, in traditional bulk silicon processes, reverse bias at the source-substrate junction results in charge coupling, making the threshold voltage VTH move with source

potential. It not only constricts the overdrive voltage and decreases transconductance gm but also brings about severe signal-dependent nonlinear distortion, degrading amplifier linearity.

Then, the benefits of advanced device architectures in suppression are shown. To address these physical constraints, this paper looks into the high-level performance of gate-all-around (GAA) and fully depleted silicon-on-insulator (FD-SOI) technologies.

GAA architecture uses its 360° all-sided gate control and fully depleted channel elements to improve electrostatic integrity over the channel potential to a significant degree. This efficiently prevents the drain field from being penetrated, lessening CLM effects.

FD-SOI technology uses the buried oxide layer (BOX) to cut off the electrical connection between the body and substrate. This basically gets rid of the threshold voltage drift caused by body effects, thus providing a physical basis for enhancing device output impedance and linearity.

Thirdly, the physical trade-off in high-frequency bandwidth and the path to solve it are explained. In high-frequency application cases, the Miller effect is the main barrier for bandwidth.

The study shows that when multiplying the gate-drain parasitic capacitance Cgd by the Miller factor, a large equivalent input capacitance Cin comes into being. When combined with the source resistance, it forms a low pass filter. This makes the high-frequency gain roll off at - 20 dB/decade, showing the basic trade - off between gain and bandwidth.

To sort out this matter, the proposed cascode active feedback structure makes use of transistor T2 to isolate and fix the AC potential at the output node of the input stage, decreasing the Miller multiplication factor to nearly zero ($Ceq \approx Cgd$). This technique successfully detaches the gain-bandwidth trade off, maintaining high transimpedance gain and remarkably increasing the - 3 dB bandwidth of the circuit.

Summarily, high-performance single-stage amplifier design necessitates a "device physics optimization + circuit topology innovation" approach. Utilizing advanced processes such as GAA and FD-SOI to suppress short-channel and body effects at the physical level, combined with cascode structures to eliminate Miller effects at the circuit level, is the essential path to breaking traditional performance bottlenecks and achieving concurrent optimization of high gain, high linearity, and wide bandwidth.This study gives both theoretical framework and practical guidance for the design of high - performance analog integrated circuits in the post-Moore era.

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