A Wide Temperature Range CMOS Bandgap Voltage Reference With 4.689ppm/°C in 65nm

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Abstract. This paper proposes a low TC BGR voltage source working in a wide temperature range of -45 to 125°C, based on TSMC 65nm. To address the limitation that the TC of traditional first-order temperature-compensated BGRs is difficult to be lower than 10 ppm/°C, this paper proposes an improved method limits the output voltage at the starting point within the temperature range by introducing a resistor, thereby optimizing the output waveform from the traditional parabolic waveform to an approximately sinusoidal waveform, thus effectively reducing the TC without increasing circuit complexity. Simulation results based on the Virtuoso show that, with a power supply of 3.3V and tt corner, this BGR achieves a low TC of 4.689 ppm/°C, a PSRR of -63.5 dB at low frequencies, and a power consumption of 67 μW.

Keywords: Temperature Compensation, BGR, Low TC, Power Supply Rejection Ratio, Wide Temperature Range

1 Introduction

Nowadays, with the progress and development, the demand for integrated circuits is constantly growing across many industries. The feature size of devices is constantly shrinking, and the power consumption of integrated circuits continues to decrease. As an important module in analog integrated circuits, the BGR (BGR) can provide a reference output independent of temperature and supply voltage. It has received widespread attention from researchers in the research process of integrated circuits and has achieved great development. BGRs not only have superior performance, but are also fully compatible with standard CMOS processes, making them widely used as reference sources in analog integrated circuits.

To meet the needs of industrial production, BGRs with different performance requirements have emerged. Because traditional BGR designs typically employ only first-order temperature compensation, their TCs are generally difficult to achieve below 10 ppm/°C. To address this, Xiong et al. proposed a BGR employing high-order curvature compensation technology, achieving a TC of 1.02 ppm/°C [1]. Since BGRs in SoCs are affected by power supply voltage

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fluctuations, Fu et al. introduced a low-power regulator into a high PSRR BGR design. This design achieves a low TC and low noise while maintaining a PSRR of −80 dB at 1 kHz [2]. Highly integrated SoCs place demands on BGRs with low power consumption and low voltage. Huang et al. proposed a BGR design without operational amplifiers, achieving a power consumption of 192nW [3]. In addition, Liu et al. proposed a reference source with an all-MOSFET structure. By adjusting the transistor to work in the subthreshold region, the circuit has a low voltage reference output with a value of 151.9mW and a power consumption of 17.6nW [4]. Also based on an all-MOSFET structure, Tong et al. designed a reference source with a power consumption of 9.6nW and a reference voltage of 210mV [5].

This article will introduce some basic principles of BGR and design a BGR based on 65nm CMOS process. Compared with other BGR, the proposed design archives a high performance in a wide temperature range, and it can be used in system designs that require the lowest possible complexity.

2 Basic principle

In analog integrated circuit design, it is often necessary to bias a certain part of the circuit. For example, in operational amplifiers, the tail current source often needs to be obtained from a reference current through a current mirror, which can be generated by a BGR. Furthermore, in low-dropout linear regulators (LDOs), the operational amplifier requires a reference voltage to ensure that the output voltage is independent of temperature; this reference voltage can also be generated by a BGR. A BGR can generate a reference output whose output is independent of PVT, and can provide a constant bias for other circuits.

Figure 1 shows a self-biased circuit with an introduced source resistor, which enables the output to remain unaffected by power supply voltage fluctuations. There are two current mirrors composed of M_3, M_4, M_1, and M_2. They bias each other. Assuming channel length modulation effect is ignored, then $I_{OUT} = KI_{REF}$. Although the circuit eliminates the influence of the power supply voltage, its output current is only proportional to I_{REF} and is not a real current value. Therefore, a resistor R_S is added to the circuit [6-8].

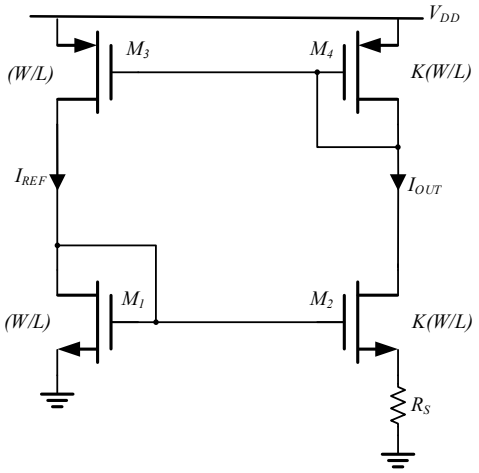

Fig. 1. A self-biased circuit with an introduced source resistor.(Picture credit: Original)

In this circuits R_S will decrease the current of M_2, and the expression for I_{OUT} can be derived from the following derivation.

$$\sqrt{\frac{2I_{\text{out}}}{\mu_n C_{\text{ox}}(W/L)_S}} + V_{TH1} = \sqrt{\frac{2I_{\text{out}}}{\mu_n C_{\text{ox}} K(W/L)_N}} + V_{TH2} + I_{\text{out}}R_S \tag{1}$$

After Ignoring body effects.

$$\sqrt{\frac{2I_{\text{out}}}{\mu_n C_{\text{ox}}(W/L)_N}\left(1 - \frac{1}{\sqrt{K}}\right)} = I_{\text{out}}R_S \tag{2}$$

The expression that yields the final I_{OUT}.

$$I_{OUT} = -\frac{2}{\mu_n C_{\text{ox}}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{3}$$

In this expression, the output I_{OUT} determined by the source resistor R_S, and the expression is independent of the power supply voltage, thus obtaining an output that does not fluctuate with the power supply.

Finding a completely temperature-independent output in semiconductor processes is extremely difficult. However, by superimposing the output of a positive TC (PTAT) and a negative TC (CTAT), a reference output that approximates the temperature independence can be obtained relatively easily.

$$I_c = I_s \exp\left(\frac{V_{be}}{V_T}\right) \tag{4}$$

$$I_s = bT^{4+m} \exp\left(-\frac{E_g}{kT}\right) \tag{5}$$

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4+m)V_T - E_g}{T/q} \tag{6}$$

In order to find a quantity that is positively correlated with temperature, some scholars have proposed two bipolar transistors operating at different current densities, as shown in Figure 2, whose base-emitter voltage difference (ΔV_{BE}) is proportional to the absolute temperature. The relationship between ΔV_{BE} and temperature is derived as follows.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_t \ln\left(\frac{nI_0}{I_{S1}}\right) - V_t \ln\left(\frac{I_0}{I_{S2}}\right) = V_t \ln n \tag{7}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n > 0 \tag{8}$$

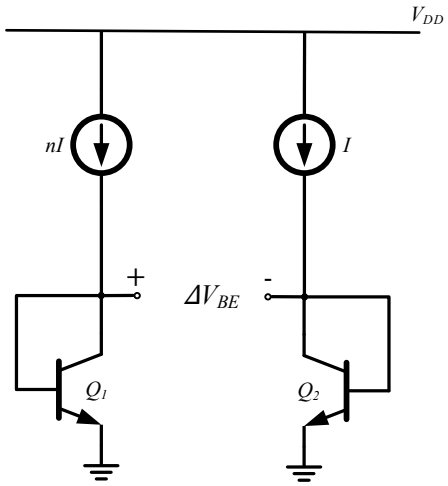

Fig. 2. ΔV_{BE} generation circuit. (Picture credit: Original)

By using the methods described above to generate negative and positive TC voltages respectively, a circuit can be designed to superimpose them to obtain a temperature-independent reference voltage. As shown in Figure 3, the Brokaw BGR circuit combines the design in Figure 1, using the V_{BE} difference between Q1 and Q2 to construct the current, which is independent of the power supply. The voltages at points X and Y are equal because the source voltages of M_3 and M_4 are clamped by the same V_{GS}, and the voltage applied to resistor R_S is the difference between the V_{BE} of Q1 and Q2, i.e., the voltage difference is PTAT. In addition, the voltage at point Z, i.e. the V_{BE} 为 CTAT，of transistor Q2, is CTAT. Therefore, the voltage output at point Y can be considered independent of temperature.

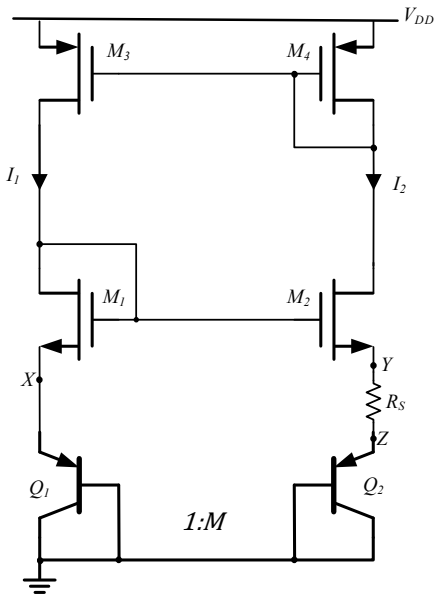

Fig. 3. Brokaw BGR circuit. (Picture credit: Original)

Although the above circuit can obtain the reference voltage relatively easily, this clamping method using a current source is rather crude, and due to the channel length modulation effect, there are errors in the voltage clamping at points X and Y. To address this issue, operational amplifiers (op-amp) can be incorporated into the design of BGRs. This method utilizes the virtual short characteristics of op-amps to better clamp the circuit. Figure 4 shows a classic bandgap voltage reference source employing this method. The circuit requires the op-amp to have a sufficiently high gain so that the voltages at points X and Y can be better clamped. The V_{REF} is the voltage with zero TC, which is represented by the following expression (9), where V_{BE} is the amount representing CTAT and $V_T ln\, n$is the amount representing PTAT. By adjusting the ratio of R_1 and R_2, a reference voltage independent of temperature can be obtained.

$$V_{\mathrm{REF}} = V_{BE} + \frac{R_2}{R_1} V_T \ln n \tag{9}$$

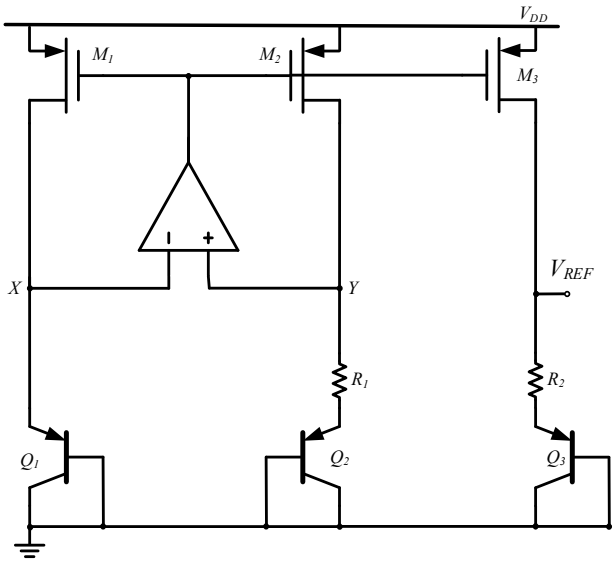

Fig. 4. BGR circuit with introduced op-amp. (Picture credit: Original)

3 Proposed design

In the previous chapter, this paper analyzed the basic principle of BGRs and introduced a BGR voltage source that introduced an op-amp. This chapter presents a BGR voltage source designed based on this circuit, suitable for engineering applications. Traditional BGR voltage sources with op-amp compensate for VBE using thermal voltage V¬T. This first-order temperature compensation makes it difficult to achieve a TC of the reference source below 10 ppm/°C. This design reduces the TC by introducing a resistor to limit and compensate the output voltage at the starting point within the temperature range of -45 to 125°C. Compared to the traditional first-order temperature compensation method, which outputs a parabolic waveform, this method outputs a sinusoidal signal. Furthermore, this design uses a certain proportion of the current mirror output current to bias the op-amp, thereby offsetting the op-amp output changes under temperature variations. This design effectively and simply reduces the TC to below 10 ppm/°C, and also exhibits good PSRR and chip consistency.

3.1 Design of op-amp

As an important part of this design, the performance of the operational amplifier directly affects the various performance indicators of the BGR. In the design shown in Figure 5, the op-amp acts as a clamp and biases the current mirror tube. In this design, the clamped voltages at points X and Y are approximately between 600mV and 900mV, and the op-amp in this design should be PMOS inputs. Furthermore, this design does not actually require high-gain op-amp, and the need to compensate for high-gain two-stage op-amp would increase the complexity of the design. Finally, since the entire BGR system requires a relatively high PSRR, if an op-amp with a high

PSRR is used, the small signal generated by power supply fluctuations will affect the output current of the current mirror. Therefore, this design does not require an op-amp with a high PSRR. In summary, this design employs a PMOS-input folded common-source cascode operational amplifier.

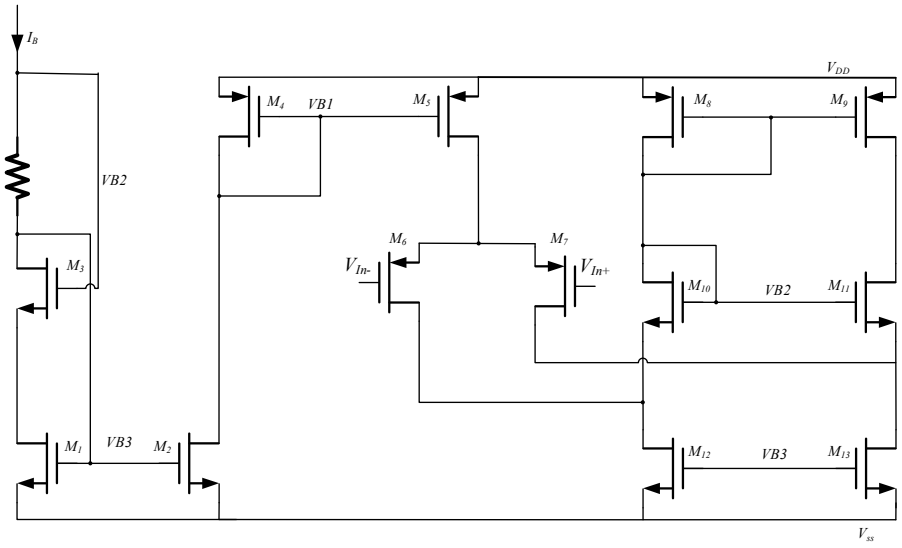

Fig. 5. The mentioning op-amp circuits. (Picture credit: Original)

It is worth noting that this op-amp design requires current matching of the PTAT current circuit of the BGR to ensure that the op-amp input point can be well clamped. Therefore, this op-amp can be biased by the PTAT current in the reference source through a current mirror, that is, IB is biased through the reference source, which is reflected in the Core circuit of the BGR voltage source.

3.2 Design of the core of the bgr voltage source

Figure 6 shows the Core circuit of the BGR voltage source. The current on transistor M_3 will actually be mismatched with that on transistors M_1 and M_2. To suppress the channel length modulation effect, resistors R_3 and R_4 are added to the drain terminals of transistors M_1 and M_2 in the original circuit, thereby eliminating the reference output deviation caused by the inconsistency of current. Furthermore, in actual simulation tests, biasing the op-amp can prevent it from clamping the X and Y points effectively. By introducing the PTAT current I_B to bias the op-amp, the M_2 transistor branch can achieve a good positive TC effect. In this design, by setting the resistance and ratio of R_1 and R_2 the output value is limited to the same value at -45°C and 125°C, thereby achieving a downward shift in the overall output curve and easily obtaining a lower TC.

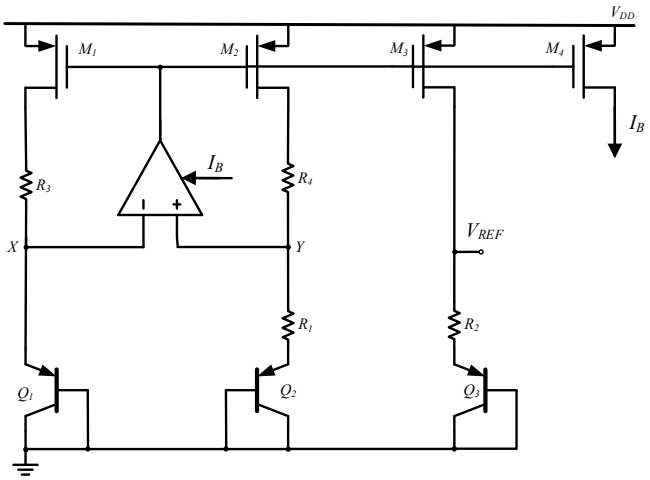

Fig. 6. Core of the BGR voltage source. (Picture credit: Original)

4 Simulation results

In the previous chapter, this paper analyzed some basic principles of BGRs and introduced a BGR voltage source that introduced an op-amp. This chapter presents a bandgap refe

4.1 TC simulation

The waves in Figure 7 show the output simulation results of this design. In the temperature range of -45 to 125°C, the output waveform of a traditional BGR voltage source is generally a downward-opening parabola. In contrast, the output waveform of this design is an approximately sinusoidal signal. In PVT simulations, under the ss corner, the simulated output waveforms for different power supply voltages all showed a poor upward trend. The output waveforms for other corners, however, were relatively good.

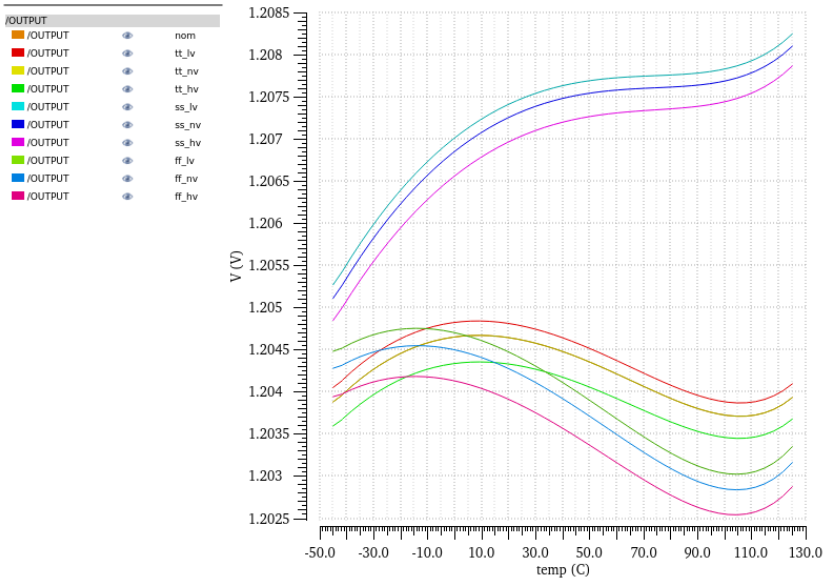

Fig. 7. Simulation results of BGR reference voltage output. (Picture credit: Original)

The TCs in Table 1 were calculated based on the simulation results of the BGR reference voltage output. These results show that the TCs of different power supply voltages can reach below 10 ppm/°C under the tt and ff corners, while the TC under the ss corner is greater than 10 ppm/°C. The TC simulation results are consistent with the output waveform of the reference voltage. Except for the ss corner, all other corners show good temperature characteristics.

Table 1. Simulation results of TC.

corner_power supply	tt_3V	tt_3.3V	tt_3.6V	ss_3V	ss_3.3V	ss_3.6V	ff_3V	ff_3.3V	ff_3.6V
TC (ppm/°C)	4.752	4.689	4.434	14.52	14.59	14.72	8.459	8.358	8.022

4.2 PSRR simulation

The waves in Figure 8 show the PSRR simulation results of this design. The results show that within the low frequency range of 1kHz, except for the simulation environment with a 3.6V power supply voltage input at each corner, the PSRR is less than -60dB in other environments. At a high frequency of 1MHz, the PSRR in various simulation environments reaches approximately -50dB, while at a frequency of 1GHz, the PSRR is around -55dB. The simulation results show that the design has good PSRR and a certain rejection to power supply fluctuations.

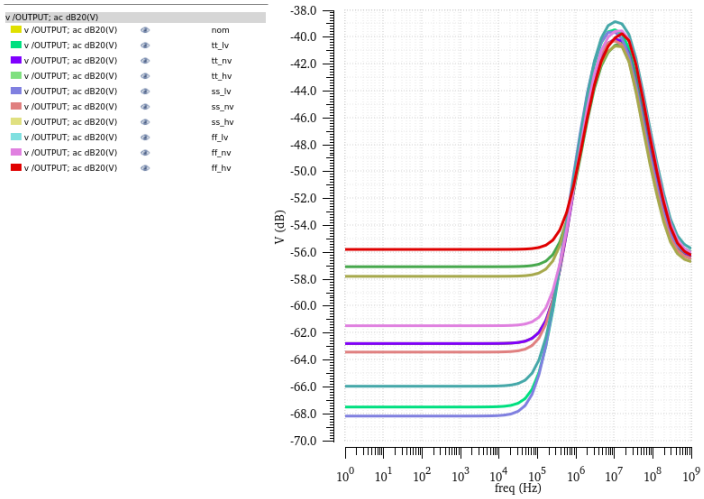

Fig. 8. Simulation results of PSRR. (Picture credit: Original)

4.3 Monte carlo simulation

Figure 9 shows the Monte Carlo simulation results of this design. The simulation was set to a power supply voltage of 3.3V at room temperature and 200 samples. The results show that the highest reference voltage is 1.21369V and the lowest is 1.19591V. Statistical results show that the mean reference voltage is 1.2048 mV, the standard deviation is 2.96309 mV, and the ratio of the standard deviation to the mean is 0.24594%, indicating that the reference output deviation of this design is small and has a certain degree of chip consistency.

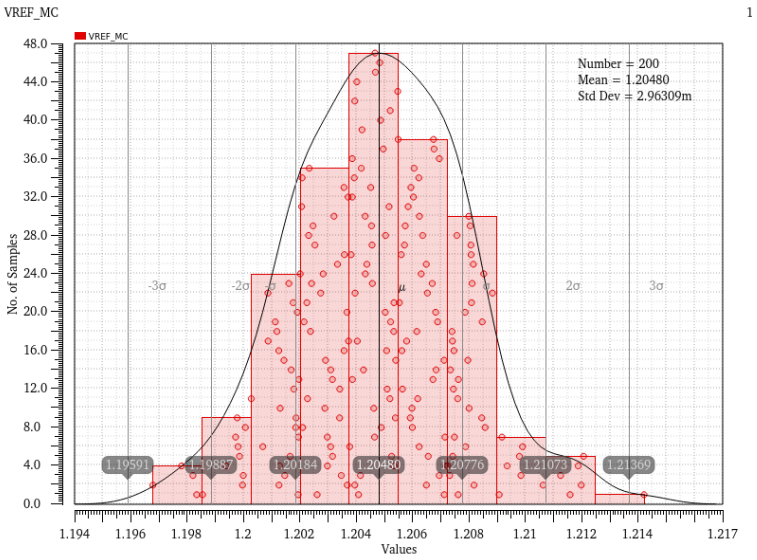

Fig. 9. Simulation results of Monte Carlo. (Picture credit: Original)

Based on the simulation results, the BGR voltage source designed in this paper achieves a TC of 4.689 ppm/°C over a wide temperature range of -45 to 125°C under standard operating conditions, a PSRR of -63.5 dB at low frequencies, and a small ratio of standard deviation to mean. Table 2 compares the performance indicators of this design with those of published bandgap voltage references. This design achieves relatively good performance indicators with a relatively less complex circuit design by using limit compensation for the highest and lowest temperature points within the temperature range.

Table 2. The performances compared with published bandgap voltage references [8-11].

Performances	This BGR	BGR.	BGR.	BGR.	BGR.
Process (nm)	65	350	180	180	65
Power Supply(V)	3.3	2.6-5	1.8	1	0.85
Reference(V)	1.205	2.47	1.235	0.5	0.65
Temperature Range (°C)	-45-125	-45-125	0-125	-40-125	-20-80
TC(ppm/°C)	4.689	3	93	85.08	111
PSRR(dB)	-63.5@dc	-83@dc	N/A	-105.54	-38
POWER(W)	67μ	N/A	11.5n	5.13μ	38n
σ/mean (%)	0.24594	0.2	N/A	N/A	0.59

5 Conclusion

This article introduces the basic principles of BGRs and explains the meaning of their various performance indicators. Based on the principle of BGRs, this paper designs a BGR voltage source. This BGR achieves a wide temperature range of -45-125°C, a TC of 4.689 ppm/°C, a PSRR of -63.5dB at low frequencies, and a small ratio of standard deviation to mean under standard conditions of 3.3V power supply and tt corner. This circuit can be used in system designs that require the lowest possible complexity. However, this design suffers from a high TC at the ss corner, which can be mitigated using trim. Furthermore, chopping techniques can be employed to optimize potential op-amp input misalignment in this design.

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