Load Evolution and Gain/Linearity Trade-off Mechanisms in High-Performance Single-Stage Amplifiers

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Abstract. This article systematically reviews the development path of high-performance single-stage amplifiers under low-voltage constraints. First, leveraging the superposition principle and physical equivalent models, this paper clarifies the physical mechanisms of circuit nonlinearity and the physical connotation of impedance characteristics. Subsequently, it systematically discusses the evolutionary logic of load techniques: it analyzes the "gain–swing deadlock" caused by traditional resistive loads, examines how active loads realize impedance decoupling, and further derives inverter-based current-reuse architectures. In response to the recent demand for ultra-low-power design, it focuses on application strategies of inverter-based structures at 0.3 V ultra-low supply voltage and in the subthreshold region. This paper further investigates linearization techniques centered on source degeneration and comparatively studies the trade-off between resistive degeneration and active degeneration in terms of noise characteristics and area efficiency. The survey indicates that combining inverter-based current-reuse topologies with active linearization techniques is a key trend for future high-energy-efficiency.

Keywords: Analog front end; Low-voltage design; Current reuse; Source degeneration; Linearization techniques

1 Introduction

In the intelligent era of ubiquitous connectivity, whether implantable brain–computer interfaces or large-scale industrial sensor nodes, miniaturized electronic systems are profoundly reshaping human life and modes of production. These edge devices are typically powered by batteries or even energy harvesting, which imposes extremely stringent power constraints. For example, in neuroscience research, long-term monitoring of electroencephalographic signals requires the power density of implantable chips to be tightly controlled to prevent tissue thermal damage. This implies that, under a nanowatt (nW)-level power budget, the amplifier—being the first and core component of the signal chain—must still provide high-fidelity amplification for weak signals. As a result, extreme energy efficiency has gradually replaced pure speed metrics and has become the primary objective of next-generation analog circuit design.

However, as CMOS technology nodes continue to scale down, the supply voltage has dropped from the traditional 3.3 V to 0.6 V or even lower. Harrison et al. early established the basic architecture of low-noise amplifiers for neural recording, laying the theoretical foundation for

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this field [1], Later, Wattanapanitch et al. demonstrated an energy-efficient micropower neural recording amplifier, further advancing this research direction [2]. Yet, with compressed headroom, transistors can hardly remain deeply in saturation, leading to a pronounced degradation of intrinsic gain. Conventional cascode structures require stacking multiple transistors and thus become unusable under ultra-low supply voltages. Designers are therefore forced to make difficult trade-offs among gain, swing, and linearity. As noted by Grasso et al. in their latest survey, analog design is shifting from the paradigm of "voltage-domain stacking" to that of "current-domain reuse" [3].

This paper reviews solutions in existing studies that address these challenges through topological evolution, with emphasis on the evolutionary logic from "passive loads" to "current reuse." Section 2 analyzes, at the physical level, the mechanisms underlying nonlinearity and impedance characteristics. Section 3 systematically reviews the development trajectory of load techniques and, in combination with key publications from the past five years, provides an in-depth analysis of inverter-based current-reuse techniques under 0.3 V ultra-low-voltage operation and their performance breakthroughs. Section 4 focuses on circuit linearization techniques and discusses recent progress in source-degeneration strategies. Through a systematic review of frontier literature, this paper aims to provide a clear technical path for the design of high-performance low-voltage amplifiers.

2 Theoretical basis and physical mechanism analysis

2.1 Superposition principle and "AC ground"

In analog circuit analysis, the concept of "AC ground" originates from the superposition principle. That is, the instantaneous voltage at any node in a circuit can be decomposed into a DC component and an AC small-signal component, which linearly superimpose. For an ideal supply node, because its DC voltage is constant and its AC component is zero, it appears as ground in the small-signal model. As discussed by Chatterjee et al., in ultra-low-voltage designs such as 0.5 V, an accurate understanding of this superposition principle is particularly critical for constructing body-driven biasing circuits, because it decomposes a nonlinear full circuit into linear AC paths, thereby providing theoretical support for subsequent analysis [4].

2.2 Gain fluctuation and the mechanism of nonlinearity

Nonlinear distortion in amplifiers fundamentally arises from the non-constancy of the MOS transconductance g_m. According to the square-law relationship, g_m exhibits a bell-shaped dependence on the instantaneous overdrive voltage; this "amplitude dependence of gain" causes waveform distortion at the output. In low-power designs, to pursue high g_m/I_D efficiency, transistors often operate in the subthreshold region, where the exponential current–voltage nonlinearity is even more pronounced, making linearization an urgent core challenge.

3. Load evolution and current-reuse techniques

3.1 The dilemma of resistive loads: gain–swing deadlock

In early common-source amplifiers with resistive loads, analysis by applying the chain rule shows that the voltage gain A_v exhibits a linear dependence on the load impedance R_D. However, the dynamic resistance and the static resistance of a linear element are tightly coupled. If R_D is increased, the DC voltage drop inevitably increases as well. With a fixed supply voltage, this causes the output DC level to decrease substantially, driving the transistor into the linear region. This "gain–swing deadlock" makes purely resistive-load structures difficult to adapt to the low-voltage requirements of modern nanometer processes.

3.2 Decoupling strategy of active loads

To break the "gain–swing deadlock" imposed by purely resistive loads, the active-load technique emerged. The core mechanism is to introduce a PMOS transistor operating in saturation as a current-source load. From the small-signal equivalent model, a transistor in saturation can provide a very high AC output resistance r_o, thereby effectively improving the intrinsic voltage gain of a single-stage amplifier. Meanwhile, under large-signal DC bias conditions, this structure only needs to sustain the transistor overdrive voltage (i.e., the saturation voltage drop), avoiding the severe DC drop caused by a large passive resistor. This feature successfully realizes a physical-level decoupling between the circuit's dynamic AC gain and its static DC operating point, enabling a large output voltage swing even under extremely limited supply headroom.

3.3 The rise of current reuse and inverter-based structures

Although active loads effectively resolve the deadlock between gain and swing, the PMOS transistor is used only as a current source and does not participate in the core signal amplification. To further exploit energy-efficiency potential, the inverter-based amplifier architecture has gradually become a central research hotspot in AFE design over the past five years.

The most prominent characteristic of this architecture is its bilateral push–pull mechanism, which can achieve a substantial (additive) improvement in transconductance efficiency. The input signal is applied simultaneously to the gates of both PMOS and NMOS transistors. Theoretical derivation shows that this push–pull mechanism successfully achieves "current reuse". In simple terms, without adding additional static bias current, the effective transconductance of this circuit has been improved, reaching approximately $g_{m,n} + g_{m,p}$ [5]. Leveraging its inherent advantage of requiring no vertically stacked transistors, and combined with body-driven technology, this structure can achieve a DC gain of 65 dB with a power consumption of only 9 nW. This fully demonstrates that this topology does have the potential to break through the so-called headroom limit [6].

To further optimize the overall figure of merit (FOM) of amplifiers, biasing inverter-based structures in the subthreshold region has become an important strategy to improve energy efficiency. Lv et al. investigated this design approach [7]. The results show that, relying on the exponential current–voltage characteristic of transistors in subthreshold operation and superimposing the current-reuse mechanism, the circuit can trade extremely low static power

for relatively high effective transconductance. This property makes it well-suited to biomedical scenarios with stringent energy budgets, such as cardiac pacemakers.

In addition, to mitigate the inherent sensitivity of inverter-based structures to process, voltage, and temperature (PVT) variations, robustness-enhancement solutions have also been proposed. Rodovalho et al. presented a solution based on self-biased (Self-Biased) and supply-voltage-scalable techniques [8]. By introducing a dynamic feedback loop to precisely lock the quiescent operating point, this technique ensures stable amplifier performance over a wide range of environmental variations, effectively overcoming the major obstacle to engineering deployment of this architecture.

4. Linearization technique strategies

4.1 Source degeneration mechanism and noise trade-off

Source degeneration introduces a series of negative feedback, shifting the determinant of gain from nonlinear active devices to highly linear feedback elements. Zhang et al. systematically summarized the theoretical basis for improving the input third-order intercept point (IIP3) using this mechanism [9]. However, introducing physical resistors inevitably generates additional thermal noise, leading to a confrontation between linearity and noise performance. To address this physical trade-off, Wang et al. proposed a quantitative analysis model in their latest neural-recording amplifier design, based on “power-to-noise optimization” [10].

The key innovation of this work lies in abandoning traditional experience-based parameter tuning and instead precisely solving for the theoretically optimal degeneration resistance. Under strict linearity constraints, it successfully pushes the overall system noise toward the theoretical physical limit. This achievement not only alleviates the noise degradation brought by passive degeneration but also demonstrates that, through system-level quantitative optimization, an optimal balance between noise and linearity can indeed be realized under extremely low power budgets, providing an important deterministic design guideline for high-fidelity bio-signal acquisition.

4.2 Frontier exploration of active source degeneration

As technology nodes continue to scale into deep submicron, the large chip area occupied by passive high-value resistors has become a prominent bottleneck limiting high-density integration. To break the area constraint, Rodovalho proposed an innovative active source degeneration technique (Active Source Degeneration) [11]. This technique abandons traditional physical resistors and instead uses MOS transistors operating in the deep linear region as degeneration elements. Experimental results show that this strategy not only saves about 40% of layout area, but also cleverly combines forward body biasing to actively compensate the second-order nonlinearity coefficient of the dominant transconductance devices.

The core innovation of this scheme is “using nonlinearity to cancel nonlinearity,” exploiting the controllability of active devices to compensate for their own nonidealities. Its significant advantage is that it thoroughly breaks the traditional physical barrier whereby “high linearity inevitably leads to large area,” proving that under area-constrained advanced nodes, electrical

compensation via auxiliary circuitry can effectively replace bulky passive devices, thereby achieving very high area efficiency.

In high-frequency driver amplifier designs that must handle larger signal swings, active linearization techniques exhibit stronger topological adaptability. Jiang et al. successfully extended linearization strategies to push–pull architectures and proposed a dual-loop dynamic biasing technique [12]. By monitoring signal amplitude in real time and dynamically adjusting gate-bias voltages, this structure achieves deep suppression of intermodulation distortion (IMD).

The key innovation of this work realizes a mechanism shift from "static biasing" to "dynamic tracking." Experimental results demonstrate that, when facing complex large-signal excitations, the dynamic compensation mechanism can effectively expand the linear input range of the circuit. This case further reveals that integrating dynamic bias control with complex reuse topologies is a crucial evolutionary direction for solving distortion challenges in future wide-dynamic-range AFEs.

5. Conclusion

This paper systematically reviews the technological evolution path of high-performance single-stage amplifiers under low-voltage and low-power constraints. The analysis indicates that, as integrated-circuit processes continue to scale, the load topology of single-stage amplifiers has undergone a profound transformation—from traditional resistive loads to active loads, and further to inverter-based current-reuse architectures (Current Reuse). Now the design ideas of the analog circuit have changed a lot, and it is no longer just the pursuit of high gain, but also takes into account the factors of noise efficiency factor and ultra-low voltage adaptability. Through the study, in the case of particularly low voltage, the inverter structure with subthreshold bias and bilateral push-pull technology can solve the problem of energy efficiency. Furthermore, the study reveals that if the active source degeneration and dynamic self-biasing methods are added, the nonlinear distortion of the device itself can be well controlled, so that the circuit has more adaptability to process, voltage, and temperature (PVT) variations. These results provide a theoretical basis for the performance improvement of nanoscale analog front-end chips, and more importantly, give a specific design direction for achieving high gain and high linearity under extremely low power consumption conditions. It is foreseeable that with the development of edge computing and heterogeneous integration technology, the previous fixed circuit design may not be enough. Future research should focus on combining the key technology of machine learning-assisted intelligent bias technology and dynamic noise reduction methods designed for the characteristics of bioelectrical signals, so that the circuit can be automatically adjusted to the best.

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