Common-Mode Voltage Suppression of a Five-Level ANPC Inverter Based on a Novel SVPWM Strategy

Sizhe Wei

{2350302@tongji. edu. cn}

College of Transportation, Tongji University, Shanghai, 201204, China

Abstract. To address the issue that the amplitude of common-mode voltage (CMV) in inverters tends to increase as the number of voltage levels rises, this paper takes a three-phase five-level ANPC inverter as the study object and reviews a CMV suppression method based on a novel SVPWM strategy that reconstructs the space-vector diagram by selecting 19 vectors that generate zero CMV from the 125 space vectors of conventional five-level SVPWM, thereby suppressing CMV while substantially reducing the computational burden. Theoretical analysis and simulation results both demonstrate that the method can significantly reduce the CMV amplitude while maintaining output waveform quality and effectively balance capacitor-voltage; however, its linear modulation range is reduced compared with that of conventional SVPWM.

Keywords: five-level ANPC inverter; novel SVPWM strategy; CMV suppression; capacitor-voltage balancing; redundant switching states

1 Introduction

In recent years, multilevel inverters have attracted extensive attention in high-voltage and high-power applications. The basic principle is to synthesize an approximate sinusoidal output with multiple voltage levels. Compared with two-level inverters, multilevel inverters can produce higher-quality waveforms while reducing the stress of voltage when devices switching and, to some extent, enabling lower switching frequency to improve system efficiency.Noticeably, the five-level active neutral-point-clamped (ANPC) inverter becomes increasingly important. However, common-mode voltage (CMV) amplitude increases with the number of voltage levels. CMV may induce electrical erosion and electromagnetic interference, reducing equipment lifetime. Suppressing CMV while maintaining output performance has become a key issue in the modulation of multilevel inverters.

In recent years, space-vector PWM (SVPWM) methods for CMV suppression in five-level inverters have received an increasing attention. For instance, Zhang et al. decomposed a five-level SVPWM scheme into two three-level SVPWM modulators: one three-level inverter uses switching states with zero CMV, the other uses conventional SVPWM modulation [1]. This

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method can reduce the maximum CMV by approximately 60%. To balance DC-bus neutral-point voltage, Jiang L et al. injected a zero-sequence current and determined an optimal key zero-sequence voltage according to the required neutral-point current, minimizing the voltage ripple of neutral-point on the DC side [2]; they further narrowed the zero-sequence voltage range to constrain the CMV amplitude, ensuring that one quarter of the DC-bus voltage exceeds the CMV magnitude. Liu et al. proposed a two-carrier PWM algorithm for a novel five-level inverter to eliminate CMV [3], achieving the zero-CMV objective while balancing flying-capacitor voltage .

Although the above methods suppress the CMV effectively, the conventional SVPWM becomes highly complex, and the computational burden increases dramatically. To address this issue, this paper reviews a novel five-level SVPWM algorithm based on zero-CMV vectors, which synthesizes the reference voltage vector using vectors with zero CMV, suppressing the CMV amplitude and significantly simplifying the computation. Both theoretical analysis and simulation experiments verify the effectiveness of the method.

2. Operating Principle of the Inverter and the Novel Modulation Strategy

2.1 Operating Principle of the ANPC Inverter

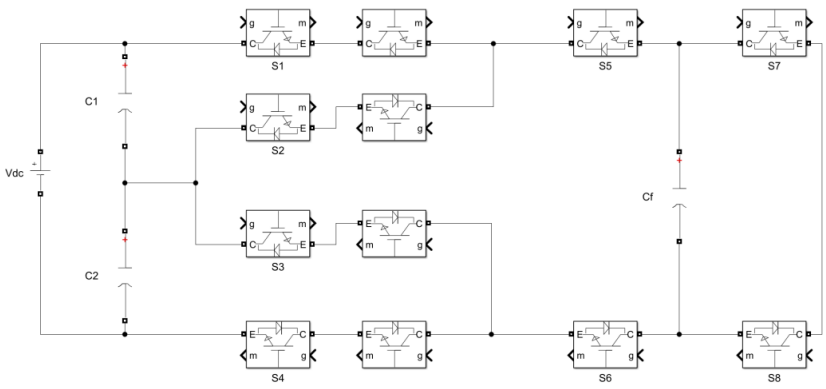

Fig. 1. Topology of single-phase five-level ANPC inverter (Photo/Picture credit: Original).

Fig. 1 depicts the five-level ANPC inverter topology. The inverter is a three-phase system, and every phase leg contains 8 switching devices (S1−S8), DC-link capacitors (C_1, C_2), a flying capacitor (C_f), a neutral point O, and V_{dc} denotes the DC-bus voltage. Taking phase A as an example, when switching combination S1, S3, S5, S7 applied, the output voltage is U=0.5V. When switching combination S1, S3, S5, S8 or S1, S3, S6, S7 applied, the output voltage is U=0.25V. When switching combination S1, S3, S6, S8 or S2, S4, S5, S7 applied, the output voltage is U=0V. When switching combination S2, S4, S5, S8 or S2, S4, S6, S7 applied, the

output voltage is U=−0.25V. When switching combination S2, S4, S6, S8 applied, the output voltage is U=−0.5V. The operating principles of other two phases are analogous. In total, the inverter has eight distinct switching combinations (V0–V7), which are mapped to five discrete voltage levels. As a result, the three levels (−E, 0, E) each have one redundant switching state, meaning that the same output level can be realized by multiple switching combinations. Although redundant states are equivalent from the load perspective, they affect the DC-link capacitors and the flying capacitor in a different way; therefore, they can be exploited for balancing the voltage of the capacitor.

The output voltages of a five-level ANPC inverter consist of positive-, negative-, and zero-sequence components, where the common-mode voltage (CMV) corresponds to the zero-sequence component. The phase voltages U_{AO}, U_{BO}, U_{CO} are defined as the voltages between each phase-leg output terminal (A/B/C) and the midpoint of the DC-side bus. The common-mode voltage. The common-mode voltage V_{no} is computed as the arithmetic average of the three phase voltages:

$$V_{no}=\frac{U_{AO}+U_{BO}+U_{CO}}{3} \tag{1}$$

From (1), it can be derived that the CMV has seven discrete levels: 0, ±E/3, ±2E/3, ±E, ±4E/3, ±5E/3, ±2E.

2.2 CMV Suppression Strategy of the Novel SVPWM Algorithm

The novel SVPWM algorithm screens the 125 voltage vectors generated by conventional SVPWM and synthesizes the reference voltage vector using only 19 zero-CMV voltage vectors, thereby eliminating the CMV and substantially reducing the computational burden. Meanwhile, redundant switching states are used as compensation to balance the voltage across DC-link capacitor. However, as larger voltage vectors are unavailable, the linear region of the novel SVPWM shrinks compared with conventional SVPWM, and the ratio of their linear regions is 0.866 [4]. The implementation of the novel SVPWM algorithm incluses sector partitioning, sub-triangle identification, duty-ratio computation, switching-sequence generation, control-signal generation, and redundant switching-state selection. The reference voltage vector Vref is expressed as:

$$V_{ref}=V_{\alpha}+jV_{\beta} \tag{2}$$

V_{α} and V_{β}represent the components along the α and β axes of the reference vector, respectively. The novel SVPWM algorithm redefines the sector partitioning. Sector I spans from -π/6 to π/6, and the remaining sectors are obtained by successive counterclockwise rotations of π/3. Each sector is further divided into four sub-triangles, Δ1, Δ2, Δ3, Δ4. The sub-triangle can be identified according to the following rules (taking Sector I as an example):

If V_{ref} is located within Δ1, the following condition are satisfied: $V_{dc}\geq 3V_{\alpha}/2$; $V_{\beta}\leq 1$

If V_{ref} is located within Δ2, the following condition are satisfied: $V_{dc}\geq 3V_{\alpha}/2$; $V_{\alpha}/3-V_{\beta}/\sqrt{3}\geq -1$; $V_{\alpha}+\sqrt{3}V_{\beta}\leq 1$

If V_{ref} is located within Δ3, the following condition are satisfied: $V_{dc}\geq 3V_{\alpha}/2$; $V_{\alpha}/3-V_{\beta}/\sqrt{3}\leq -1$

If V_{ref} is located within Δ4, the following condition are satisfied: $V_{dc}\geq 3V_{\alpha}/2$; $V_{\alpha}+\sqrt{3}V_{\beta}\geq 1$

The identification rules for the other sectors are analogous. When the reference vector falls within a given sub-triangle, the reference vector V_{ref} is synthesized using the three vertex voltage vectors V_1, V_2, V_3:

$$V_{ref}\cdot T_s=V_1\cdot T_1+V_2\cdot T_2+V_3\cdot T_3 \tag{3}$$

$$T_s=T_1+T_2+T_3 \tag{4}$$

T_1, T_2, T_3 are the respective dwell times for V_1, V_2, V_3, within one switching period T_s. Using (3) and (4), the dwell times and duty ratios are derived for synthesized vectors, based on which the switching sequence is generated.

The novel SVPWM algorithm balances capacitor-voltage by controlling redundant switching states. First, signals controlling the voltage across the flying-capacitor and the voltage across the DC-link capacitor are generated according to the following equations:

$$\Delta V_{fj}=V_{fj}-\frac{V_{dc}}{4}(j=a,b,c) \tag{5}$$

$$SigFly_j=\Delta V_{fj}\cdot i_j(j=a,b,c) \tag{6}$$

$$\Delta V_o=V_{c2}-\frac{V_{c1}}{2} \tag{7}$$

$$SigDC_j=\Delta V_o\cdot i_j\cdot V_j(j=a,b,c) \tag{8}$$

ΔV_{fj} is the voltage deviation of flying-capacitor; V_{fj} represents the voltage of phase-j across the flying-capacitor ; V_{dc} denotes the voltage of DC-bus; i_j is phase-j current; $SigFly_j$ represents the control signal for the voltage across the flying-capacitor ; ΔV_o is defined as the neutral − point voltage error.; V_{c1}, V_{c2} are the DC-link capacitors(C_1, C_2) voltages; V_j is reference voltage of phase-j; $SigDC_j$ is the signal controlling the voltages of DC-link capacitor. Redundant switching states are then selected according to the control signals. When $SigFly_j>0$, $SigDC_j>0$, the switching state is selected from the set {V0, V1, V3, V4, V5, V7};conversely, when $SigFly_j<0$, $SigDC_j<0$, the switching state is selected from {V0, V2, V3, V4, V6, V7}. In this manner, the capacitor voltage is balanced by charging or discharging the flying capacitor.

3. Simulation-Based Case Verification

To evaluate the CMV suppression capacity of five-level ANPC inverter, this paper compares three representative modulation strategies: conventional SHEPWM, conventional SVPWM, novel SVPWM, in terms of CMV magnitude, output-voltage quality, and capacitor-voltage balancing capability.

3. 1 SHEPWM

To prove the effectiveness of SHEPWM algorithm, Dai tested a five-level ANPC inverter modulated by SHEPWM in a MATLAB/Simulink simulation[5]. The simulation parameters were set as follows: DC-side voltage V_{dc}=1000V; a three-phase Y-connected balanced RL load with R=10Ω, L=1mH; and an AC-side frequency f=50Hz.

The results show that the line-to-line output voltage waveform consists of nine voltage levels, exhibits no voltage degradation, and has favorable harmonic performance. The maximum CMV amplitude at the inverter output is $V_{dc}/3$, approximately 333.3V. Although conventional SHEPWM provides a certain degree of CMV suppression, its suppression remains markedly inferior to that of the novel SVPWM, with the amplitude being approximately one order of magnitude higher.

3.2 Conventional SVPWM

To assess the performance of conventional SVPWM, the following observations are summarized from simulation results reported by Liu, Li, and others [4,6]:

From the perspective of the CMV waveform, the maximum CMV amplitude under conventional SVPWM is $5/6V_{dc}$. The CMV amplitude is relatively high, and spikes and abrupt transitions are more likely to occur during switching transitions.

From the perspective of flying-capacitor voltage balancing, under steady-state operation with conventional SVPWM, the flying-capacitor voltage is approximately 20V with a ripple of about 2V, which is far greater than the specified flying-capacitor ripple threshold of 0. 5V. For the DC-link capacitors, the steady-state voltage ripple is approximately 0.5V. Overall, conventional SVPWM still exhibits limitations in CMV suppression and capacitor-voltage balancing.

3.3 Novel SVPWM

To prove the effectiveness of novel SVPWM strategy, Liu tested a five-level ANPC inverter modulated by the novel SVPWM in a MATLAB/Simulink simulation[4]. The simulation parameters were as follow: V_{dc}=100V; a three-phase Y-connected balanced RL load with R=10Ω, L=1mH; flying-capacitor ripple threshold $\Delta V_{f,th}$=0.5V; and AC-side frequency f=50Hz.

The simulation indicates that, from the perspective of the CMV waveform, the CMV amplitude is $0.03V_{dc}$, approximately 3V, indicating that the novel SVPWM effectively suppresses the output CMV. From the perspective of the output-voltage waveform, the line-to-line output voltage consists of nine levels and closely approximates a sinusoid, with no voltage degradation; the total harmonic distortion is THD=2.77%, indicating favorable harmonic performance and high waveform quality. Notably, the novel SVPWM suppresses CMV without sacrificing the output quality.

From the perspective of flying-capacitor voltage balancing. When the system is under steady-state operation, the flying-capacitor voltage is approximately 20V, and the voltage ripple is below 0.2V, which is lower than the ripple threshold (0.5V), indicating a stable flying-capacitor voltage and an effective balancing control. For the DC-link capacitors, the voltage ripple is approximately 0.15V, indicating an effective suppression of DC-link capacitor voltage fluctuations. When the initial voltages of C_1, C_2 are respectively set to 60V and 40V, the circuit reaches steady state at approximately 120ms, and both capacitor voltages converge to the reference value of 50V, indicating that the strategy can regulate capacitor voltages even under nonzero initial conditions.

4. Comparison and Analysis

Based on the above results, the three strategies exhibit significant distinctions. In terms of CMV suppression, conventional SHEPWM limits the CMV amplitude to $V_{dc}/3$, indicating a certain suppression effect; however, it remains much higher than that achieved by the novel SVPWM. The CMV amplitude of conventional SVPWM can reach $5V_{dc}/6$, yielding an even higher peak, making its suppression capability the weakest among the three. By contrast, the CMV amplitude of the novel SVPWM is $0.03V_{dc}$, which can be regarded as approximately zero compared with the other two strategies, demonstrating superior CMV suppression capability.

In terms of capacitor-voltage stability, the conventional SVPWM exhibits a flying-capacitor voltage ripple of approximately 2V and a DC-link capacitor voltage ripple of about 0.5V, both exceeding the specified thresholds, indicating insufficient regulation of the voltages across the flying capacitor and the DC-link capacitors. By contrast, the novel SVPWM reduces the flying-capacitor ripple to below 0.2V and limits the DC-link ripple to approximately 0.15V, indicating a stronger capacitor-voltage stability. Considering both metrics, the novel SVPWM performs best in CMV suppression and capacitor-voltage balancing.

The novel SVPWM strategy achieves CMV suppression and a balance of capacitor-voltage by selecting zero-CMV vectors and applying redundant-state compensation. However, compared with conventional SVPWM, this method exhibits a reduced linear range, and the ratio of their linear regions is 0.866 [4]. To ensure that the reference voltage is synthesized by zero-CMV vectors, the novel SVPWM inevitably excludes nonzero-CMV vectors, shrinking the available region in linear modulation, which directly limits the capability for high-amplitude output.

To improve linear performance of the novel SVPWM strategy, a hybrid-vector strategy can be adopted to compensate the linear region: zero-CMV vector combinations are used when the demand for output voltage is low, and a simplified-vector-based ANPC CMV suppression strategy is employed when a larger output is required [7,8]. In this way, some low-amplitude CMV vectors are allowed to participate in synthesis, and the linear region can be expanded to some extent. Subsequently, capacitor-balancing control can be employed for correction, thereby achieving a trade-off between CMV suppression and output capability [9, 10].

5 Conclusions

This paper addresses the issue of the common-mode voltage (CMV) during PWM modulation in three-phase five-level ANPC inverters and reviews a CMV suppression scheme using a novel SVPWM strategy. The core idea is to select 19 zero-CMV vectors from the 125 voltage vectors of conventional SVPWM and reconstruct the space-vector diagram; on this basis, sector partitioning, region identification of the reference vector, duty-ratio computation, and switching-sequence generation are performed, thereby suppressing the CMV amplitude and significantly reducing computational complexity. In addition, to balance capacitor-voltage , this paper further summarizes a complementary control scheme based on redundant switching-state compensation: by constructing control signals for the flying- and the DC-link capacitors, the scheme guides preferential selection among redundant states to balance the voltage across the flying- and the DC-link capacitor.

Case-study results show that, relative to SHEPWM and conventional SVPWM, the novel SVPWM can markedly reduce the CMV amplitude and effectively suppress capacitor-voltage ripple, offering the advantage of simultaneously achieving CMV suppression and capacitor-voltage balancing. However, this paper also points out that the strategy entails inherent trade-offs. Since some high-amplitude voltage vectors are excluded, the linear range of the novel SVPWM is reduced compared with conventional SVPWM, which may limit output capability under high output-voltage demand.

Future work may proceed in the following direction: to address the issue of the reduced linear region, a hybrid-vector modulation strategy can be investigated—maintaining zero-CMV vector synthesis in the low-amplitude region while introducing low-CMV vectors in the high-amplitude region to expand the linear range. Overall, the novel SVPWM algorithm provides an effective way in CMV suppression while balancing capacitor-voltage in five-level ANPC inverters, and it is valuable for further engineering issues.

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