# From Logical Effort to Machine Learning: A Survey on Delay Modeling in Digital Circuits

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**Abstract.** As the process nodes of integrated circuits approach the nanoscale, precise delay modeling has become a key factor in determining the performance and reliability of chips. Traditional model-based methods, which rely on mechanism-based reasoning for modeling, have limitations. In contrast, the new modeling paradigm based on machine learning has significant advantages. However, the two approaches, starting from different paths, have different fundamental idea**s**. This paper takes the technological development process of digital circuit delay modeling as an example, reviews the development history and comparison of the classic logic effort theory and various popular machine learning techniques at present, and constructs a framework to analyze the differences between these two types of modeling methods from aspects such as modeling philosophy, accuracy and efficiency, interpretability, data dependence, and generalization ability. It is found from the principle that the two modeling ideas are not in a replacement relationship but complement each other. The traditional formula-driven method has high interpretability and is an effective method for precise simulation and design of core devices at the current stage; while the data-driven modeling method based on big data can obtain more accurate results by learning from large-scale data. From a practical perspective, the trend of big data and high computing power is unstoppable. Therefore, as the two continue to integrate, it will further promote the development pace. Eventually, it will drive EDA towards a more intelligent "AI-native" direction.

**Keywords:** Digital Circuit Delay Modeling, Electronic Design Automation, Graph Neural Networks, Timing Prediction, AI-Native Design.

## 1 Introduction

Integrated circuits (ICs) are the backbone of the information age. With the continuous progress in all application fields from mobile communications to high-performance computing, they have become one of the most important technological driving forces in the contemporary world. However, the continued shrinkage of devices to the nanoscale drives increasing complexity in chip design and drives up associated costs Within this context, the critical role of the Electronic Design Automation (EDA) toolchain stems from its decisive impact on a chip's final Performance, Power, and Area (PPA) [1].

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Accurate timing closure is essential to ensure the correct functionality and performance of the chip, playing a vital role throughout the EDA flow. Consequently, obtaining an accurate circuit delay model is of great significance. Logical effort distinguishes itself among traditional delay models through its simple and elegant linear formulation. This model facilitates rapid performance estimation in the early design stages, providing crucial optimization guidance and profoundly shaping CMOS design methodology [2]. However, as technology progresses into deep-submicron and nanometer nodes, interconnect delay becomes dominant. Concurrently, heightened process variations and intensified coupling effects exacerbate secondary physical phenomena—including source impedance, coupling capacitance, and power supply noise—rendering them more pronounced and nonlinear.All these factors lead to inherent errors in the accuracy of the original simplified logical effort model [3]. In response, researchers have developed more detailed equivalent circuit models, look-up tables, and empirical formulas to address these limitations [4]. Nevertheless, these improvements essentially constitute incremental patches within the traditional formula-driven paradigm. They not only increase modeling complexity but also fail to keep pace with the rapid evolution of process technologies. As a result, they are no longer sustainable in terms of accuracy, efficiency, and generalization.

This landscape is now being reshaped by the integration of artificial intelligence (AI) and machine learning (ML) into scientific computing, including EDA. For circuit delay modeling, ML introduces a paradigm shift towards data-driven approaches. By learning complex, nonlinear relationships from vast simulation or measurement datasets, models such as gradient boosting trees and neural networks demonstrate the potential to achieve prediction accuracy surpassing that of traditional methods. A particularly promising direction is the use of graph neural networks (GNNs), which offer a breakthrough by natively representing circuit netlists as graphs to inherently capture topological connectivity and physical proximity—key for timing analysis. Beyond specific models, the emerging concept of circuit foundation models aims to learn general circuit representations through self-supervised pre-training, enabling flexible adaptation to tasks like timing prediction. This indicates that EDA is moving from "AI-assisted" (AI4EDA) to "AI-native" (AI-Native) [5]. Although there have been numerous studies in the past that have improved classic models or developed new ML models, such as using GNN for post-layout delay prediction, or comparing a certain ML method with a specific traditional method, there are still few studies that summarize and generalize the overall development of delay modeling from the "logical effort era" to the "machine learning era" and the two heterogeneous paradigms [6]. The essential differences between the two paradigms have not been thoroughly analyzed and discussed. Under such circumstances, a systematic review will undoubtedly enrich scholars' understanding of this technological change and help engineers and scholars better choose appropriate methods or combine different models for specific scenarios to further improve accuracy or interpretability.

To fill this gap, this review paper aims to clarify the development process of digital circuit delay modeling, from the classic logical effort-based modeling method to traditional model methods that can address nanoscale challenges, and ultimately to the new machine learning-based modeling paradigm. This paper constructs an overview of the overall technological evolution from the dual perspectives of historical review and multi-faceted comparative analysis. Building on this foundation, it proposes a comprehensive analytical framework to compare traditional and machine learning methods across key dimensions: modeling philosophy, accuracy and efficiency, interpretability, data dependency, and generalization capability.

Based on this, the research objectives of this paper are as follows: First, to clarify the value of logical effort and its fundamental limitations due to advanced processes; second, to organize traditional models and clarify the development trajectory and existing problems of traditional models; third, to introduce in detail the application of machine learning methods in delay modeling from three aspects: technical points, application cases, and paradigm shifts; fourth, to objectively compare the advantages and disadvantages of the two methods and their suitable application scenarios; fifth, to look forward to future research directions, such as data-efficient learning, explainable AI (XAI), and multi-physics field collaborative optimization.

## 2 Classic Delay Model: The Era of Logical Effort

### 2.1 The Basic Principles of Logical Effort

In the early days of EDA development, a primary function of design tools was to estimate digital circuit performance using classical delay models. The core value of these models lies in incorporating simplified physical abstractions, thereby providing designers with intuitive performance estimates for rapid preliminary design choices. Notably, the logical effort model is a very representative simple linear expression. This model directly decomposes gate delay into the product of logical effort and electrical effort, allowing designers to compare the different structures of various circuits from the very beginning without going through the cumbersome simulation process [7].

### 2.2 Advantages and Historical Value

The merit of the logical effort model lies in its simplicity and inspiration. At larger process nodes (such as tens of nanometers), it only focuses on gate delay and neglects the influence of interconnects. It omits all the physical details of the devices, allowing designers to focus more on achieving the optimal logic topology, that is, which gates should be larger and how many levels of devices should be connected in series. The CMOS design philosophy guided by this understanding had a significant impact on the CMOS design methodology at that time.

### 2.3 Inherent Limitations and Challenges

However, the logical effort model operates based on multiple assumptions and only considers the impact of interconnect delays in a basic manner. The significant increase in interconnect resistance and capacitance at deep-submicron and smaller nodes leads to wire delay exceeding and becoming dominant over gate delay. Moreover, this model cannot account for increasingly prominent nonlinear physical phenomena, such as process variations, voltage drop, temperature fluctuations, and transistor coupling effects. Consequently, it fails to accurately predict the real performance of modern nanoscale chips.

## 3 Classic Delay Model: The Era of Logical Effort

### 3.1 Complex Effects Brought by Nanoscale Processes

The core issue of nanoscale process scaling exposes and exacerbates the limitations outlined in Chapter 2, posing fundamental challenges for delay modeling: First, the proportion of

interconnect delay significantly increases and may even become dominant; second, minor variations in transistor size can cause large variations in electrical parameters (process variations); third, in high-density scenarios, the mutual coupling between wires leads to increased fluctuations in the delay of individual wires. These factors collectively contribute to the nonlinearity, statistical nature, and context dependence of circuit delays.

### 3.2 Evolution and Improvement of Traditional Models

To address the above challenges, traditional models based on "formula-driven" approaches have evolved. Meanwhile, the industry has developed more detailed equivalent circuit models, which store precise delays of standard cells under various conditions in large lookup tables. Additionally, more complex dynamic delay models (IDM) have emerged, capable of more accurately simulating signal degradation and other functions, with theoretical simulation accuracy approaching that of physical systems. The aim of these studies is to make the models more consistent with physical systems, increasing their complexity and the amount of data they contain.

### 3.3 Bottlenecks in Evolution

However, this approach hit a ceiling relatively quickly. The complexity of the models grew rapidly, and constructing lookup tables covering all process corners required significant costs. Even more fatal was the lack of generality in such models; models adjusted for a specific process node were difficult to transfer to other nodes and had to be redone from scratch. In other words, these methods were like "patching" within the original system, inevitably constrained by the original design framework and unable to respond promptly and effectively to the rapid iteration of technology and products. This created an opportunity for the emergence of the new data-driven paradigm.

## 4 Classic Delay Model: The Era of Logical Effort

### 4.1 Paradigm Shift: From Auxiliary Tools to Core Drivers

The development of artificial intelligence and machine learning has brought about a paradigm-level change to circuit delay modeling. Machine learning offers a brand-new "data-driven" approach to obtaining complex mappings between inputs and outputs using data, largely avoiding the difficulties of constructing physical models through EDA methods. Therefore, in the context of AI assisting EDA development to solve individual problems, it has entered a new era based on learning and opened the door to entirely new AI-native design processes.

### 4.2 Key Technical Paths

Current research mainly follows several technical paths:

Supervised Learning Predictive Models serve as the most direct form of application by learning the mapping between features and delays from annotated data. Two representative case studies are outlined below:

The SLoT method primarily targets the prediction of dynamic timing errors in functional units. Its core technique employs a Random Forest classifier, which takes features such as input

operands and circuit toggling activity as input to accurately predict potential runtime timing violations. This approach demonstrates the potential of supervised learning for dynamic timing verification [8].

The AiMap+ method is specifically designed for cell delay prediction to optimize the synthesis flow. It utilizes customized attention mechanisms and a custom neural architectures architecture to predict delays. These predictions are then used to guide the technology mapping step in logic synthesis, significantly improving the quality of the output circuit [9].

Graph neural networks: Since circuit netlists are inherently graph structures, using GNN for timing prediction is a recent breakthrough. For instance, a GNN-CNN hybrid model is used to predict path delays and flip times in the pre-routing stage, and this is integrated into commercial EDA tools to improve timing convergence. PreRoutGNN first conducts a global circuit pre-training and then uses a graph partitioning strategy that retains sequence to achieve more accurate pre-routing timing slack prediction. Additionally, a specialized multi-task learning strategy for post-layout GNN timing prediction has been proposed, which further improves the prediction accuracy and efficiency of GNN by jointly predicting multiple related timing parameters [10].

Frontier exploration: Research in multimodal and foundation models is in its infancy, but efforts have already begun to explore how to build more powerful models that integrate more types of data modalities. A pioneering example is the MOSS framework constructs a multimodal representation for circuits. It achieves this by fusing two distinct data modalities: textual descriptions of the circuit's register-transfer-level (RTL) behavior, encoded by a Large Language Model (LLM), and its structural netlist represented as a graph, encoded by a Graph Neural Network (GNN). This integration of high-level functional semantics with low-level topological data has demonstrated superior accuracy in predictive tasks such as arrival time estimation [11].

### 4.3 Application Cases and Impacts

The aforementioned machine learning-based approaches have demonstrated significant potential. Both supervised learning models (such as SLoT and AiMap+) and GNN models (such as PreRoutGNN) have outperformed their traditional counterparts in terms of prediction accuracy. Previously, they were more like tools to assist engineering design work; now, they have evolved to continuously self-improve based on data and algorithms, becoming the driving force behind design. For instance, they can progress from estimating the delay of individual task units to the overall design of the entire process.

## 5 Classic Delay Model: The Era of Logical Effort

### 5.1 Multi-dimensional paradigm comparison

From the classic logical effort formula to today's various machine learning models, the essential change in digital circuit delay modeling has undergone a paradigm shift from "formula-driven" to "data-driven". There are certain disputes regarding the universality and applicability of the two paradigms. Therefore, this paper will respectively start from the perspectives of formulas and data, and on the basis of comparing the strengths and weaknesses of the two paradigms,

evaluate their overall advantages and disadvantages. Based on the six dimensions in Table 1 and considering the factors related to the development of delay prediction methods within the general framework of model evaluation, a comprehensive analysis will be conducted.

### 5.2 Dialectical View:

Compared with traditional implementation methods, there is no complete replacement relationship. They are paradigms that are respectively suitable for their own missions and complement each other. From the perspective of the requirements for models in the early stages of design exploration such as timing simulation and RTL optimization, the traditional rule-based methods cannot be completely replaced at present. The characteristics of high interpretability and low data dependence also make the traditional rule-based models still have an irreplaceable position in future design exploration, as they still provide designers with direct physical intuition. Moreover, this type of model is also one of the most effective data sources and the most suitable benchmark verification targets.

The greatest advantage of machine learning methods is that they can solve high-dimensional and nonlinear problems, and can also be used to capture difficult issues such as nanoscale interconnect coupling and process variations. They have great application potential when high precision is required (such as timing verification before sign-off and clock tree synthesis). Especially when using graph neural networks to solve circuit connection structures in circuit graph representation, this algorithm form is naturally well-suited. Currently, they are also one of the most important links to integrate data-driven approaches with knowledge in the field of circuit design [12-14].

It is not about one paradigm replacing others, but rather developing towards integration. This includes using machine learning techniques to provide more accurate scaling rules or compensation factors for traditional models; or developing machine learning models in a "white box" manner to enhance model interpretability. The ultimate goal is to achieve an adaptive modeling ecosystem where physical mechanisms and data intelligence are mutually complementary.

**Table 1.** Comparative Analysis of Delay Modeling Paradigms across Key Dimensions

| Comparison dimension | Traditional modeling methods (formula-driven) | Machine learning methods (data-driven) |
|---|---|---|
| Philosophy of Modeling | Physics/formula-driven: Explicit mathematical models derived from semiconductor physics equations and circuit theory, including logic effort or equivalent circuit models based on look-up tables, etc. | Data-driven: Read and learn from a large amount of simulation or measurement data to obtain the implicit mapping relationship from input features (topology, load, etc.) to output delay. |

| | | |
|---|---|---|
| Precision and efficiency | Early-stage estimation is efficient, but later-stage accuracy hits a bottleneck: In the early design stage (without layout and routing), it is possible to quickly obtain some trend-oriented guidance. However, at the nanoscale process nodes, continuously adding model complexity to approach a more realistic physical scenario (such as numerous look-up tables) comes with a significant characterization cost, and it becomes increasingly difficult to improve accuracy. | When there is sufficient data, more accurate methods can be used. After obtaining a sufficient amount of high-quality training data, the prediction accuracy can also be increased compared to traditional models. Meanwhile, for the entire sample set, the computational speed of methods such as dynamic networks and adaptive computing in cutting-edge research can also be improved [15]. |
| Interpretability | The model has a clear physical meaning and a definite mathematical expression. The designer can trace the cause of the delay, making it easy to understand and more convincing. | Generally low ("black box"): Unlike deep learning models, the internal decision-making process is difficult to directly understand [16]. This is also one of the reasons that have affected its application in important design stages. |
| Data dependency | Low: Almost no training data is required, relying on the pre-characterized parameters provided by the process library and physical formulas. | Extremely high: Severe reliance on large-scale, high-quality labeled datasets (from simulation or post-silicon measurements). The cost of obtaining, cleaning, and labeling the data is huge [16]. |
| Generalization | Stable within the defined domain but weak in cross-domain capability: Under certain process corners and design rule conditions, it remains correct within the existing models, but cannot be extended to new process corners or completely different circuit layouts. | Potential and challenges coexist: The application of techniques such as transfer learning and domain adaptation has a certain generalization ability, but the model performance is constrained by the distribution of the training data and is prone to errors on out-of-distribution data [17]. |
| Application maturity | Very mature: The current EDA tool chain in the industrial sector has been refined over several decades and has become a highly integrated mature product. | Previously, the main focus was on addressing specific issues by developing small products or tools. However, when it came to tasks like time series prediction and hot spot detection, these evolved into dedicated functions and eventually led to an AI-native design process [17]. Nevertheless, the entire end-to-end process has not yet been fully integrated. |

## 6 Conclusion

This survey has reviewed the historical development of digital circuit delay modeling techniques, tracing the evolution from the elegant logical effort paradigm to the promising data-driven paradigm. It clearly delineates the transformation from the modeling paradigm based on physical formulas to the data-driven paradigm. Traditional models, with their solid physical foundation and good interpretability, served as fundamental models for early design decisions. However, they encountered difficulties in terms of numerical accuracy and robustness due to the spatiotemporal cross-coupling and temporal nonlinearity in nanoscale processes. As a result, a large number of machine learning methods, such as graph neural networks, emerged. These methods can directly learn the complex mapping relationships of circuit structure and spatiotemporal behavior (delay) from data without solving formulas, breaking through the traditional accuracy ceiling. "Data-driven" is not simply "formula-driven", but rather forms a mutually reinforcing and complementary new pattern with "formula-driven" at different stages and abstraction levels.

Although machine learning has brought innovation to delay modeling, it is difficult to be fully integrated into production-level EDA processes. In the future, timing modeling that combines causal inference and explanation capabilities is expected to become the mainstream trend. Currently, most data-driven models present correlation relationships, but actual circuit delays are determined by physical causality. Future models should incorporate causal inference at a deeper level to uncover truly reliable causal relationships, overcome false correlations caused by factors such as process and load variations, and provide robust and generalizable prediction results.

Developing causal discovery and causal reasoning frameworks suitable for timing analysis is an important research direction. It is necessary to improve data and computational efficiency, overcome the difficulty of obtaining large amounts of labeled data, reduce dependence on large datasets, and actively conduct research on small sample learning, self-supervised learning/semi-supervised learning, and effective data augmentation algorithms. Adopting lightweight model structures and dynamic reasoning strategies to solve the computational challenges brought by massive circuits is also imperative. Promoting the development of Explainable AI (XAI) to gain the trust of design engineers and support decision-making is another direction that needs to be pursued. Increasing the interpretability of deep learning models is essential for machine learning to play a greater role. Understanding the logic of specific timing predictions of GNN-like models and relating them to physical properties of circuits can solve the problem of achieving "Trustworthy AI in EDA". Delay models are no longer just isolated prediction tools but also part of the AI-based design flow. First, explore foundational models, agents, self-learning/evolutionary algorithms, and other technologies to build systems that can simultaneously solve multiple objectives such as timing, power, and area, and can be iteratively improved, and achieve the leap from "tool automation" to "design intelligence".

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