Intelligent Adaptive VDD Scaling Architecture under the Breakthrough of Physical Limits

Lingyi Zhang[1]

a206751@siswa.ukm.edu.my[1]

Faculty of Engineering and Built Environment,Universiti Kebangsaan Malaysia,Bangi Selangor,43600,Malaysia[1]

Abstract. As Moore's Law continues to advance, integrated circuit process nodes continue to shrink. Power consumption and energy efficiency have become the primary bottlenecks restricting the improvement of chip performance. Power supply voltage (VDD) scaling is one of the core technologies for reducing chip power consumption and optimizing energy efficiency. Its applications always face a fundamental trade-off between performance delay and energy consumption. This article systematically reviews the evolution of VDD Scaling and Delay-Energy optimization techniques. It is divided into three key stages. First, the physical basis of the technology and its early theoretical construction are explained. Then, the core optimization methods in the era of process scaling are analyzed. Finally, the latest development trends in the post-Moore era will be discussed. By tracing the technological developments and key breakthroughs, this article provides researchers in related fields with a clear development framework and a well-defined road map for future research. It also provides theoretical reference and technical guidance for the design of next-generation high-efficiency integrated circuits

Keywords: VDD scaling, Energy efficiency optimization, Delay-Energy Trade-off technological development

1 Introduction

As global dual-carbon goals continue to advance, the demand for technological performance and computing power is also constantly increasing. Under dual pressure, energy efficiency computing is facing severe challenges. Its urgency for development has also increased significantly. On the one hand, the pursuit of efficiency in technological upgrades is increasing exponentially. The explosive growth in computing power at AI computing centers is driving a surge in electricity demand, and industrial manufacturing is increasingly reliant on high-power equipment [1]. These factors highlight the technological bottlenecks of high-density heat dissipation and the steady rise in energy consumption, making it difficult for traditional cooling and power supply models to keep pace with technological development. On the other hand, the constraints on emission reductions in the global carbon neutrality process continue to tighten.

ICMEEA 2026, April 24-26, Singapore, Singapore

DOI 10.4108/eai.24-4-2026.2364878

High-energy-consuming industries face bottlenecks in energy efficiency improvement and the rigid requirements of mandatory energy consumption limit standards. The conflict between traditional high-energy-consuming models and the need for green transformation is becoming increasingly acute. As a result, VDD scaling has become one of the most pivotal technologies to resolve these contradictions. Its quadratic relationship with dynamic power consumption has become a key core theoretical foundation for solving the energy efficiency dilemma. By indirectly changing the overdrive voltage and adjusting the power supply voltage, VDD scaling can dynamically adapt to performance and energy consumption. VDD scaling technology has become a key method to resolve the contradiction between high efficiency requirements and emission reduction constraints. However, its development process lacks a complete overview from theory to intelligent adaptive practice. Therefore, this article divides the evolution of VDD scaling technology into three core stages, using time as the main thread. The first stage consisted of theoretical foundation building and initial optimization before 2000. This phase focuses on verifying the power consumption formula and conducting preliminary exploration of static voltage regulation, thereby establishing the underlying logic for the technology application. The second phase, from 2000 to 2015, was a period of dynamic optimization and system-level expansion. This phase will shift the research focus to the implementation and cross-level collaborative optimization of Dynamic Voltage Frequency Regulation (DVFS) technology. Ultimately, this achieved an improvement in energy efficiency from individual devices to system architecture. The third phase, from 2015 to 2024, will be characterized by extreme-scale and heterogeneous integration. In this stage, which focuses on advanced manufacturing processes and heterogeneous computing scenarios, intelligent adaptive voltage regulation and multi-domain collaborative management have become the core technologies. By segmenting the process, we can clearly understand the internal logic and key milestones of technological evolution, and intuitively present the technological shortcomings and breakthrough directions at different stages. This provides a systematic and targeted reference framework for the subsequent innovative research and development and engineering practice of VDD scaling technology.

2 Theoretical basis and preliminary optimization (Before 2000)

2.1 1965 Moore's Law

In 1965, Gordon Moore proposed Moore's Law, which predicted the development of semiconductors [2]. Its core content is the formulation of original predictions. Assuming costs remain constant, the number of transistors that can be placed on an integrated circuit doubles every year, and chip performance will improve accordingly. Furthermore, it was proposed that this trend would continue for a long time. This prediction provides clear guidance for semiconductor process iteration and chip R&D direction. Furthermore, it also provides device-level support for subsequent VDD scaling requirements [3].

2.2 1974 Dennard’s scaling law

In 1974, Dennard's scaling law was published by Robert Dennard [3]. The core of this law is that as transistor size shrinks, its power density remains constant, and chip power is proportional to area. Specifically, when the linear size of a transistor is reduced by 30% (i.e., to 0.7 times its

original size), the area will be reduced by 50%. To maintain a constant electric field, the voltage is also reduced by 30% simultaneously. This results in a 65% reduction in transistor energy consumption and a 50% reduction in power consumption. At the same time, circuit delay is reduced by 30%, and operating frequency will increase by approximately 40%. Ultimately, with each generation of technology iteration, the chip's transistor density will double and the computing speed will increase by 40%, while the overall power consumption will remain unchanged. The Dennard’ s scaling law fills the gap in Moore's Law. This law clearly defines the relationship between size reduction and performance and power consumption, explaining "how multiple transistors translate into high performance". It supported the early development of chips. At the same time it was established the core theory of VDD scaling in relation to energy efficiency and delay balance.

2.3 1980-1990 Preliminary optimization

The period from 1980 to 1990 was the initial optimization phase of VDD scaling technology. At this stage, the gate dielectric thickness shrinks to the nanoscale, and the source and drain extensions become shallower, both of which work together to drive VDD down from 5V to 3.3V. This is both an inevitable adaptation to advancements in semiconductor technology and a key optimization for balancing power consumption and performance. Among them, the gate oxide layer is thinned to about 7NM with the process node and reduces VDD synchronously according to the constant electric field requirement. This avoids dielectric breakdown and maintains channel control capability by preserving gate capacitance, providing process support for voltage reduction. Shallower source and drain extension structures can suppress short-channel effects and enhance gate electrostatic control. This is suitable for low-voltage operation requirements, while complementing the performance of VDD reduction. Ultimately, the 3.3V voltage level strikes a balance between a safety margin for gate dielectric withstand voltage and board-level power supply stability. It also adapts to the compatibility requirements of older 5V systems. Furthermore, after the voltage drops from 5V to 3.3V, according to the power consumption formula P=CV^2f, the dynamic power consumption will be significantly reduced. This would perfectly solve the heat dissipation problem caused by the increased integration of transistors at the time. This series of optimizations not only made 3.3V the mainstream power supply standard for a long time to come [4].

2.4 1995 Further optimization

In 1995, VDD dropped to 2.5V, marking the beginning of the 0.25μm node in semiconductor technology [4]. This resulted in a low percentage of static power consumption. This is a key optimization for implementing the Dennard’s scaling constant electric field strategy. Its core is to solve the high electric field reliability problem in the 3.3V era through process improvement and circuit design adaptation. Simultaneously achieve a significant reduction in static power consumption.

With the process evolving towards 0.25μm, the gate dielectric is further thinned. Maintaining a voltage of 3.3V would exceed the dielectric tolerance limit and exacerbate the hot carrier effect. Therefore, VDD is synchronously reduced according to the constant electric field logic. During this period, lightly doped drain (LDD) and sidewall isolation layer technologies matured. This technique can weaken the strong electric field in the source and drain regions, reducing the damage to the gate dielectric caused by hot carrier injection. This allows the device to operate

stably even at a low voltage of 2.5V. Meanwhile, the gate employs a heavily doped polysilicon process to suppress the gate depletion effect [4]. This ensures that the gate's control over the channel does not weaken as the voltage decreases, laying a solid technological foundation for applications at 2.5V.

This optimization incorporates dual power reduction. First, based on the formula P=CV^2f, reducing the voltage from 3.3V to 2.5V significantly reduces dynamic power consumption. Secondly, the coordinated reduction of voltage and threshold voltage will effectively suppress sub-threshold leakage current. It achieved a significant reduction in static power consumption ratio. Furthermore, this voltage scaling reinforces the bond between VDD scaling and process iteration. This also validated the effectiveness of the technical approach of "process miniaturization - voltage reduction - power consumption optimization". This provided a practical paradigm for the subsequent evolution of 0.18μm and 0.13μm processes towards 1.8V and 1.2V voltages. This also supported the development of early microcomputers and other devices.

3 Dynamic optimization and system-level technologies (2000-2015)

3.1 2000 130nm and STI

In 2000, 130nm process technology was achieved through shallow trench isolation (STI), copper interconnect, and low-k technologies [5]. STI is the core isolation technology. This process reduces leakage current and parasitic resistance and capacitance by improving device isolation and interconnect structure. This alleviates the problems of performance degradation and power consumption increase under low VDD conditions. This allows the chip to maintain good speed and energy efficiency even under non-ideal voltage scaling conditions.

According to the constant electric field scaling theory, as device size decreases, VDD must be reduced simultaneously to maintain the electric field strength and control power consumption. However, at the 130 NM process node, due to the physical limitations of silicon, the threshold voltage cannot be scaled proportionally [6]. If VDD decreases excessively, it will cause an imbalance in the ratio of VDD to the threshold voltage. This leads to a decrease in drive current and a significant increase in circuit delay. Therefore, the scaling of VDD is limited to this process node. This makes it difficult to achieve ideal scaling with device size. However, non-ideal VDD scaling can further exacerbate leakage current problems due to changes in electric field distribution [6]. Furthermore, it can exacerbate current leakage problems. STI technology effectively suppresses parasitic leakage currents in adjacent devices and edge regions by providing high-quality device isolation. This mitigates the risk of leakage current caused by VDD inability to scale proportionally. The combination of these two technologies, under 130 NM process conditions, achieves a trade-off between device performance, power consumption, and circuit stability.

3.2 2003 DVFS

In 2003, DVFS technology became widespread thanks to the Intel Centrino platform, breaking the previous limitations of fixed VDD scaling. The shift from "statically fixed" to "dynamically adaptable" became a key turning point in the development of VDD scaling technology.

In previous processes such as 130nm, VDD scaling was limited to fixed levels and had adjustment lag. Most of them can only operate at a preset fixed voltage and cannot adapt to different loads. In 2003, Intel's Pentium M processor on the Centrino platform was upgraded with an enhanced version of Speed-Step technology. It enables DVFS to achieve dynamic scaling of VDD at multiple levels. It can switch between multiple pre-verified voltage-frequency combinations (OPPS) based on the laptop's load. Ultimately this enabled VDD scaling to achieve a precise match with the actual load for the first time. With the widespread application of DVFS, a hardware and software collaborative voltage regulation system is gradually taking shape. This provides system-level support for dynamic scaling of VDD. By deeply integrating a high-sensitivity power consumption monitoring module with the processor platform, the system can sense the CPU's operating status in real time. This allows it to quickly adjust the power supply voltage. This overcomes the response lag problem caused by hardware and software decoupling in traditional VDD scaling. This collaborative mechanism significantly improves the response speed of voltage regulation. This makes DVFS more suitable for dynamic, multitasking scenarios such as laptops [7].

3.3 2008-2009 ABB integration of DVFS technology

In 2008-2009, the reduction in device size under 90NM semiconductor technology led to prominent leakage current problems. To save energy, the equipment needs to reduce VDD to 1V for high performance and to 0.8V for low power consumption [7]. However, simply reducing the voltage can lead to problems such as insufficient transistor drive current and performance degradation. Meanwhile, the maturity of technologies such as threshold voltage optimization and circuit anti-interference design has precisely resolved this contradiction. This provides support for low-voltage solutions, and, combined with voltage and frequency regulation technology, further mitigates performance shortcomings. During this period, the industry also achieved the integration of Dynamic Voltage Frequency Scaling (DVFS) and Adaptive Body Bias (ABB) technologies. DVFS dynamically matches the power supply voltage with the operating frequency. Under high load, it increases VDD and frequency to ensure performance, and under low load, it decreases both to reduce power consumption [7]. In contrast, VBB (body bias) technology optimizes the threshold characteristics of a device by adjusting the body bias voltage of the transistor. These two factors respectively affect the system-level operating state and the device-level electrical characteristics. They have obvious complementarity [8]. Combining these two technologies at the 90nm process can achieve a 22-fold reduction in power consumption and leakage current. This technology maintains high computing demands in high-performance devices while keeping power consumption in the micro-ampere range in low-power devices [8]. This not only extends the battery life of portable devices, but also provides a reference paradigm for low-voltage, low-power designs in subsequent advanced processes.

3.4 2011 FINFET

In 2011, Intel first put the FINFET structure into mass production in its 22nm Ivy Bridge processor. It overcomes the technical bottleneck of planar transistors with its unique three-dimensional structure, successfully achieving high-performance output under low VDD. It also solved the current leakage problem [9].

The channel of a FINFET is a vertically protruding "fin" shape, and the gate surrounds the channel from three directions. Compared to traditional planar transistors, this three-dimensional

structure significantly improves the electrostatic control capability of the gate over the channel. Its three-dimensional encapsulation design can effectively suppress the short-channel effect that occurs after the transistor size is reduced. This makes current transmission more controllable and provides a structural basis for low VDD environments [9].

Intel has also optimized the manufacturing and adaptation details of FINFET for this mass production run. For example, yield can be improved by using dual-function gate technology and optimizing the gate stacking process, and transistor performance can be improved by using conformal doping technology [9]. This not only enabled stable mass production of the 22nm process, but also provided a reference for the industry to promote low VDD designs. FINFET has become the mainstream for advanced processes of 16nm and below, continuously driving the upgrading of chips towards low power consumption and high performance [9].

3.5 2012 multi VDD and multi VTH gate-level optimization techniques

In 2012, as chip manufacturing processes evolved to the 40NM/28NM nodes, the increased transistor density exacerbated aging effects such as bias temperature instability and hot carrier degradation. Multi VDD and multi VTH gate-level optimization techniques have matured as a result. The two work together to form a dual mechanism of "prevention + supplementation" to alleviate the delayed degeneration caused by aging [10]. Multi VDD technology prioritizes power supply based on gate-level module timing, allocating high VDD to critical paths to ensure drive speed. It also works with a voltage converter to solve the problem of signal compatibility across different voltage domains. Multi VTH technology relies on a multi-threshold transistor library to select low VTH transistors with fast initial switching speeds for the critical path. This is to offset the delay caused by the increase in threshold voltage after aging. This technology also uses high VTH transistors with low leakage current and strong anti-aging capabilities for non-critical paths, reducing static power consumption and aging rate. This collaborative approach leverages EDA tools to automate the clustering of gate-level modules and transistor replacement. This eliminates the need to significantly increase the chip area. Actual tests show that it can reduce the aging delay degradation of the circuit over its entire life cycle by more than 40%. At the same time, it reduces static leakage current on non-critical paths by about 50%. Therefore, this technology balances the requirements of high performance and low power consumption, becoming the mainstream solution for gate-level optimization at this process node.

4 Extreme scaling and heterogeneous integration(2015-2024)

4.1 2018 LPDDR5 VDD2 rail

The LPDDR5 memory released in 2018 adopts a dual VDD2 power rail design. Its core relies on the coordinated operation of the memory controller and the power management unit. It is also equipped with two independent power supply voltage domains. One set of standard voltage requirements to meet high bandwidth and high load scenarios such as large-scale games and high-definition video processing. Another set is designed for low-load scenarios such as standby and light data read and write operations, with even lower voltage requirements. This enables rapid switching of power supply voltage domains within nanoseconds based on real-time load conditions without interrupting basic memory operation. Compared to the single-rail fixed-voltage design of LPDDR4, this dual-rail design breaks through the limitation of "single voltage

adapting to all scenarios". It achieves precise voltage and load matching [11]. Since memory power consumption is positively correlated with the square of voltage. Switching to a lower voltage domain under low load can significantly reduce redundancy losses in both static and dynamic power consumption. Actual testing shows that, under the same load, this memory chip can reduce power consumption by approximately 20%–30% compared to LPDDR4. This reduces heat generation and improves the stability of equipment operation. With this feature, it can be better adapted to application scenarios of mobile devices such as smartphones and tablets. At the same time, this technology provides fundamental support for memory-level power consumption optimization in future mobile devices. It helps to handle more complex AI computing and multitasking needs.

4.2 2021 LVDD2h

The LVDD2H technology, which was implemented in 2021, is a low-voltage optimization solution that Micron specifically designed for LPDDR5X memory. Building upon the LPDDR5X architecture that splits VDD2 into the VDD2H high-voltage domain and the VDD2L low-voltage domain, it further reduces the VDD2H high-voltage range to 1.05V for high-frequency scenarios. Simultaneously, dynamic voltage and frequency switching technologies such as DVSC and EDVFSC are used to ensure power supply stability. This not only meets the performance requirements in the 8.533-10.7Gbps high-frequency range, but also achieves additional energy savings in high-frequency application scenarios based on the principle that power consumption is positively correlated with the square of voltage [12]. LVDD2H technology not only improves the heat dissipation performance of mobile devices and extends battery life, but also provides stable and low-power memory support for edge AI applications.

4.3 2023 3D chip stacking and Sip packaging technologies

In 2023, the integration of 3D chip stacking and SIP packaging technologies enabled precise VDD control at the component level. It provides key support for the implementation of artificial intelligence accelerators. 3D chip stacking technology stacks multiple independent dies vertically using methods such as through-silicon vias (TSVS) and hybrid bonding. This significantly reduces the interconnection distance between components [13]. SIP packaging technology relies on high-density substrates and silicon inter-posers to integrate chips and passive components of different processes and materials into a single package. The integration of these two elements creates a highly efficient heterogeneous integration system. The integrated components (such as AI computing dies, HBM memory dies, etc.) can be equipped with independent power supply units, along with a voltage management module. It can adjust the VDD voltage as needed according to the real-time load of different components. At the same time, short-distance interconnection reduces power transmission loss and ensures voltage control accuracy. This technical solution reduces the overall energy consumption of the AI accelerator and alleviates the heat dissipation pressure under high load through precise VDD control. It also solved the "memory wall" problem by leveraging the high-bandwidth interconnect of 3D stacking. Furthermore, it flexibly combines computing and storage components with optimal performance through heterogeneous integration. This allows it to adapt to different AI task loads, greatly improving the accelerator's design flexibility and operational stability.

4.4 2024 ultra-low VDD transistors based on spintronics

In 2024, an ultra-low VDD transistor based on spintronics was realized. Its core is to break away from the traditional framework of silicon-based devices that rely on electron charge to transmit information. This technology uses electron spin orientation as an information carrier. It achieves spin modulation through voltage-controlled magnetic anisotropy (VCMA) and the spin Hall effect. Based on this, it is combined with two-dimensional magnetic semiconductors or optimized magnetic hetero-structures [14]. Simultaneously, it achieves reliable information reading and writing by precisely adjusting the gate electric field to change the spin direction of the magnetic layer. Simultaneously, optimization of nanoscale material interfaces and lattice structures reduces spin scattering loss. Ultimately, an ultra-low write voltage of less than 0.1 volts was achieved. This design not just breaks through the bottleneck of traditional silicon-based transistors being limited by the "Boltzmann tyranny" and unable to significantly reduce voltage. It also significantly reduces Joule heat and energy consumption due to its ultra-low voltage characteristics. Simultaneously, by utilizing the high-speed transmission of spin signals to shorten the delay, the energy-delay product (EDP), a key indicator for measuring device energy efficiency and speed, is significantly optimized. Compared to traditional devices, this design exhibits superior overall performance [15]. It provides new hardware support for future high-density integrated circuits, edge AI computing and other scenarios that are sensitive to power consumption and require massive data processing.

5 Future Directions and Challenges

After 2025, VDD technology will achieve breakthrough development around three core directions: "ultra-low power consumption, precise control, and deep collaboration". Machine learning-driven dynamic voltage-frequency regulation (DVFS) prediction models will be fully implemented. The lightweight neural network integrated in the RTL design phase can learn multi-dimensional data such as workload, temperature, and latency. This achieves optimal proactive VDD prediction with nanosecond-level response. This technology can reduce device power consumption by more than 28% in scenarios such as automotive electronics and edge AI through multi-domain collaborative control. It will also combine quantification technology with carbon sensing scheduling to achieve a 45% reduction in energy consumption while ensuring the accuracy of AI models. At the same time, the deep integration of new materials and new structures will become a key support for the continued breakthrough of VDD to below 0.1V. Two-dimensional semiconductors (such as Bi_2O_2Se), high-k dielectric materials, and other materials will be combined with innovative structures such as gate-around-all-aspects (GAA) and three-dimensional stacking (M3D). This enables it to maintain high current density and device stability at ultra-low voltages. Ultimately, a collaborative and optimized system will be built across the entire chain of "devices-circuits-architecture-packaging". This system will drive the practical deployment of VDD with a voltage of <300mV in scenarios such as edge computing, autonomous driving, and IOT terminals. It even moves into lower voltage ranges, continuously breaking the limits of energy efficiency ratio.

6 Conclusion

VDD scaling technology has evolved from a simple design choice involving adjusting single circuit parameters to a complex system-level energy efficiency optimization solution. It integrates the requirements of circuit, architecture, algorithm and system levels. It can effectively address the core challenges of increased leakage power consumption and greater timing convergence difficulties at deep sub-micron and below process nodes. As a core supporting technology for improving chip energy efficiency, its efficiency improvement faces significant bottlenecks due to single-level optimization limitations. Relying solely on independent optimization at a single level is no longer sufficient to meet the diverse needs of scenarios such as heterogeneous computing and low-power IOT. Research has confirmed that cross-level collaborative design is the key to overcoming this bottleneck. Only by achieving deep linkage and parameter matching at all levels can the energy efficiency potential of VDD scaling technology be maximized. In the future, breakthroughs in this technology will heavily rely on the deepening of cross-level collaboration between circuits, architecture, algorithms, and systems. VDD scaling technology needs further refinement of the adaptation mechanisms at each level. Furthermore, its application scenarios can be expanded by combining advanced technological trends. It provides core support for the research and development of next-generation low-power, high-efficiency chips.

References

[1] S. S. Rajput, M. Saad, T. Sharma, 2025 Tu(r)ning AI Green: Exploring Energy Efficiency Cascading with Orthogonal Optimizations, https://arxiv.org/html/2506.18289v1

[2] G. E. Moore, "Cramming more components onto integrated circuits," Proc. IEEE, vol. 86, no. 1, pp. 82–85, Jan. 1998, doi: 10.1109/JPROC.1998.658762

[3] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," IEEE J. Solid-State Circuits, vol. 9, no. 5, pp. 256–268, Oct. 1974, doi: 10.1109/JSSC.1974.1050511

[4] P. H. Woerlee, C. A. H. Juffermans, H. Lifka, et al., A low power 0.25 μ m CMOS technology, in Proceedings of the 1992 International Technical Digest on Electron Devices Meeting (IEDM 1992), pp. 31 – 34 (1992), DOI:10.1109/IEDM.1992.307302

[5] K. K. Young, S. Y. Wu, C. C. Wu, et al., “A 0.13 μm CMOS technology with 193 nm lithography and Cu/low-k for high performance applications,” in *2000 IEEE International Electron Devices Meeting (IEDM) Technical Digest*, San Francisco, CA, USA, 2000, pp. 331–334, doi: 10.1109/IEDM.2000.904382.

[6] M. Bohr, “A 30 Year Retrospective on Dennard’s MOSFET Scaling Paper,” IEEE Solid-State Circuits Society Newsletter, vol. 12, no. 1, pp. 11–13, Winter 2007, doi: 10.1109/N-SSC.2007.4785534.

[7] W. H. Cheng, B. M. Baas, Dynamic voltage and frequency scaling circuits with two supply voltages, in Proceedings of the 2008 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2988 – 2991 (2008), DOI:10.1109/ISCAS.2008.4541648

[8] Gordon Gammie, Alice Wang, Minh Chau, et al., A 45nm 3.5G Baseband-and-Multimedia Application Processor using Adaptive Body-Bias and Ultra-Low-Power Techniques, in Proceedings of the 2008 IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 258 – 259 (2008), DOI:10.1109/ISSCC.2008.4523155

[9] C. Auth, C. Allen, A Blattner, et al., “A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors,” in 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 2012, pp. 131–132, doi: 10.1109/VLSIT.2012.6242496

[10] Heo, S., Lee, S., and Hwang, H., “Low-Power and High-Speed Ag_2S-Based Threshold Switching Device Enabled by Local Phase Transition-Assisted Filamentary Switching,” IEEE Trans. Electron Devices, vol. 72, no. 9, pp. 4916–4921, Sep. 2025, DOI: 10.1109/TED.2025.3592912

[11] Intel, 2025, 12th Generation Intel® Core ™ Processors, https://edc.intel.com/content/www/us/en/design/ipla/software-development-platforms/client/platforms/alder-lake-desktop/12th-generation-intel-core-processors-datasheet-volume-1-of-2/002/vdd2-dc-specifications/, 2025-08-20

[12] Micron Technology, 2022, LPDDR5X memory pushes the limits of what’s possible, http://www.shturl.cc/062ffedf426267574f29a027daa13fe5, 2022-02-01

[13] N. Chujo, K. Sakui, S. Tani Suga, et al., Bumpless build cube (BBCube) 3D: heterogeneous 3D integration using WoW and CoW to provide TB/s bandwidth with lowest bit access energy, in Proceedings of the IEEE 2023 Symposium on VLSI Technology and Circuits, pp. 1–2 (2023)

[14] P. K. Mishra, M. Sravani, A. Bose, et al., Voltage-controlled magnetic anisotropy-based spintronic devices for magnetic memory applications: Challenges and perspectives, Journal of Applied Physics, vol. 135, no. 22, 220701 (2024), DOI:10.1063/5.0201648

[15] Anupom Devnath, Junseong Bae, Batyrbek Alimkhanuly, et al., Ultralow-Power Circuit and Sensing Applications Based on Subthermionic Threshold Switching Transistors, ACS Nano, vol.18, no.43, pp.39872–39882, Oct. 2024, DOI: 10.1021/acsnano.4c08650