New Technologies of Power Transistors for Efficiency Increase of Power Converters: The Reliability Consideration

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Abstract. This paper proposes a methodology to study the reliability and failure analysis of new technologies of power transistors. The use of wide gap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) is now a good alternative to meet the integration requirements of energy conversion systems. However, the reliability of these components is a crucial issue. Aging in operating conditions is considered, associated with electrical measurements to highlight nondestructive degradations of the performance of studied transistors. A step of looking for failure mechanisms in the material is made in order to identify any physical degradation. The information collected provide the user with valuable data and help to make an optimum choice of the component which can be integrated into the equipment. The presented work proposes the description of a methodology that meets these requirements and shows the study of two technologies of power transistors used in new generations of power converters.

Keywords: Electronic reliability, failure analysis, power transistor, ageing tests.

1 Introduction

The total market for Silicon Carbide (SiC) power components will account for more than one billion US dollars (US $ 1 trillion) by Yole Development organization in 2022 [1]. Applications such as PFC / power supplies and photovoltaic inverters are now contributing to the growth of this market. Photovoltaic applications seem to largely integrate SiC products. Indeed, SiC solutions offer a better system performance / cost ratio for photovoltaic inverters. In the future, applications related to electric vehicles, rail and others will also contribute to the evolution of the market.

In this context, the new power transistor technologies, now available on the market, offer increased performance compared to traditional silicon components, in terms of high voltage, high temperature and high switching frequencies.

However, these new wide gap components show random degradation problem, and reliability studies are still needed to qualify these components [2], [3], [4], [5]. The approach by long-term testing under operating conditions remains essential for integrators.

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The components under test are then aged thanks to dedicated benches where the electrical and environmental measurements are monitored. Degradations are observed and recorded, non-destructive and microstructural analyzes are made in order to identify the failure mechanisms responsible for performance degradations.

This set of techniques is implemented in the GPM laboratory, for applications of microwave amplifiers and switching power transistors, the work is carried out in collaboration with academic and industrial partners from the aeronautics, automotive and renewable energy sectors [6], [7], [8], [9].

In this paper, we present the general methodology developed in collaboration with the research team and partners meeting the defined objectives. Afterwards, we develop two examples of studies which are based on SiC MOSFET (Metal Oxide Semiconductor Field Effect Transistors) and GaN power transistors for switching applications.

2 Reliability and failure analysis study procedure of next-generation power transistors

The proposed methodology is summarized in **Figure 1**, which provides an overview of the various stages of the study of reliability and physical failure analysis of wide gap technology transistors. The studied components come mostly from the commercial sector and, thereby, little prior knowledge is available concerning the operation and physical structure of these devices. The first step, identified as step 1, consists in searching, from the manufacturer's documents or data sheets, the electrical, physical, and structural characteristics of the DUT.

From the data collected, failure indicators are defined, and electrical characterization based on measurements are implemented by means of the development of specific benches, this is step 2.

In step 3, the operational conditions are established, the component is aged on the dedicated bench, according to a particular mission profile, the electrical parameters are monitored, and measurements of failure indicators are regularly performed after each aging phase. A specific bench equipped with current measuring probe up to 30 A is used to record the I-V static characteristics of the transistor under test, a commercial source meter is used to measure both low gate and drain leakage currents.

According to one or more criterion of variations of the measured parameters, typically a variation of 20% of the nominal value, the aging phase is stopped, and the step 4 then consists in decapsulating the resin or ceramic packaging by laser ablation and chemical etching. This delicate operation, must be performed in order to maintain the integrity of the component. The active chip of the component is then accessible for a visual investigation, then by optical microscopy, the extrinsic elements such as metal access surfaces and bonds are controlled.

In order to precisely locate a possible defect, the PEM (Photon Emission Microscopy) and Optical Beam Induced Resistance Change (OBIRCH) techniques complete the analysis at this stage. Step 5 is implemented with a level of investigation depending on the requirements of the study. Scanning or transmission electron microscopy tools can be used, associated with a

FIB tool (Focus Ion Beam) to explore the internal structure of the component at the ultimate scale of a few tens of nanometers.

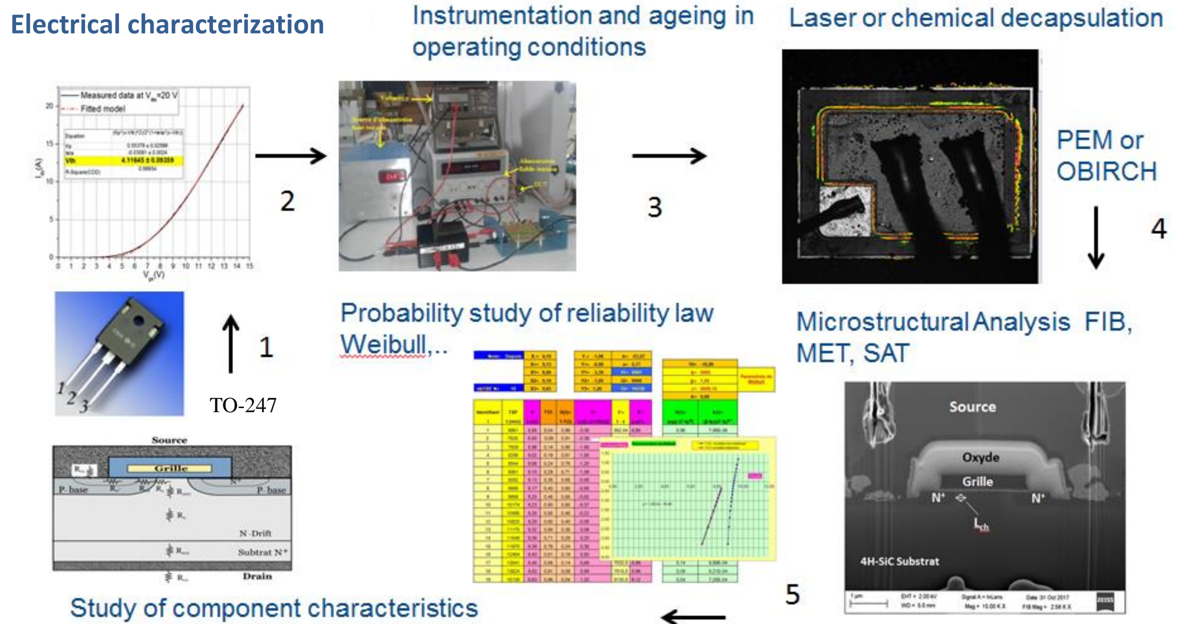

Fig. 1. Methodology to study reliability in operational conditions.

In order to meet the users requirements, study of reliability using Weibull law can be implemented in the methodology. The different parameters: Failure rate (Lambda), MTBF (Mean Time Between Failures) and MTTR (Mean Time To Repair) provide valuable information for system design and maintenance. The reference [10] describes reliability studies carried out on RFID tags, the performance of two tags of two manufacturers aged in temperature storage were compared.

These various steps make it possible to validate the study of the component in its mission profile, thus meeting the requirements of the user, but also to extract and analyze the physical defects at the origin of degradations of its characteristics. In the following paragraphs, we will develop examples of studies for new generations of SiC MOSFET and GaN power transistors, using the methodology described above.

3 Reliability and physical analysis of SiC power MOSFET failures for switching applications

Due to their interesting characteristics in thermal and in high level voltage domains, SiC MOSFETs are a promising technology. However, the feedback on their reliability is not as important as an older technology like Si, especially concerning the impact of ESD (Electro Static Discharge). This stress is important since the specific structure of SiC MOSFET may be sensitive to this kind of stress, and because electrostatic discharges are present at several places in the context of a power transistor.

The ESD appears when two objects with different electrostatic potentials get closer fast and generates a fast and important transfer of charges. This may also cause irreversible damage at manufacturing, handling or storage of an electronic device or component. The microelectronics industries are very concerned about this subject and are constantly looking for solutions, such as protection circuits, to control it and limit its consequences. An ESD test is also important to characterize the immunity of a transistor or a technology regarding this stress.

Several models of ESD have been developed and considered various contexts of stress. At first Human Body Model (HBM) simulates the electrical behavior of an operator standing in front of the table where the device is located and touching it with a finger [11]. This model is the most used since human is the main cause of ESD in industry. Usually, this simulation is achieved with an adapted couple resistor/capacitance. The Machine Model (MM) simulates the discharge produced by accumulation in a machine on a component [12]. This discharge is stronger than HBM since the electrical resistance of a machine is often very low. At least, Charged Device Model (CDM) considers a charge accumulated by the component itself during storage or manipulation confronted to a fixed potential of an external object (ground) [13].

For each discharge model, different tests protocols may be used in accordance with specific industrial standards like MIL-HDK, JEDEC, AEC, among others. For example, the ISO 10605:2008 describes tests to evaluate performances of electronic modules in road automotive context. This standard considers ESD appearing during assembly, due to maintenance staff or due to user. The tests in the ISO 10605 standard, which often involve an ESD gun comprising a R/C cell, use either a 330Ω or 2kΩ resistance, depending on the use of a metallic tools or not by user [14]. Several levels of severity are fixed by voltage from 2kV to 15kV.

When a MOSFET undergoes an ESD, a strong current is flowing during a few nanoseconds, which causes an important and local rise of temperature and various kinds of failures in the transistor structure [15], [16]:

- Filamentation: appearance of a conducting filament between source and drain
- Oxide breakdown: the gate oxide is destroyed by an overvoltage
- Hot carrier injection: nondestructive but modifies the isolating layers and the electrical characteristics of the transistor.
- Bonding breakdown: an overcurrent destroys the bondings by fusion.

The ESD stress implies also important consequences of the SiCMOSFET technology and test campaigns have to be realized to evaluate its impacts on a specific transistor family. The following parts present such a campaign on two generations of transistors of the same manufacturer, to understand evolution of ESD impact between them.

3.1 SiC MOSFETs under test

Among the leaders in SiC technology, the manufacturer Wolfspeed commercialized three generations of power transistors since 2011. Each generation improves the maximum drain current and the maximal case temperature, but valuable information is unavailable concerning ESD immunity under specific conditions.

Table 1. References of components involved in this study.

Generation	Ref.	I_{ds}(max)	V_{ds}(max)	Tc(max)
Gen2L	C2M0280120D	10 A	1200 V	150°C
Gen2H	C2M0160120D	19A	1200V	150°C
Gen3L	C3M0280090D	11,5 A	900V	150°C
Gen3H	C3M0120090D	23 A	900V	150°C

The following study involves the two last Wolfspeed generations. In table 1, letters L and H are indicating "Low" or "High" current transistors. In each generation, different references have various electrical characteristics and different power application. All these transistors are based on a VDMOS structure which is shown in **Figure 2**.

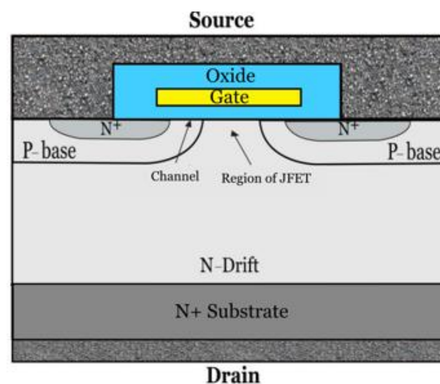

Fig. 2. Schematic structure of Wolfspeed transistors

3.2 ESD Tests

The ESD tests were realized on 8 components of 4 categories (2 of each) of Table.1 respecting ISO 10605 standard. An electrostatic gun shown in **Figure 3** was used with a couple 2kΩ/330pF simulating an HBM discharge model.

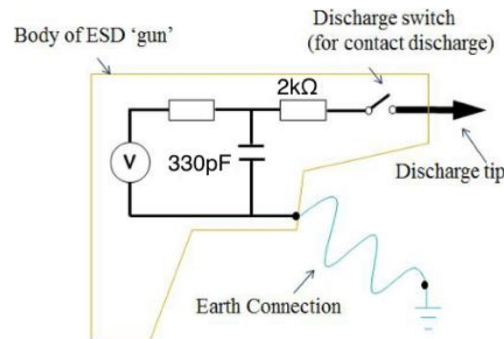

Fig.3. Electrostatic Gun schematic

Stress of 8kV and 15 kV were applied repeatedly (4 times and up to 12 times on some transistors) on gates pin to evaluate gate oxide robustness and to appreciate evolutions between generations. Drains and sources pin were leaved open.

3.3 Results and analysis

Electrical measurements have been achieved before and after stress in order to estimate discharge impact on the behavior of the transistors. This comparison yields interesting information concerning the failures that may appear in the devices.

At first, saturation current I_{dsat} and on-state resistance $R_{ds(on)}$ are determined from the output characteristics ($I_{ds} = f(V_{ds})$) of the transistors. These parameters show few variations due to the stress ($R_{ds(on)}$ decreases and I_{dsat} increases, about 1% for both) on two generations except for a transistor Gen3L that received a 15kV stress where I_{ds} decreases and $R_{ds(on)}$ increases about 10% for both.

Leakage currents I_{gss} and I_{dss} were measured on a specific bench and schematic. I_{gss} increases a lot for both generations (average values about 3000% for Gen2 and 10000% for Gen3). I_{dss} increases about 100% for Gen2L and Gen3L but doesnot change significantly for Gen2H and Gen3H.

Threshold voltage V_{th}, transconductance K_p and transverse electrical field θ were determined from output characteristics with a Levenberg-Marquardt Algorithm **[9]**. The stress induces an average decrease of 2% for V_{th} on both generations, with highest values on Gen3L transistors. K_p and θ increase slightly for both generations.

At least, C-V measurements on gate-source, drain-source and drain-gate diode were performed on a specific bench, to get more information on failure process during the stress. The measured capacitance variations globally reveal the appearance of positive traps in the oxide volume. The effect of these traps is in good accordance with the decrease of V_{th} and the increase of I_{gss}.

All the variations observed yields to a conclusion that the ESD stress mainly affects the oxide volume near the gate of the transistors and also the input parameters of the transistor.

High current transistors (Gen2H and Gen3H) are less sensitive to this stress and no significant difference seems to appear between the two generations.

4 Switching GaN transistor for energy conversion applications.

The GaN technology is another alternative to SiC for increasing the integration of energy conversion devices. Thanks to these new devices, the automobile market anticipates an integration density multiplied by 3, with a loss reduction of 50% and a cost reduction of 20% [17]. The advantage of the GaN technology compared to silicon substrate results from the ability to operate at: high frequency due to increased velocity saturation, high temperature and high voltage due to the large band gap material [18], [19]. In this paper, we use anew commercial component from GaN systems manufacturer, whose reference is GS66508P, it is a p-type gate normally-off which operates in the 650V/30A range, its main characteristics are given in reference [20].

4.1 Aging tests with switching mode

The successive aging steps and the dynamic measurements are carried out by means of a dedicated switching bench described in reference [9]. **Figure 4a.** shows a view of this setup. This includes two transistors noted DUT_C and DUT_V switching the DC source voltage to fix the desired electrical parameters in two states. The DUT_M is alternately subjected to a high current by the mean of DUT_C, then, out of conduction, subjected to an electric field by DUT_M.

The aging bench eliminates the need for significant energy consumption because, with this original operating principle, no power load is needed. To ensure this operation, the PWM_1 and PWM_2 signals are two complementary pulses whose pulse width can be modulated. The bench is instrumented using a digital oscilloscope connected to measurement probes.

Also, it places similar electrical waveforms on DUT_M, which could exist in a large class of power management products such as DC-DC power converters. Moreover, it enables dynamic measurements, like: dynamic resistance (R_{dyn}) and switching times (tr and tf).

The DUT_M current and voltage experiment waveforms are shown in **Figure. 4b**. As can be observed, V_{DS} switch from 1.14V to 24V with a rise time equals to 53.46 ns and I_{DS} switch from 0A to 14A with a rise time equals to 3.94 µA. The studied switching conditions are chosen so that the DUT_M switches in its Safe Operating Area (SSOA).

4.2 Degradation detection and measurements caused by the aging phase

The studied component is aged in operating conditions with the bench described in **Figure 4a**. At regular time intervals, measurements are made to assess the evolution of some relevant and significant electrical parameters. To meet this goal, the threshold voltage V_{th} is extracted using the Extrapolation in the Linear Region (ELR) method. The transconductance is defined as the maximum first derivative of the input characteristic in the saturation region, and

the on-state $R_{DS(ON)}$ is defined as the inverse of the slope of output characteristics in the linear region.

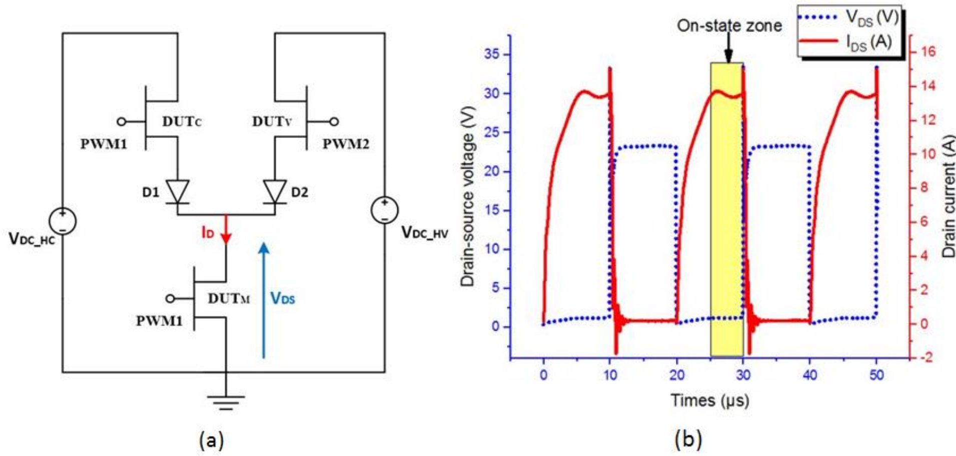

Fig. 4. (a) Setup for ageing the device in operational conditions. (b) Chronograms for I_{DS} and V_{DS} measurements.

The switching frequency is set at 50 kHz with a duty cycle of the control signal equals to 50%. The study component is thus aged at the limited Safe Operating Area (SSOA) for more than 1000 hours in operating conditions on the dedicated bench.

To ensure that the aging of the DUT_M respects the SSOA, the measurements of the junction temperature T_J and the dynamic $R_{DS(ON)}$ are performed, the temperature T_J is estimated using the thermal model and thermal Ohm's law of DUT_M package mounted on a PCB and a heat sink.

From experimental measurements chronograms, the power loss (P_{loss}) is calculated which is equal to 16.68 W, the corresponded T_J is calculated equal to 86 °C which is blow the allowable T_J=150°C from the data sheet.

Table 2 summarize the values of $R_{DS(ON)}$, g_m and I_D before and after 1008 hours of aging DUT_M under the switching conditions.

Table 2. 1008 hours aging results for the DUT.

	$R_{DS(ON)}$ mOhms	g_m(S)	I_{DS}(A)
t = 0	43.04	24.88	17.01
T=1008 hours	54.71	22.42	13.21
Degradation (%)	27.11	9.88	22.33

Drain current measurements, after each step of aging, highlight the effect of aging of the DUT operating at the limit of the SSOA. The effects are a decrease in the efficiency of DC-DC power converters, due to an increase of the power losses of the DUT_M.

Based on measurements of the aged component, considering the model provided by the constructor lacking precision, an improved SPICE model is defined taking into account the degraded performance of the component. Also, we studied the effect of aging GaN HEMT under SSOA on the efficiency of a DC-DC power converter by a simulation approach. A 12/24 V buck converter is designed which has an output power equals to 180 W in a load.

The purpose is to model the aging of the DUT_M in order to evaluate the effects of aging the GaN HEMT under SSOA on the power efficiency of the DC-DC boost converters by a SPICE simulation approach. By applying this methodology, an average decrease of the efficiency of a DC-DC boost converter equals to 4.55% after aging state for different output current. The decrease in efficiency is accompanied with an increase of conduction power loss in the DUT_M after aging, the average increase in conduction power losses equals to8.55%.

5 Conclusion

The SiC and GaN technologies allow to overcome the limits in the use of energy conversion systems by providing greater energy efficiency, including increased integration and higher switching frequencies.

The challenges are to reduce the size of the power converters and to increase energy efficiency while reducing costs. In the field of transport, the automotive sector, is addressed with the development of hybrid and electric vehicles. The aircraft industry is driven by the demand to optimize aircraft performance, the decrease of operating and maintenance costs and the reduction of gas emissions, are the most demanding sectors of energy efficiency. The field of energy conversion brings the development of the new technology for semiconductor market.

The SiC MOSFET 1200V and the GaN 650 V transistors presented in this paper are two new generation components available on the market. They are accessible to integrators and already offer an alternative to the requirements of integration of energy conversion systems. However, they continue to be the subject of reliability and failure analysis studies, in order to improve their performance and to qualify them in operational conditions for various application sectors.

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