

Design of a Microstrip Balanced Amplifier Using the Wilkinson Power Divider

Amine Rachakh¹, Larbi El Abdellaoui², Ahmed Errkik³, Abdelali Tajmouati⁴, Mohamed Latrach⁵

{rachakh.amine1@gmail.com¹, elabdellaoui20@hotmail.com², ahmed.errkik@uhp.ac.ma³}

^{1,2,3,4}MEET Laboratory, FST of Settat, Hassan 1st University, Morocco

⁵Microwave Group, Ecole Supérieure d'Electronique de l'Ouest, Angers, France

Abstract. The broadband bandwidth of power amplifiers is one of the most important features that restrict its wide usage. This work presents a new structure of a broadband power amplifier suitable for ISM band. The proposed amplifier, which is realized with two identical single-stage amplifiers and two power dividers on low loss Epoxy (FR4) substrate with a substrate thickness of 1.6mm and a relative permittivity equal to 4.4. The proposed PA demonstrates a power gain of 16 dB at 2.45GHz. The input and output matching impedances are better than -15dB throughout the band. the power amplifier delivers a maximum output power equal to 16dBm with a flat gain varied between 15-16dB.

Keywords: Power Amplifier (PA), Gallium Arsenide (GaAs) , Field-effect transistor (FET), Microstrip technology , Advanced Design System (ADS).

1 Introduction

Broadband power amplifiers are critical circuit components for wireless communication systems, as well as cellular telephone applications. The broadband power amplifier should be designed to trade-off the power gain, output power, return loss and bandwidth. The broadband amplifier can be designed by utilizing the compensation network, but the mismatching will raise the VSWR [1]. When VSWR improve, the power gain and output power will deteriorate. The balanced power amplifier can equilibrium these performance parameters for its coupling circuit at the input and output ports.

Conventionally, balanced power amplifiers are made up by associating two identical amplifiers with branch line couplers at the input and output as illustrated in **Figure 1**. Based on the circuit configuration illustrated in **Figure 1**. Balanced power amplifiers have been realized with various types of couplers, such as broadside couplers [2–3], branch-line couplers [4–5], and Lange couplers [6– 7].

Various technologies are utilized in designing PA for several applications in wireless communications. For microwave frequencies, the GaAs MESFET technology appears to be prominent. This is owing to it has superior electrical characteristics at high frequencies, which helps to transmit high output power with a minimum parasitic loss. Moreover, its inherent characteristic of low resistance and low drain-source offset voltage [8-10].

Following these studies, this paper presents a new design of a balanced power amplifier by using a Wilkinson power divider. To improve circuit performance, the microstrip lines technology is used. While in the design process, the advanced design system (ADS) software is utilized, and it can also give simulation result of amplifier final circuit such as power gain, reflection coefficient, isolation coefficient, and output power.

2 Broadband Power amplifier design methodology

The balanced power amplifier is a convenient method for realizing a broadband PA that has good performances especially in input/output return loss and flat gain. The balanced amplifier is constructed with two single-stage power amplifiers and two hybrid couplers as shown in **Figure 1.**

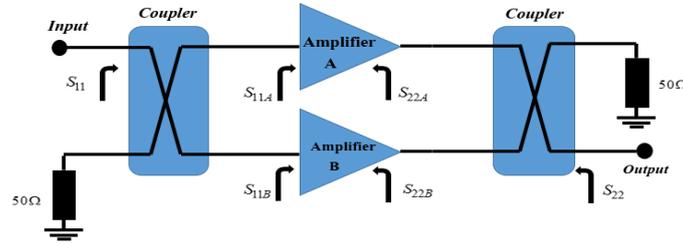


Fig. 1. Conventional topology of balanced amplifiers with hybrid couplers.

Considering the balanced amplifier architecture in **Figure 1.** the coupler on the left is working as the power divider and the one on the right is work as the power combiner, while the two amplifiers (Amplifier-A, Amplifier-B) are identical and have S-parameters $[S_A]$ and $[S_B]$ respectively. Thanks to the phase difference of the couplers, the two PA work in quadrature. it can be demonstrated that $[S]$ parameters of the overall circuit (the balanced power amplifier are **[11]** :

$$|S_{11}| = \frac{1}{2} |S_{11A} - S_{11B}| = 0 \quad (1)$$

$$|S_{12}| = \frac{1}{2} |S_{12A} + S_{12B}| = S_{12A} \quad (2)$$

$$|S_{21}| = \frac{1}{2} |S_{21A} + S_{21B}| = S_{21A} \quad (3)$$

$$|S_{22}| = \frac{1}{2} |S_{22A} - S_{22B}| = 0 \quad (4)$$

It is clear from equations (1 - 4), that the magnitude of S_{11} and S_{22} will turn zero. By adopting the balanced configuration, excellent input and output matching conditions can be acquired simultaneously, while the reverse isolation and gain are kept unchanged.

In order to design a balanced power amplifier. As a first step, a single-stage power amplifier is designed and then transformed it into a balanced amplifier configuration by incorporating the hybrid couplers.

2.1 Design of the single-stage power amplifier

The important step that should take into consideration in designing a power amplifier is the choice of an appropriate active device (transistor). The choice of an active device for a microwave power amplifier is very complicated. It implicates choosing an active device having an acceptable current rating with output power and power gain capability that meets the requirements of the intended application. It is also important that the chosen active device has a breakdown voltages which will not be exceeded by the RF and DC voltages that appear through the various junctions of the transistor and that permit the gain at frequency objectives to be met by the active device.

According to the design target, we select ATF-21170 transistor [12]. ATF-21170 is a low noise enhancement-mode GaAs FET designed to be employed for low cost commercial applications in the 500MHz to 6GHz frequency range [12]. It has high linearity, low noise and high gain performance and so on, therefore, that it can satisfy our request perfectly.

The bias circuit design is very important during an amplifier design process, The aim of the bias circuit is to set the quiescent point that is the I_{ds} and V_{gs} for an active device that causes it to work in the preferred region. From a general perspective, there are different kinds of biasing networks although in power amplifier applications. Low complexity is required. One commonly and probably used method is to utilize a radial stub immediately after $\lambda/4$ high impedance bias line that will facilitate to realize proper isolation at desired RF/microwave frequency, whatever the component to use after $\lambda/4$ long bias line [13].

A stable and strong bias circuit to supply an appropriate quiescent operating point is important since the bias circuit will also affect the output power, gain, stability and so on. A class-A biasing point was chosen to obtain a good performance in power gain with good matching impedances and high output power. Depending on the datasheet [12]. We select the typical quiescent operating point, $V_{ds} = 4$ V, $V_{gs} = 0.5$ V, $I_{ds} = 60$ mA.

The power amplifier may fail if the design circuit is unstable because of oscillation. There are two natures of stability namely conditional stability and unconditional stability. Conditional stability in PA presents when the stability factor (k) less than 1 and this condition rely on the source and the load termination. It can keep the system stable for a certain range of source and load impedances [14]. To contrariwise, the unconditional stability in PA happens when stability factor more than 1, ensures the circuit to be stable for all source/load impedances. For the proper running of the power amplifier, the unconditional stability must be ensured. For this, we add a taper line to the source of the transistor [15] as shown in **Figure 2**.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} \cdot S_{22} - S_{12} S_{21}|^2}{2 |S_{12} S_{21}|} \quad (5)$$

Where k is the stability factor [14].

In the design of power amplifier, the matching network makes the input/output impedance transform to 50Ω impedance in the condition of good power gain and low return loss. The schematic of the proposed single-stage power amplifier is shown **Figure 2**; it comprises a stability network, bias network, the input and output matching networks, For machining, a “T” type matching is used at the input and the output sides of the transistor.

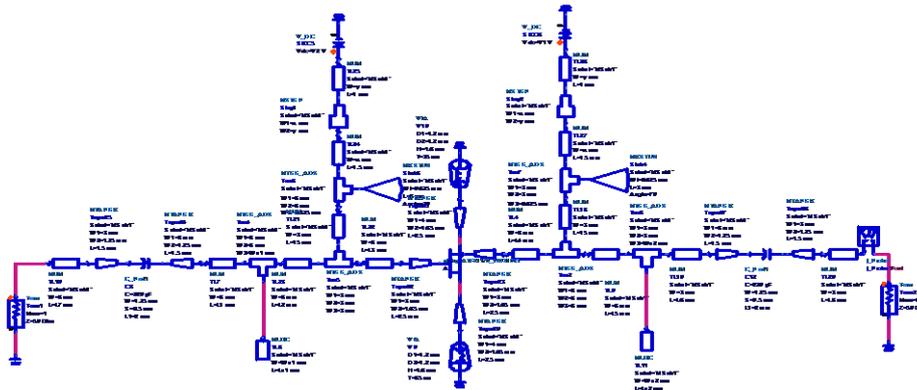


Fig. 2. The schematic of the proposed single-stage power amplifier

The simulation results of the proposed single-stage amplifier circuit are illustrated in **Figures 3–5**. **Figure 3** presents the simulated S-parameters of the performance of the proposed single-stage power amplifier. the power gain (S_{21}) of this power amplifier is about 19dB with an isolation coefficient (S_{12}) lower than -24dB at 2.45GHz, and the reflection coefficients are less than -10dB over the interested band; it can be observed that the input reflection coefficient (S_{11}) is less than -38dB and the output reflection coefficient (S_{22}) is less than -33.5dB at 2.45GHz. Whereas the circuit achieves a maximum saturated output power of 14dBm as shown in **Figure 4**. As depicted in **Figure 5**, it can be seen that $k > 1$ over operating frequency band. Consequently, the condition for unconditional stability of the proposed single-stage power amplifier is confirmed on the interested band, which means there is no risk of oscillations. Despite this performance but the single-stage amplifier it has a narrow band.

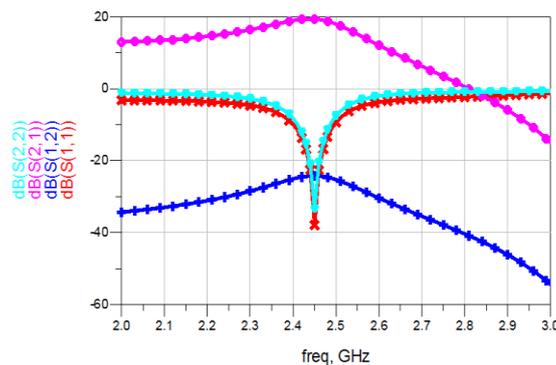


Fig. 3. S-parameters versus frequency of the proposed single-stage amplifier.

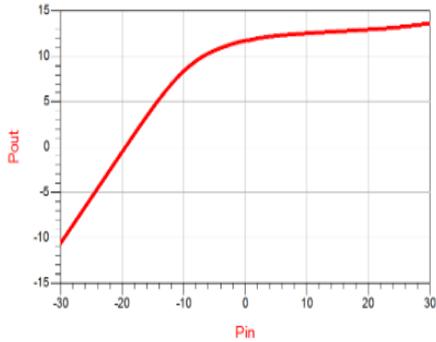


Fig. 4. Input power versus output power for 2.45GHz.

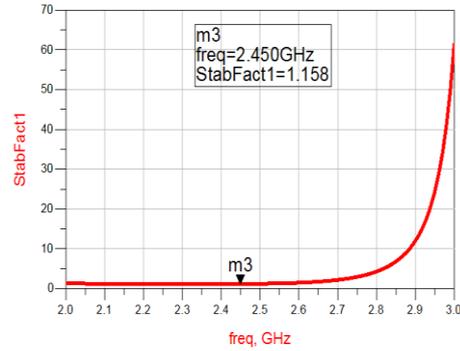


Fig. 5. Stability factor versus frequency characteristics.

2.2 Design of the balanced power amplifier configuration

After we have finished designing the structure of the single-stage PA we move on to the next step, which is the design of the hybrid coupler.

Due to the branch-line coupler has low-performance and large-coupler is difficult to implement, the Wilkinson power divider has been utilized in this work. The Wilkinson power divider is a type of classical one with a straightforward structure and easy to implement. The circuit has been designed on Epoxy substrate ($\epsilon_r = 4.4$, $\tan\delta = 0.025$) with 1.6 mm thickness. The selection of the substrate should consider its permittivity and its thickness. These characteristics impact on bandwidth. Epoxy (FR4) combines good electrical features, availability and price. In order to verify the accuracy of the design, the simulation has been carried out on an Agilent ADS. The characteristic impedance is 50Ω and the center frequency is 2.45GHz, then the length and width of the microstrip can be determined using LineCalc tool. The schematic circuit of the Wilkinson divider and simulation results are illustrated in **Figure 6** and **Figure 7**, respectively. The results indicate that the isolation (S_{32}) between port 2 and port 3 is lower than -27dB. The transportation gain (S_{21}) is -4.8dB, the reflection coefficient (S_{11}) of each port is also less than -38dB.

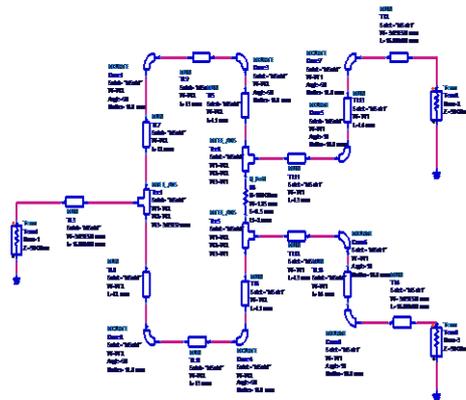


Fig. 6. The schematic circuit diagram of the Wilkinson power divider

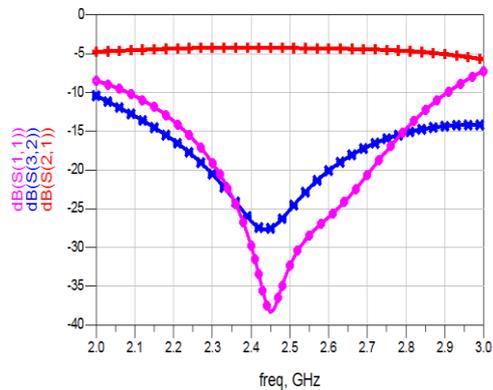


Fig. 7. The simulated results of the Wilkinson power divider

Finally, we mix two parallel single-stage amplifiers and two power dividers. The printed circuit of the balanced power amplifier was implemented in microstrip technology using the Epoxy substrate (FR4) with a relative permittivity of 4.4, a thickness of 1.6mm, a metallization thickness $t=0.035\text{mm}$ and a tangential loss of 0.025. For more realizable results, Momentum tool is performed. Layout architecture utilized to show the location of the components and the real circuit size. The layout of the final proposed balanced power amplifier structure is presented in **Figure 8**, where the overall size of this balanced PA is 260 mm (L) * 93 mm (W). The simulation results of the balanced power amplifier circuit are illustrated in **Figures 9–11**.

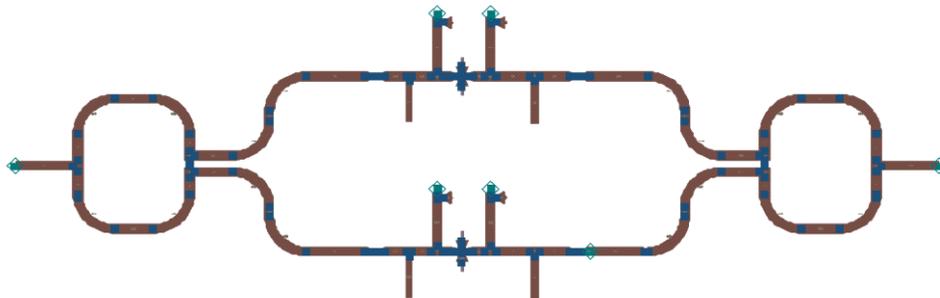


Fig. 8. The complete structure of the balanced amplifier

The S-parameter of the proposed balanced power amplifier is presented in **Figure 9**. For this structure, the power gain is more than 16dB in the required frequency range of 2.40–2.50GHz with an isolation coefficient (S_{12}) is less than -28dB in the operating frequency band. Note that the power gain is dropped by 3dB at the peak-gain frequency for the balanced PA due to the additional loss of the Wilkinson power divider. Whereas the input and output reflection coefficient (S_{11} and S_{22}) of this amplifier are less than -15dB with the input reflection coefficient S_{11} is between -26dB and -38dB, while the output reflection coefficient S_{22} ranges between -15dB and -19dB. It is clear from the result that the proposed balanced amplifier provides good matching impedances.

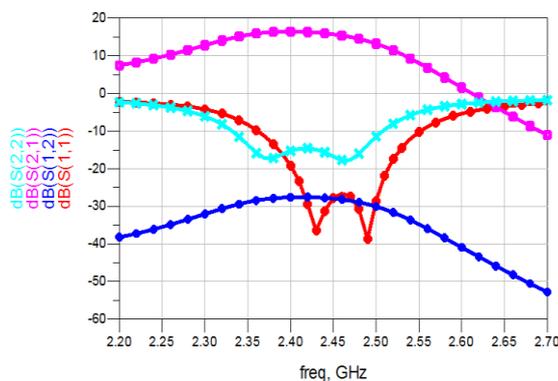


Fig. 9. S-parameters versus frequency of the proposed balanced amplifier.

Thereby this balanced amplifier has a bandwidth equal to 100MHz from 2.40GHz to 2.50GHz. From **Figures 10** and **11**, we can see that the max value of the output power rise up to 16dBm and the stability factor of the amplifier is bigger than 2.1 that signifies the circuit is unconditionally stable.

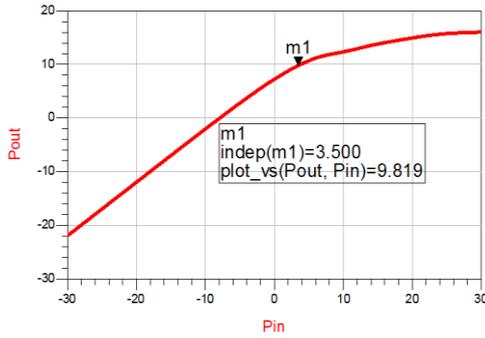


Fig. 10. Input power versus output power for 2.45GHz.

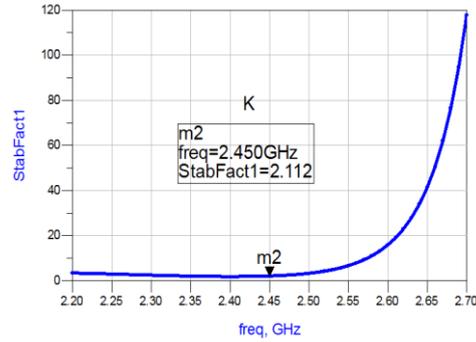


Fig. 11. Stability factor versus frequency characteristics.

After the completed the design of the balanced amplifier, a performance comparison between the proposed amplifier and other designed amplifiers in literature in terms of power gain, reflection coefficients and supply voltage are introduced in **Table 1**. As mentioned in **Table 1**, we can clearly observe that the proposed amplifier achieves a better performance compared to the cited works.

Table 1. Comparison between the proposed amplifier with published literature.

Ref	Technology	Frequency (GHz)	Supply Voltage (V)	Power Gain (dB)	Output Power (dBm)	Input Return Loss (dB)	Output Return Loss (dB)
[16]	GaAs FET	1.10-3.00	3	12	14.8	-25	-17
[17]	CMOS	1.65-2.00	10	10	18.5	-21	-8
[18]	Si BJT	1.75 - 2.15	12	11 ± 0.5	8@1dB	-22	-18
This Work	GaAs FET	2.40-2.50	4	16	16	-38	-19

3 Conclusion

In this study, we have developed a new balanced power amplifier by using a Wilkinson power divider. This balanced amplifier was designed using the microwave simulation Advanced Design System (ADS) software. The proposed amplifier was designed by a microstrip technology and packaged GaAs FET ATF-21170. The final circuit has achieved a wide bandwidth of 100 MHz, with The S_{11} and S_{22} are all less than -15dB, output power up to 16dBm, and 16dB power gain. Furthermore, the proposed balanced amplifier can keep more than 1dB

gain flatness at the whole operation band which shows much better performance than the conventional narrowband amplifier (single-stage amplifier).

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