A Novel Zero Bias Microstrip MESFET Power Limiter

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Abstract. In this article, a novel limiters power is designed and validated by ADS software. The new limiter is based on a mictrostrip circuit and uses MSFET transistors and Schottky diode as actives components. This Power Limiter have been optimized in two steeps: the first circuit is composed of one stage. Simulation of this circuit presents some limitation in termes of limitation rate. To improve this performance, a new circuit composed of two stages is simulated and optimized. The final circuit exhibits 25 dB of limitation rate while insertion loss is -1 dB with a threshold input power level of 0 dBm until a maximum input power level of 30 dBm.

Keywords: Microstrip, Power limiter, MESFET transistor, Schottky Diode.

1 Introduction

Currently, various types of semiconductor diode power limiters are used to improve the reliability and protection of communication and radar systems implementing high power microwave sensitive electronic components [1]–[4].

Generally, Power Limiter designs incorporate a planar-mounted PIN diodes network or Schottky diodes [5]–[8]. Figure 1 presents the classical topologies found in several scientific literatures on circuit protectors [5]–[7], [9]–[11]. These limiters can be optimized for operating frequency ranges and power levels.

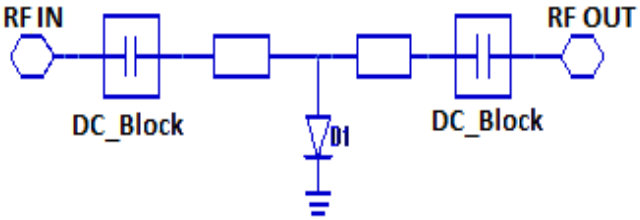

Fig. 1. Classic Power Limiter Topology

In this article, a new limiter power is designed and validated using a transistor and two Schottky diodes. The transistor operates as variable impedance that absorbs the extra power over the threshold supported by the load. While the Schottky diode functions as a signal detector and generates the DC electric current needed to bias the transistor and reducing the power threshold limit to activate the protective mode of the power limiter.

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Depending on the mode of supply of the power limiters, there are two types: the active power limiters that require an external current to operate and the passive power limiters that are zero biais. In this article, the proposed design is a new passive power limiter that does not require DC current.

In the next section, the theory approach and the description of the proposed circuit will be exposed, in the validation section, the s-parameters and Harmonic simulation results will be exposed and discussed.A comparison between the proposed circuit and other circuits in literature will be presented and commented at end.

2 Research Method

2.1 MESFET transistor operation

The structure of the Schottky contact field effect transistor is based on an active layer (channel) directly implanted in the semi-insulating substrate [12]–[14]. Figure 2 shows the cross section of a MESFET transistor. This device is composed of an insulating layer of GaAs above which, a layer of N-doped semiconductors above, a metal port called gate is connected directly to this layer. The source and drain ports are two negatively doped semiconductor layers. The source and drain contacts have ohmic contacts in contrast to the Schottky gate contact. The length of the metal gate is typically 0.5 to 1.0 µm for discrete transistors but it may be 0.2 µm for integrated circuits [10].

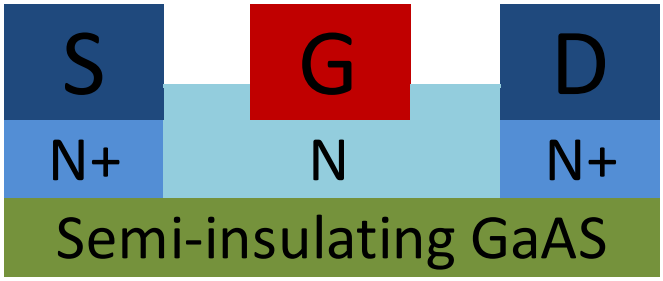

Fig. 2. Structure of MESFET transistor

In addition to their use as active elements in amplifiers, MESFET Transistors are used as active devices in variable attenuators, switches and phase shifters [10], [12], [15], [16]. The use of MESFET transistors in solid state passive power limiters is another application of this device [1], [6], [17], [18].

For most control applications, the MESFET is switched between a low impedance state, or a high impedance state, or pinchoff state corresponding respectively to the linear, no-linear and cutoff regions of this component. This switching is achieved by applying a negative voltage on its Gate port.

Russell Gaspari and Harold Yee [19] report four reasons to prefer FET technology over PIN diode in microwave control circuit:

1. The FET biasing is isolated from RF line and needs minimal RF Choke
2. Possibility to achieve insertion gain rather than insertion loss

3. Switching from On to Off consume very low energy
4. The switching speed is better in the FET than the PIN diodes

The basis of operation of a MESFET is the ability to modulate the thickness of the channel via the gate [12]. A depopulated layer of free electrons, called the space charge zone (SCZ), is created under the gate. No current can cross this layer. The region where the current can flow is therefore reduced to the fraction of the active layer that is not depopulated. In normal operating mode the drain is positively polarized with respect to the source, while the gate is always biased negatively, with respect to the source.

The operation of a MESFET is summarized by the following steps [12], [14]:

At a fixed drain voltage, the negative bias of the gate has the effect of increasing the penetration of the space charge zone (SCZ) in the active layer, thereby decreasing the flow of current. When the gate voltage is sufficiently negative, the SCZ completely close the channel, no longer allowing the current to flow. The transistor is then said "pinched off" and the voltage applied to the gate is then called clamping voltage or pinchoff voltage Vp.

In high power, Schottky diode will generate a DC rectified current. The orientation of the schottky diode relative to the gate port of the MESFET transistor, will allow in one direction to bias the gate by a negative voltage.

2.2 Use of MESFET transistor as limiter devices

The realization of MESFET-based power limiters can be achieved in several ways [7]: The first way is presented in Fig. 3. The MESFET transistor is connected parallel to load with an amplitude detector such as a schottky diode [7]. The rectified DC voltage is generated when the amplitude of incident signal is detected. This voltage is applied to the MESFET gate and its impedance is modified. As a result, the output RF amplitude is decreased.

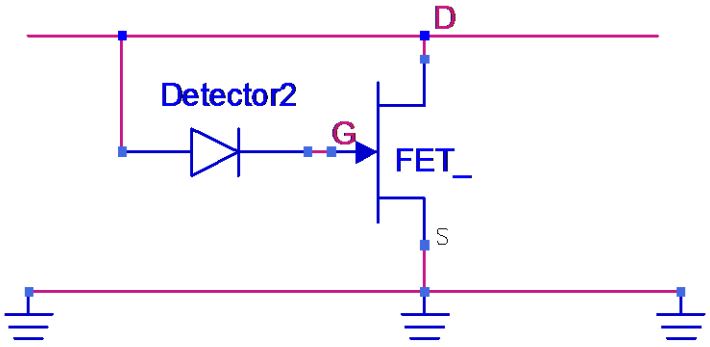

Fig. 3. Use of MESFET parallel to the load

The second way is to connect the MESFET transistor in series [18] with the transmission line as shown in Fig. 4. When the incident power is small, the MESFET has low impedance and therefore the insertion loss of the limiter is negligible. Increasing the power of the input signal provides the voltage of the Schottky barrier junction created by the gate of a MESFET. When this voltage exceeds the static threshold of the Schottky barrier junction, the direct current begins to flow. This provides the negative gate bias voltage across the gate ballast resistor.

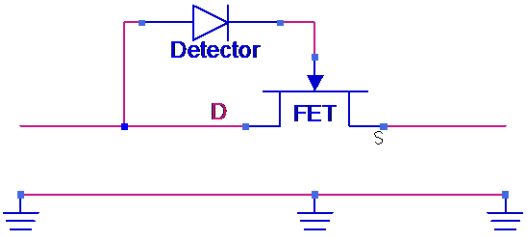

Fig. 4. Use of MESFET in series

In this proposed work, The MESFET Transistors is used in a new way as depicted in Figure 5. The MESFET is implanted as variable resistance R_{GS} and R_{GD} controlled by the voltage applied in the Gate port.

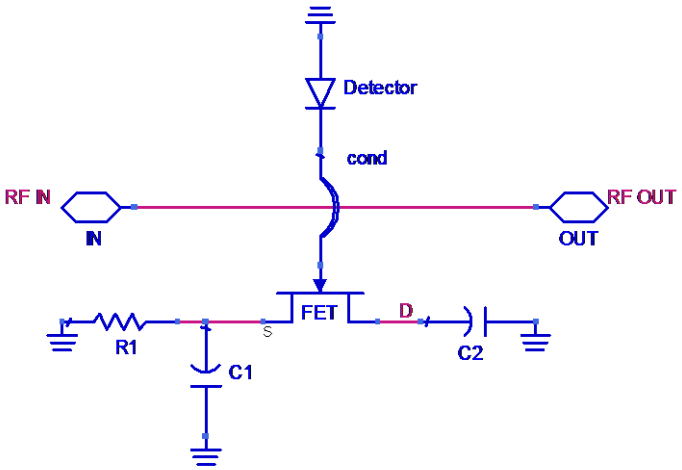

Fig. 5. Use of MESFET as variable resistance

3. Design Description

The proposed limiter is a passive power limiter based on microstrip line. One of them is a linear line that transmits the main signal to the load and the second line is derivated and connected at its end to Schottky diode and MESFET Transistor. The second line is used to divert a portion of incident signal when the amplitude of the signal reaches the threshold of the diodes. The Schottky diode operates as voltage controlled attenuator and current detector. Figure6 presents the proposed architecture. Commercial devices are used in this circuit:

- Schottky diode HSMS286B made by Avago technologies [20]
- MESFET ATF21170 made also by Avago technologies [21]

The commercial diode Avago HSMS286B has used in this circuit is a Surface Mount RF Schottky diode presented in SOT23/143 package[20] and suitable for incident power above -20 dBm. The HSMS286x family has been designed for RF applications [17], such as:

- DC biased small signal detectors to 1.5 GHz.
- Biased or unbiased large signal detectors (AGC or power monitors) to 4 GHz.
- Mixers and frequency multipliers to 6 GHz

The equivalent impedance of this Schottky diode, as depicted in Figure7, is modeled as a combination of the variable junction resistance (Rj), the parasitic capacitance and parasitic series resistance (Rs).

The ATF-21170 is a high performance MESFET GaAS transistor designed for use in low noise or medium power amplifier applications in the frequency range 0.5-6 GHz [21].

This GaAs FET device is housed in an hermetic package with a gold-based metalization. This device has a nominal gate length of 0.3 micron with a total gate periphery of 750 microns. AT21170 can dissipate a power of 27dBm at 25°C and its channel temperature can reach 175°C [21].

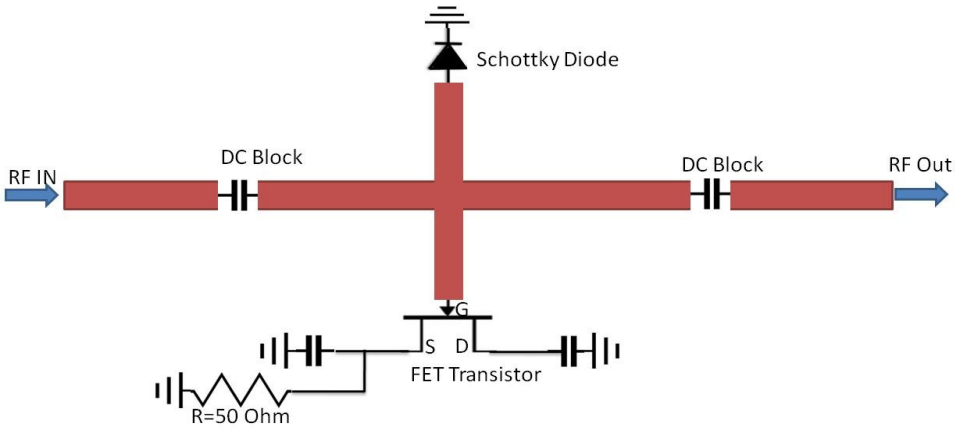

Fig. 6. Power Limiter circuit

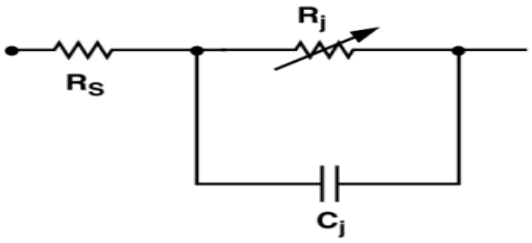

Fig. 7. Linear Equivalent Circuit Model of Schottky Diode

The designed circuit has been optimized in two steps by improving in each step the limiting rate while maintaining the insertion loss as minimum as possible.

The first circuit consists of a single stage identical to Figure 3: a stage is composed of an anti-parallel line to the main line with MESFET transistors and a Schottky diode at its ends.

In order to improve the limiting rate of the power limiter, the final circuit is obtained by joining in series two circuits. This final circuit has been optimized to keep the insertion loss as low as possible while doubling the limit rate.

4. Circuit validation by simulation and discussion

The designed circuit was validated in simulation by ADS software to check s-parameters response and harmonic simulation response of the circuit. For the simulation we use a standard FR4 substrate with a relative dielectric constant value of 4.4 and a dielectric Loss tangent value of 0.025 and a thickness of 1.6 mm. The choice of FR4 as substrate is dictated by its availability in the laboratory and its cheap cost.
As the circuit has been optimized in two steps, the first ciruit is constituted of one stage. The second circuit is formed by two stages. For each steps, the layaout schematic, the s-parameters results and harmonic simulation results will be presented and discussed.

4.1 One stage circuit

The layout of the first circuit studied is presented in Figure 8.

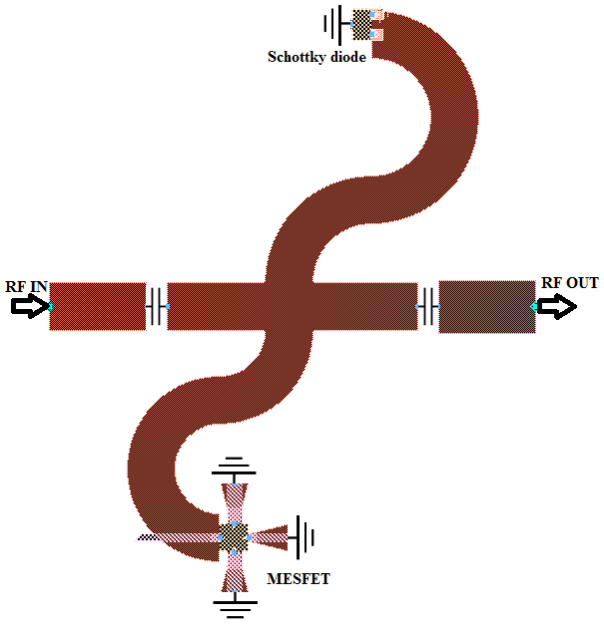

Fig. 8. Layout of one stage circuit

Figure 9 presents the s-parameters simulation results. As shown in the figure 9, the circuit presents good matching input impedance in the ISM band. The insertion loss is around -0.9dB over [3, 3.6 Ghz].

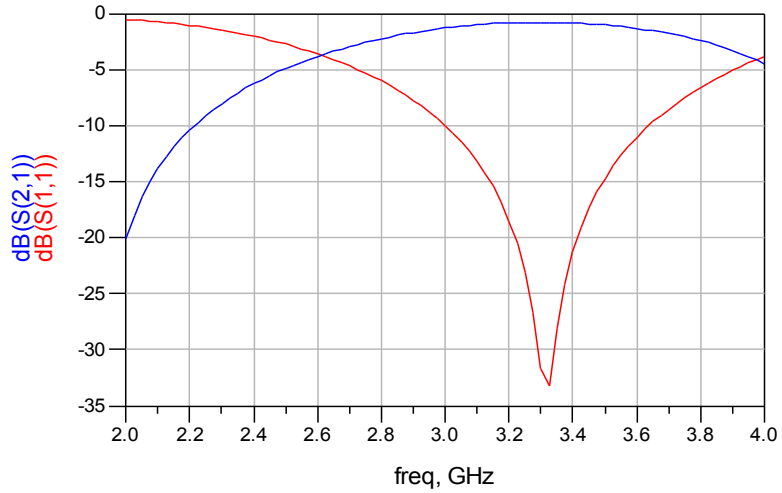

Fig. 9. S-parameters simulation results for S11 and S21

Figure 10 shows the output power versus input power. This circuit presents a low isolation at large signal (12 dB at Pin=30 dBm). These Values of protection will not be considered sufficient in many applications. In order to improve the performances of this circuit, we have simulated a second circuit with two stages. The layout of the second optimized circuit is presented in Figure 11:

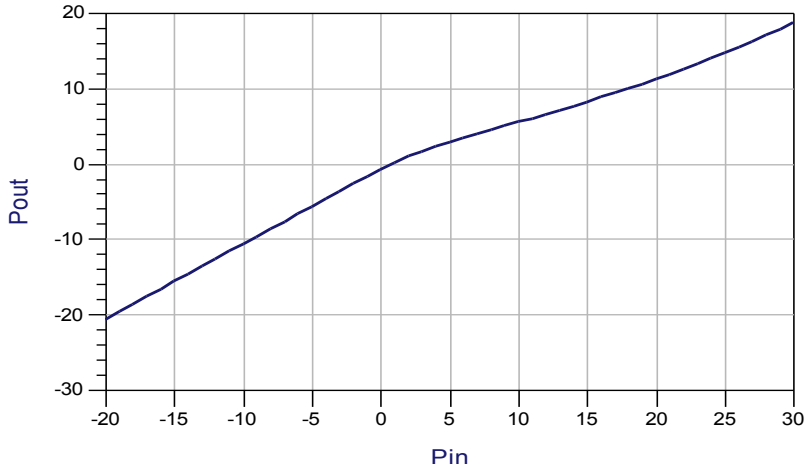

Fig. 10. Output Power versus input power

4.2 Circuit with two stages

The second circuit is obtained by adding a second stage. However, in order to reduce circuit dimension, the antidopal line is replaced by a half circle line. The final circuit is presented in the Figure 11:

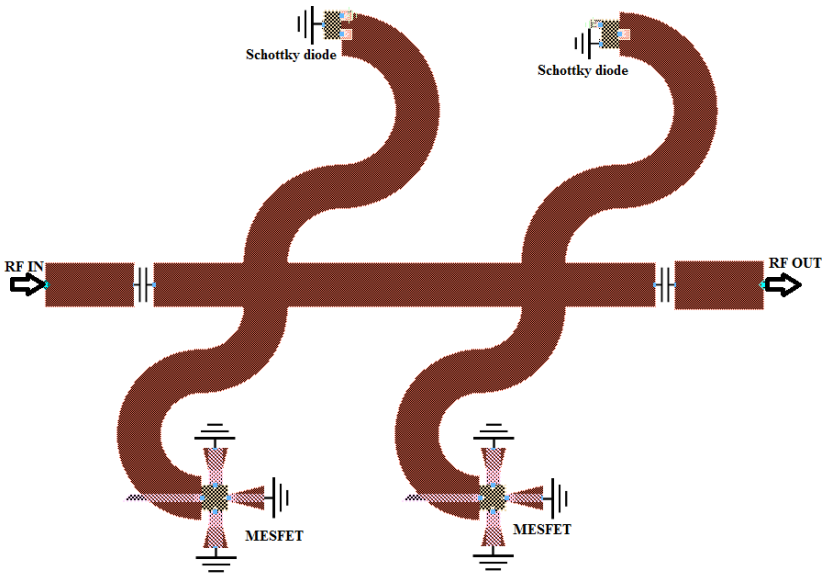

Fig. 11. Layout of two stages circuit

The simulation results of this circuit are presented in Figure 12 (S-parameters results) and in Figure 13 (Output Power Versus Input Power).

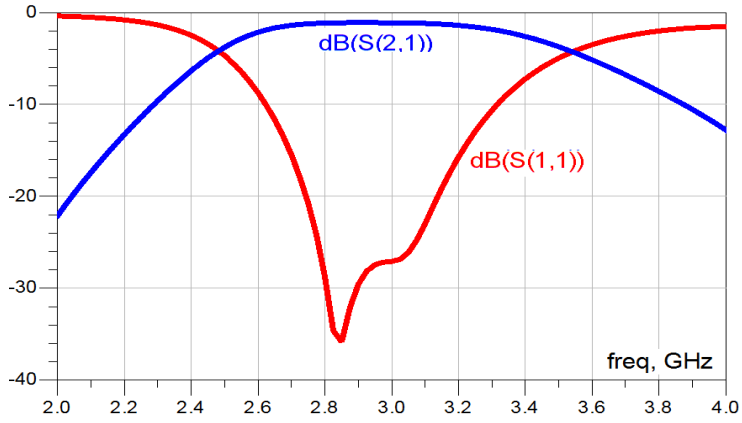

Fig. 12. S-parameters simulation for S11 and S21

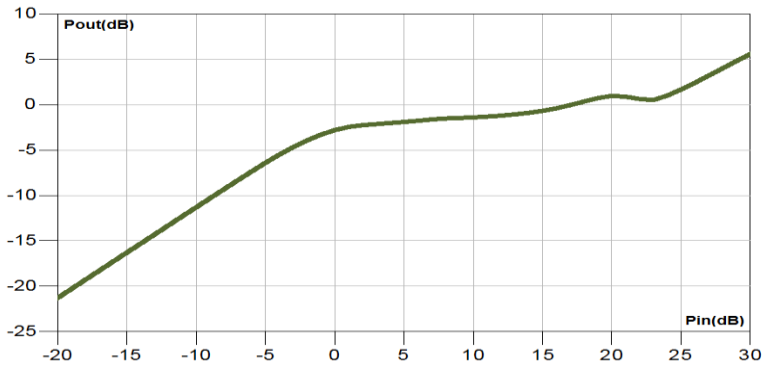

Fig. 13. Output power versus input power

Compared to one stage circuit, the two stages circuit shows better performance in isolation rate:

- Broadband frequency range of 1Ghz from 2,6 to 3,4Ghz
- Low insertion loss (-1 dB)
- The isolation rate reaches 25 dB at 2.7 Ghz.

Also the circuit presents a good stability of limitation rate across the broadband range.

5. Comparaison between the designed circuit and similar circuit in letterature

By comparing the proposed circuit against power limiter topologies constructed on a microstrip line published in the literature, the designed circuit presents an efficient and simple solution for a passive power limiter based on MESFET transistors and Schottky diodes. The table below relates different technical characteristics of the proposed limiter with those of the scientific literature.

Table 1. Comparison of microwave power limiter.

Design	Insertion loss (S21)	Frequency range	Limiting rate	References
Microstrip Passive limiters using discrete MESFET and Schottky diodes	1 dB	3 Ghz	25 dB	The proposed limiter
Planar Schottky diode	1 dB	1 Ghz	20 dB	[6]
Planar Schottky diode and MESFET based limiter	1 dB	1 Ghz	15 dB	[6]
Pin diode limiter (3 stages)	1.3 dB	Ku band	29.7 dB	[11]
Passive limiters using Discrete MESFET and Schottky diode	0.9 dB	7 Ghz	15 dB	[18]

In addition, the designed circuit shows important advantages in comparison to the state of art presented in literature:

- The circuit presents simple construction by avoiding the need of external DC current.
- The use of zero bias diodes reduces Johnson noise caused by DC current and improves reliability of the circuit.
- MESFET transistors present faster switching and RF power detections thus enhance circuit response to high power pulses.

6. Conclusion

In this paper, we have designed and validated by simulation a power limiter circuit based on zero bias MESFET transistors and Schootky diodes.
The first circuit based on one limiter stage achieves 12dB of isolation. The final optimized circuit achieves 25 dB of isolation while the insertion loss at low signal remains acceptable (around -1 dB). The circuit dimensions for the proposed frequency are: 48x38 mm². In comparaison to other power limiters in literatures, the proposed circuit presents the best performance in terms of limitation rate.

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