Tunnelling FETs, the Non-conventional Transistors: Basics

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Abstract. The tunnel field-effect transistor (TFET) exploits the band to band tunneling (BTBT) phenomenon for carrier injection and this helps to lower the subthreshold swing <60mV/decade due to the absence of thermal (kT/q) dependence. Tunnel Field Effect Transistor has been evolved by T. Baba in 1992, and provides an alternative to conventional switch based on various performance parameters. TFETs show tremendous potential from the low-power applications point of view. However, the challenge to gain a high I_{on}/I_{off} ratio in combination with subthreshold swing <60mV/decade still persists for devices to be used in high-performance circuits. To achieve this, it is required that many technologies to be used in combination for the realization of such hetero-structure TFET devices.

Keywords: Tunnel Field Effect Transistors, MOSFET, Non-conventional Transistors

1 Introduction

It is seen for the last two decades, that CMOS device technology has undergone a revolutionary change, and the process, as well as design capabilities, are explored and utilized up to the limits. The Integrated circuits are constantly resulting in higher performances and can embed more functionality per unit area due to the scaled power consumption of these CMOS-based circuits. The wide use of CMOS technology is possible only due to its scalability to smaller dimensions and it has helped in achieving higher performances along with a decrease in the power consumption due to voltage scaling. Today's processor performance enhancement has been driven by the scaling of the transistor (MOSFET) technology, which resulted in decreasing power consumption while gaining speed at the same time. This continued scaling of the transistor and huge rise in density has increased power density significantly on the chip. The reduction of supply voltages as V_{dd} is scaled has quadratically reduced the power consumption in a dynamic state, but it has highly impacted the application with static power constraints posed by high-speed computing chips requirement of being energy efficient.

As we see that to get a similar drive current for maintaining the drive strength, the Vth (Threshold voltage) is to be scaled in proportion with the V_{dd} reduction of a transistor, which causes the off-state leakage to rise exponentially leading to high static leakage and thus the static power. The basics of Tunnel Field Effect Transistors (TFETs) state it as test transistor which uses quantum tunnelling modulation as a mode of the current generation, unlike the standard MOSFETs that use thermionic emission, thus giving the lower value of subthreshold

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swing [1]. Therefore, it is a promising candidate for designing analog or mixed-signal integrated circuits specially designed for ultra-low power consumption and stability over a wide range of temperatures for longer life [2-4]. We will discuss the basic TFET device structure, understand the functionality qualitatively.

The tunnel field-effect transistor (TFET) exploits the band to band tunnelling (BTBT) phenomenon for carrier injection and this helps to lower the subthreshold swing <60mV/decade due to the absence of thermal (kT/q) dependence[5, 6]. Tunnel Field Effect Transistor has been evolved by T. Baba in 1992, and provides an alternative to conventional switch based on various performance parameters as mentioned below:

- Potential for exceeding the subthreshold swing limit of 60mV/decade.
- Ultra-low-voltage and ultra-low power.
- Higher I_{ON}/I_{OFF} current ratio.
- Immune to Short channel effects.
- Highly reduced leakage currents.
- Overcoming the speed limitations as a tunnelling mechanism is utilized.
- The device operation range for sub-threshold and super threshold regions is available.

These devices can also be utilized as a biosensor as alternate methods are being explored in biomolecules detection for comparison and analysis of sensitivity to various devices [7, 8]. These devices due to their high detection ability will help in improving the quality of medical tests and methods that can be utilized for mass usage. Moreover, the demand for low power devices in the medical field is encouraging bio-medical devices to be designed using new technologies that can reduce the burden of cumbersome equipment with smart digital devices replacing them.

2 Basics of TFET

2.1 TFET basic definition and its working

The tunnel field-effect transistor (TFET) is still treated as an unconventional type of transistor. Figure 1 shows the tunnel FET structure on SOI. It can be described as a gated p-i-n+ diode, with the gate residing on an undoped or intrinsic region, which forms the channel. p+ region is named as the source and n+region is the drain [9, 10]. A look at the structure gives the impression of its similarity to the conventional MOSFET structure, but there exists a fundamental difference in the switching mechanism. Both these things make this device a prime candidate in low-power circuits. The tunnelling FET, as lies in the name itself, modulates the quantum tunnelling through the barrier rather than the thermionic emission over the barrier for the conventional transistor [11]. This phenomenon will be further discussed in the following sections.

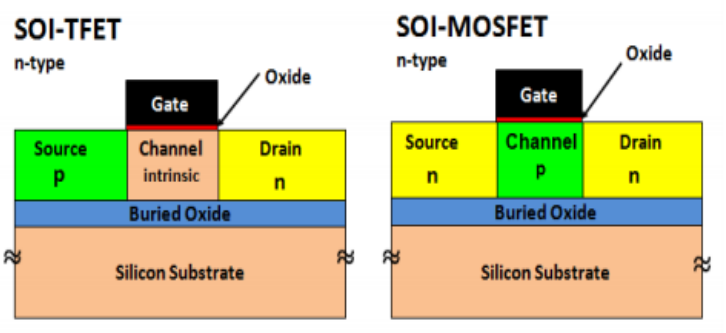

Fig. 1. Basic structure of a TFET and MOSFET

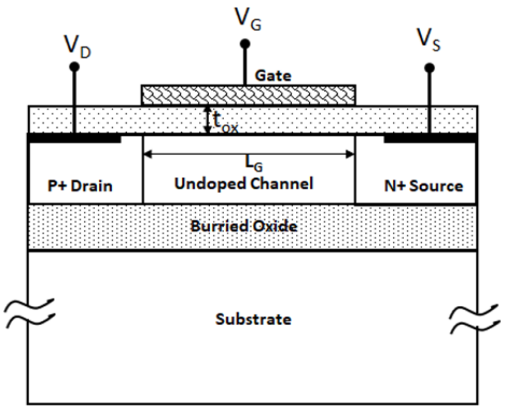

Fig. 2. Schematic diagram of single gate n-type TFET on SOI substrate

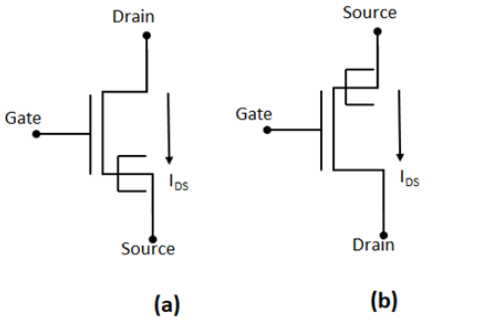

Fig. 3. Circuit symbol of TFET (a) n-type and (b) p-type

There are several modifications to this structure to improve the on-state current value e.g., double gate TFET (DG-TFET) which has two gates, one at the top and the other at the bottom of the substrate [12-14]. In the schematic representation of TFET, the source terminal is

identified by putting a bracket-like symbol in the MOSFET symbol structure as shown in Figure 2 and 3.

3 Simulation and device modelling methodology

Simulations are done using Silvaco's TCAD ATLAS software for three devices, which are, SOI-TFET, double gate TFET, and SOI-MOSFET. Their characteristic curves are plotted and compared. Evaluation parameters for comparison of these devices are ION/IOFF, subthreshold swing and leakage current. The simulation employs non-local tunnelling model. Bandgap narrowing effect is included. The effect of concentration-dependent mobility and SRH models should also be included. Band diagram across a horizontal cutline at off-state is shown in the Figure 4. The valence band of the source and conduction band of the channel is not aligned initially. But as higher gate bias is applied, the simulated band diagrams start modifying the barrier thickness.

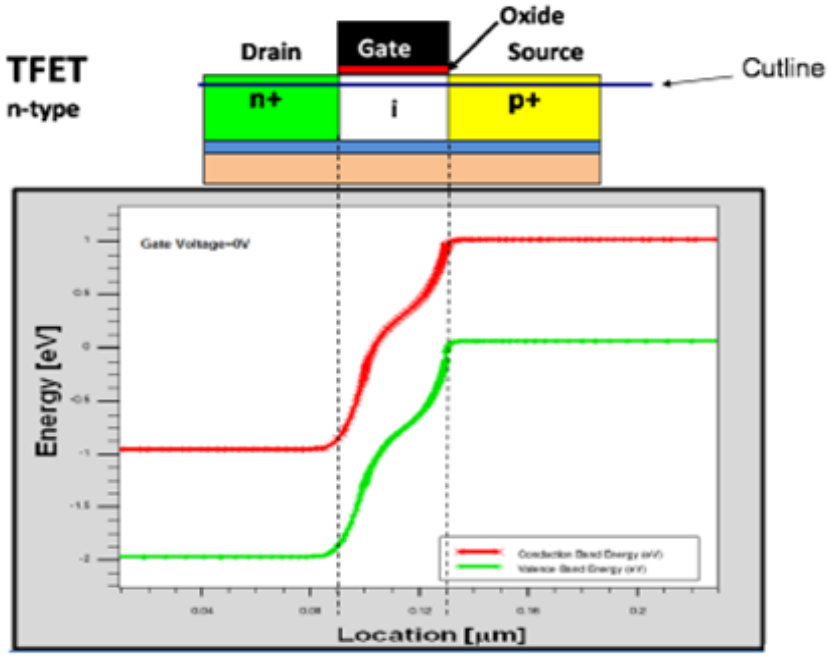

Fig. 4. Band diagram of off-state TFET across horizontal cutline

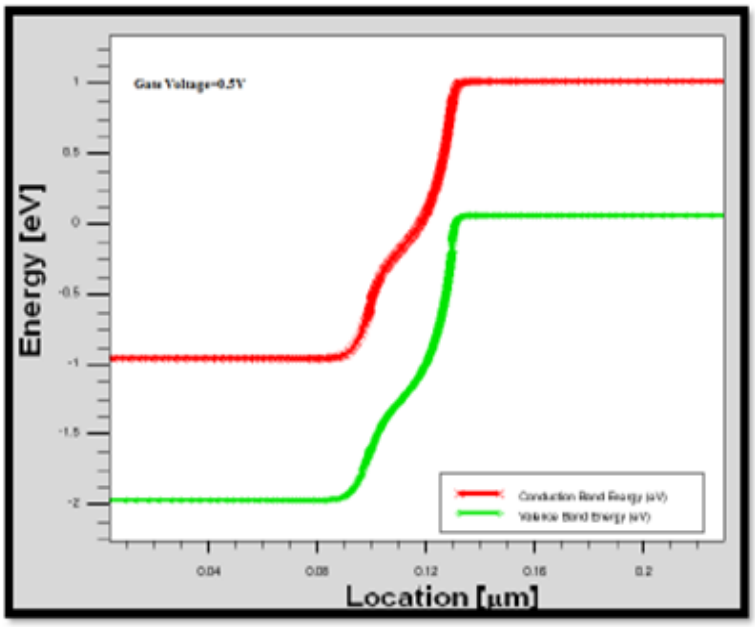

Fig. 5. Band diagram at gate bias=0.5V

The thinning of channelling width as more gate bias is applied can be observed in Figures 4 to 7. The pinning phenomenon is also evident in Figure 7. The simulated transfer characteristics are showing expected behaviour. The curves of different drain voltages, for negative gate bias sweep, don't overlap as the drain bias directly influences the tunnelling current (channel drain is the tunnelling junction), as discussed in the previous chapter. On the other hand, when the gate bias is swept positively, the drain bias has no direct effect on the tunnelling current (source-channel is the tunnelling junction), hence the curves almost overlap for most of the gate bias sweep. As discussed previously, the only effect of drain bias is when the pinning of bands begins. The heterojunction TFET such as GaSb/InAs TFET and many other materials chosen for TFET such as Germanium and Indium based compounds the pinning of bands begins. The heterojunction TFET such as GaSb/InAs TFET and many other materials chosen for TFET such as Germanium and Indium based compounds Ge, Ge Sn, In As and Ga Sn are difficult to model and is a limitation to find the optimum TFET material. The non-ideal ties arising due to trap sites or any defect resulting in non-abrupt band edges play a crucial role and need to be considered in simulations to match the experimental results with theoretical data. The non-ideal ties arising due to trap sites or any defect resulting in non-abrupt band edges play a crucial role and needs to be considered in simulations to match the experimental results with theoretical data

3.1 Impact of doping

The source and drain doping also play an important role in these devices. When the source side is doped highly, the depletion region at the source-channel junction will have less width thus shortening the distance travelled by the electrons tunnelling form the valance band edge of source to the channel as compared to the higher depletion width for the low source doping.

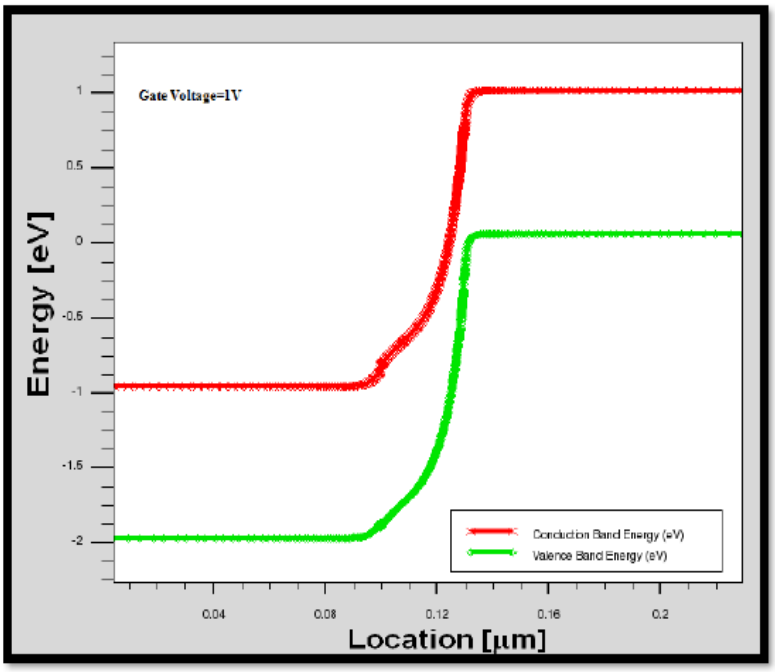

Fig. 6. Band diagram at gate bias

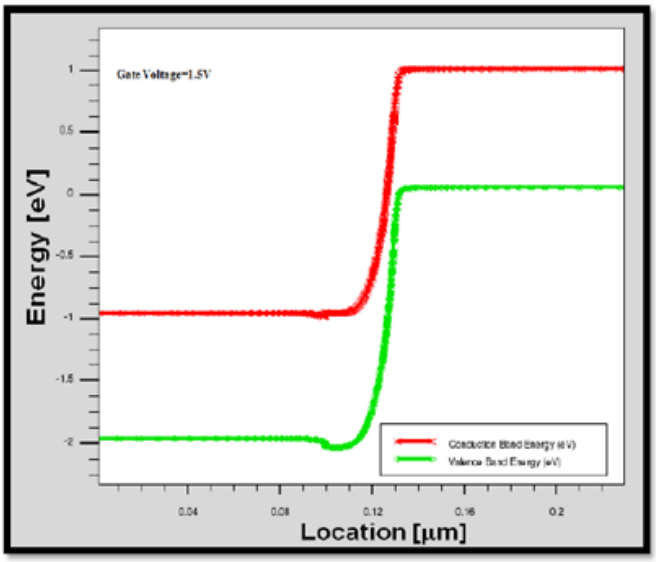

Fig. 7. Band diagram at gate bias=1.5V

Therefore, in case of higher doping of source, the higher tunnelling probability is expected across the source-channel junction, thereby increasing the ON current, resulting in higher drive strength.

3.2 Gate oxide effects

Gate Oxide The oxide capacitance is taken as Cox=εox/tox, where εox is the oxide permittivity and tox is the thickness of gate oxide. We can approximate the gate oxide effects using this simple formula, the gate oxide thickness reduction will increase the gate oxide capacitance. The higher the gate oxide capacitance, higher will be the charge in the channel region, and better gate control over the channel. The coupling efficiency of the gate to the channel can be increased by maintaining the thinner gate oxides in the device. But at the same time, the thin gate oxides are prone to carrier tunnelling from the channel to the gate, causing an increase in the gate leakages, which is highly unacceptable in devices. The end-use of the device also defines the leakage limits that can be compromised with gate control.

3.3 Channel length affecting device parameters

It is very well known that conventional MOSFET's drain current is largely dependent on the channel length, but interestingly the TFETs drain current shows little dependence to the length of the channel. The current conduction is largely through BTBT, the tunnelling current is governed mainly by the electric field at the source-channel junction and the alignment of the bands at the source side, as depicted in Figure 8. It must be noted that beyond the critical length of the channel, a decrease in the channel length is affected by the direct source to drain leakage.

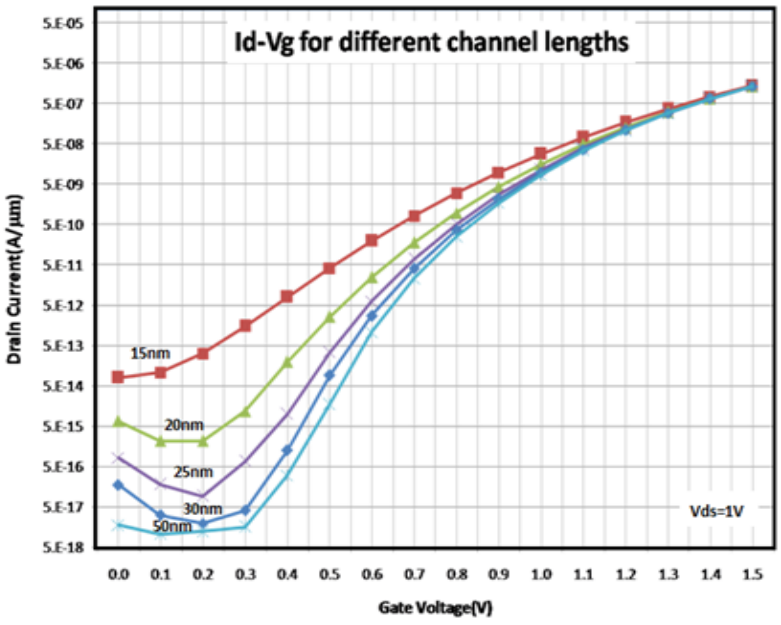

Fig. 8. Id-Vg plot for different channel lengths of TFET

4 Conclusion

TFETs show tremendous potential from the low-power applications point of view. However, the challenge to gain a high I_{on}/I_{off} ratio in combination with subthreshold swing <60mV/decade still persists for devices to be used in high-performance circuits. To achieve this, it is required that many technologies to be used in combination for the realization of such hetero-structure TFET devices. In lower technology node its fabrication becomes viable and can be a real, standalone device comparable to MOSFETs.

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