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All-Digital Background Calibration Technique for Offset, Gain and Timing Mismatches in Time-Interleaved ADCs

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Abstract

This paper presents a method for all-digital background calibration of multiple channel mismatches including offset, gain and timing mismatches in time-interleaved analog to digital converters (TIADCs). The averaging technique is used to remove the offset mismatch at each channel. The gain mismatch is calibrated by calculating the power ratio of the sub-ADC over the reference ADC. Timing skew is compensated by using Hadamard transform for error correction and least mean squares (LMS) algorithm for estimation of the clock skew. The performance improvement of TIADCs employing these techniques is demonstrated through numerical simulations.

Keywords: Time-interleaved analog-to-digital converter, channel mismatches, all-digital background calibration.

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1. Introduction

Time-interleaved analog-to-digital converter (TIADC) is a promising solution and increasingly used in systems that require high speed, high resolution, and low power consumption. It can be employed in the direct sampling receivers for software-defined radio systems, full-band capture cable TV tuner transmissions, broadband satellite receivers, sub-sampling receivers, etc. It increases the sampling rate by using the multiple channel analog-to-digital converter (ADC) that samples an analog input signal in the time-interleaving manner [1], [2]. However, the performance of TIADC is severely degraded by mismatches between sub-ADCs, including bandwidth, timing, offset, and gain mismatches [3], [4]. Therefore, correcting these mismatches is a very essential requirement.

There have been several works on channel mismatches calibration in TIADC [5]-[21]. In which, several works calibrate in either all-analog domain [5] or mix-signal domain [6], [7]. The all-analog calibration techniques can be performed with any input signal, but analog estimation is difficult to implement and is not suitable for CMOS technology. The mixed-signal calibration techniques require low power consumption and small chip area. However, its correction is inaccurate and requires an additional analog circuit. Therefore, it reduces the resolution of TIADC and increases the calibration time. Moreover, they are not portable between CMOS technology nodes.

Taking the advantages of scaled CMOS technologies, the all-digital calibration techniques overcome the above issue [8]-[21]. A general review of previously reported works based on the all-digital calibration techniques shows that those techniques focus on calibration gain and timing mismatches without addressing the offset one [8]-[17]. Authors in [18] proposed a technique to cancel offset, gain, and timing mismatches in TIADC. However, the main limitation of this technique is that there is an overlap between the basic function and desired signal when the input signal is single-tone spaced at $k\pi/M$. Instead of calibrating gain and timing mismatches by combining Hadamard transform and LMS algorithm in [19] or combining modulation matrix and LMS algorithm in [20], in this paper, we calibrate the gain mismatch by calculating the power ratio of the sub-ADC with the reference ADC. Firstly, the offset mismatch is calibrated

by taking the average of sub-ADC output samples. Finally, the timing error is calibrated by using the Hadamard transform and LMS algorithm as in [19]. In [19], [20], a calibration technique was proposed with preliminary results without detail analysis and state of-the-art comparison.

The proposed technique achieves higher performance and a faster convergence speed compared with the conventional techniques. The proposed technique significantly reduces the required hardware resources, specifically for the derivative and fractional delay filters for which no look-up table is required. In addition, the proposed technique requires only one FIR filters with fixed coefficients, thus reducing complexity and hardware resources, as compared to the bank adaptive filter techniques.

The rest of this paper is organized as follows. Section 2 introduces the TIADC model with offset, gain, and timing mismatches. In Section 3, we present the proposed all-digital background calibration technique for multiple channel mismatches. The simulation results are given in Section 4. Finally, conclusion is included in Section 5.

2. System model

Consider an M-channel TIADC which consists of offset, gain, and timing mismatches in Fig. 1. It is characterized by the offsets o_i, the gains g_i and the relative timing deviations t_i for $i = 0,1,...,M-1$. Without considering the quantization effects, the i^{th} channel's digital output can be expressed as

$$y_i[k] = g_i x((kM+i)T - t_i) + o_i. \tag{1}$$

By assuming a bandlimited input signal $x(t)$ so that $X(j\Omega) = 0$, with $|\Omega| \geq B$ and $B \leq \pi/T_s$, the output of the M-channel TIADC including offset, gain and timing mismatches is expressed as

$$\begin{aligned} Y\left(e^{j\omega}\right) = \frac{1}{T}\sum_{k=-\infty}^{+\infty}\left[\frac{1}{M}\sum_{i=0}^{M-1} g_i e^{-j\left(\omega - k\frac{\omega_s}{M}\right)t_i} . e^{jki\frac{2\pi}{M}}\right] \\ \times\left(j\left(\omega - k\frac{\omega_s}{M}\right)\right) \\ + \frac{1}{T}\sum_{k=-\infty}^{+\infty}\frac{1}{M}\sum_{i=0}^{M-1} o_i e^{jki\frac{2\pi}{M}}\delta\left(\omega - k\frac{\omega_s}{M}\right). \end{aligned} \tag{2}$$

This expression shows that, in the presence of all the errors, the input signal is modulated by the expression between brackets which combines gain and timing mismatch errors. These errors appear at each $\omega_{in} \pm k\omega_s/M$ frequency, where ω_{in} is the input frequency. Additionally, the offset mismatch tones intervene as signal independent spurious tones at each component $k\omega_s/M$.

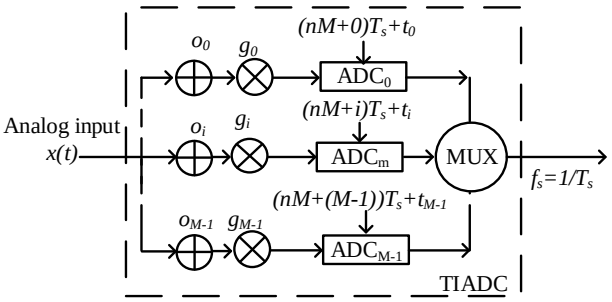

Figure 1. An M-channel TIADC with channel mismatches.

3. Proposed technique

3.1. Offset mismatch calibration

The offset calibration scheme illustrated in Fig. 2. Assume that $\hat{o}_i$ is the estimate of the offset o_i of the i^{th} channel ADC. To calibrate the offset mismatch, firstly, the offset $\hat{o}_i$ of each individual channel is estimated. Assume that the input signal is Wide-Sense-Stationary, expected value of the input is approximately zero, i.e. $\frac{1}{N}\sum_{k=0}^{N-1} g_i x\left(\left(kM+i\right)T_s - t_i\right) \approx 0$. Thus, the estimated offset values are expressed as

$$\begin{aligned} \hat{o}_i &= \frac{1}{N}\sum_{k=0}^{N-1} y_i[k] \\ &= \underbrace{\frac{1}{N}\sum_{k=0}^{N-1} g_i x((kM+i)T_s - t_i)}_{\approx 0} + o_i \approx o_i. \end{aligned} \tag{3}$$

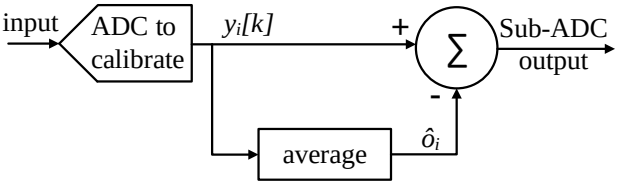

Figure 2. Offset mismatch calibration for each sub-ADC.

Firstly, the offset error can be calibrated by averaging the output of each sub-ADC over N samples as in (3) end then subtracting the average value from the ADC output as follows

$$\begin{aligned} \hat{y}_{\text{offset}}[k] &= g_i x((kM+i)T - t_i) + o_i - \hat{o}_i \\ &= g_i x((kM+i)T - t_i). \end{aligned} \tag{4}$$

3.2. Gain mismatch calibration

The signal after calibration of offset mismatch is expressed in (4). Assuming g_i denotes the gain mismatch of i^{th} sub-ADC. The goal of gain mismatch estimation is to determine the relative gain of each sub-ADC with respect to a reference ADC, i.e. g_i/g_0 . Let us assume that the first channel is the reference channel. By computing the average power of the i^{th} ADC and the reference sub-ADC, the relative gain can be estimated as

$$\frac{\frac{1}{N}\sum_{k=0}^{N-1} y_0^2[k]}{\frac{1}{N}\sum_{k=0}^{N-1} y_i^2[k]} = \frac{g_0^2 P_{x(t)}}{g_i^2 P_{x(t)}} = \frac{g_0^2}{g_i^2}. \tag{5}$$

This ratio is then taken the square root and multiplied by the i^{th} sub-ADC output to produce the corrected sub-ADC output. This output has the same gain mismatch of the reference sub-ADC as shown in Fig. 3. Therefore, the gain mismatch among sub-ADC channels is the same. Since gain calibration requires adders and multipliers running at the sampling rate of sub-ADCs, it is efficient for the hardware implementation in terms of power consumption and area.

3.3. Timing mismatch calibration

Timing mismatch calibration includes two steps of correction and estimation.

a) Timing mismatch correction

After the offset and gain mismatches are calibrated, the ADC output contains only the timing mismatch. Thus, the ADC output can be expressed as

$$y_i[k] = x((kM+i)T - t_i). \tag{6}$$

Assume that the sum of the timing mismatch in each channel is equal to zero $t_0 + t_1 + ... + t_{M-1} = 0$. The overall output spectrum of TIADC including only timing mismatch is expressed as:

$$Y\left(e^{j\omega}\right) = \frac{1}{T}\sum_{k=-\infty}^{+\infty}\left[\frac{1}{M}\sum_{i=0}^{M-1} e^{-j\left(\omega - k\frac{\omega_s}{M}\right)t_i}.e^{jki\frac{2\pi}{M}}\right] \times X\left(j\left(\omega - k\frac{\omega_s}{M}\right)\right). \tag{7}$$

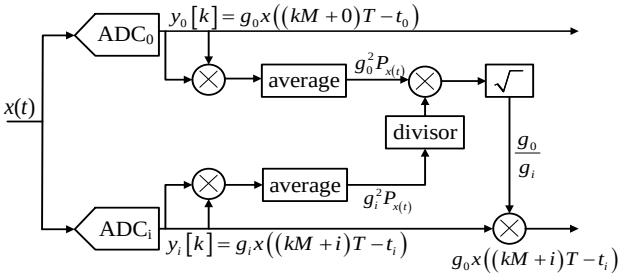

Figure 3. Gain mismatch calibration for each sub-ADC.

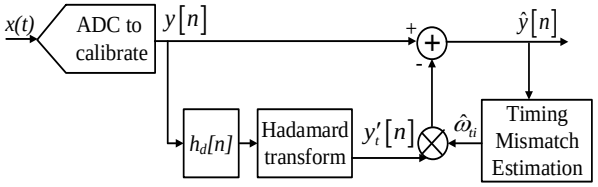

Figure 4. The calibration diagram for the timing mismatch in TIADC.

Without loss of generality, we consider the *M*-channel model without a quantization noise. $F_k(j\omega)$, $k = 0,1,...,M-1$ are channel responses, where $-\pi < \omega \le \pi$. Since $F_k(j\omega)$ have only the timing mismatch, these channel responses are expressed as

$$F_k(j\omega) = e^{j\omega(k+t_i)}. \tag{8}$$

To calibrate timing mismatch, we use Hadamard transform multiplied by the output signal of the ADC. This signal is called error signal which is used to remove the timing skew.

$$\mathbf{y}'_t[n] = y[n]\mathbf{H[n]} * h_d[n]. \tag{9}$$

where **H[n]** is Hadamard matrix with the order of *M*, $h_d[n]$ is the impulse response of the derivative filter.

$$h_d[n] = \begin{cases} \frac{\cos(n\pi)}{n} & (n \neq 0) \\ 0 & (n = 0) \end{cases}. \tag{10}$$

The calibrated signal is calculated by subtracting the error signal from the TIADC output.

$$\hat{y}[n] = y[n] - \omega_{ti}\mathbf{y}'_\mathbf{t}\mathbf{[n]}. \tag{11}$$

The filter coefficients are determined by multiplying the exact coefficients by Hanning window function. The coefficients ω_{ti} are calculated based on the sign of Hadamard matrix as follows

$$\begin{bmatrix} \omega_{t0} \\ \omega_{t1} \\ \vdots \\ \omega_{t(M-1)} \end{bmatrix} \approx \frac{1}{M}\mathbf{H}\begin{bmatrix} t_0 \\ t_1 \\ \vdots \\ t_{M-1} \end{bmatrix}, \quad (12)$$

where t_i , $i = 0,1,...,M-1$ is much less than 1 and $\omega_{t0} = 0$.

b) Timing mismatch estimation

In this section, we present the structure of the timing mismatch estimation block as shown in Fig. 5. The timing mismatch estimation block gives timing mismatch coefficients $\hat{\omega}_{ti}$ by using least mean squares (LMS) algorithm. These estimated values are used to create the estimated error signal $\hat{y}_t'[n]$. This signal is then subtracted from $y[n]$ to obtain the restored signal $\hat{y}[n]$ as

$$\hat{y}[n] = y[n] - \hat{y}_t'[n]. \quad (13)$$

where

$$\hat{y}_t'[n] = \hat{\boldsymbol{\omega}}_{\mathbf{ti}}\bar{\mathbf{y}}_{\mathbf{t}}'\mathbf{[n]}, \quad (14)$$

with $\bar{\mathbf{y}}_{\mathbf{t}}'\mathbf{[n]}$ are generated by the FIR filter $f[n]$ and Hadamard transform $\mathbf{H[n]}$ as in (15). This technique requires only one FIR filter for M - channel estimation. Thus, the circuit area is reduced.

$$\bar{\mathbf{y}}_{\mathbf{t}}'\mathbf{[n]} = y[n]\mathbf{H[n]} * h_d[n] * f[n] \quad (15)$$

Timing mismatch coefficients $\hat{\omega}_{ti}$ can be calculated from an updating of the correlation by the LMS algorithm.

$$\hat{\boldsymbol{\omega}}_{\mathbf{t}}\mathbf{[n]} = \hat{\boldsymbol{\omega}}_{\mathbf{t}}\mathbf{[n-1]} + \mu\bar{\mathbf{y}}_{\mathbf{t}}'\mathbf{[n]}\varepsilon[n] \quad (16)$$

where μ is the step-size parameter for LMS algorithm, whereas $\varepsilon[n]$ are delayed versions of $y[n]$ after the high-pass filter $f[n]$.

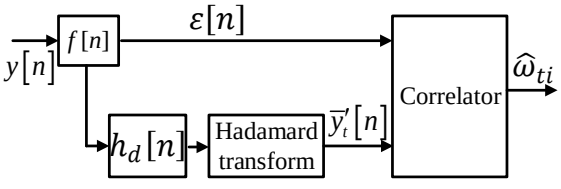

Figure 5. An M-channel TIADC with channel mismatches.

4. Simulation results

To illustrate the proposed techniques, we simulate by using Matlab software. We use a 33-tap correction FIR filter, 13-bit ADC quantization, and a sampling frequency of 2.7GHz. The correction FIR filter uses the Blackman window for truncation and delay.

To demonstrate the effectiveness of the proposed method, the simulated results of a 60dB signal-to-noise ratio (SNR), 2.7 GS/s four-channel TIADC are shown, assuming that channel 0 without timing mismatch is the reference channel for timing mismatch calibration as indicated in Tab. 1. The input signal is bandlimited with a variance $\sigma = 1$ and 2^{18} samples, LMS algorithm with adaptive step $\mu = 2^{-15}$. The signal-to-noise ratio before and after calibration was calculated according to equation (17) and (18) as follow [21].

$$\mathrm{SNR}_{\mathrm{y}} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-y[n]|^2}\right) \quad (17)$$

$$\mathrm{SNR}_{\hat{y}} = 10\log_{10}\left(\frac{\sum_{n=0}^{N-1}|x[n]|^2}{\sum_{n=0}^{N-1}|x[n]-\hat{y}[n]|^2}\right) \quad (18)$$

Table 1. The table of channel mismatch values.

Sub-ADC	Channel mismatches		
	o_i	g_i	t_i
ADC_1	-0.01273	-0.0077	0
ADC_2	0.0020524	-0.0046	0.00042065
ADC_3	0.153	-0.0318	-0.0002235
ADC_4	-0.04653	0.0169	-0.000032916

Fig. 6 shows the simulated output spectrum of the four-channel TIADC before and after channel mismatches correction. The proposed technique has completely eliminated all channel mismatches. The SNDR and SFDR are increased from 19.14dB and 21.22dB to 60.6dB and 93.21dB, respectively. Thus, the performance of TIADC is significantly improved.

Fig. 7(a) and Fig. 7(b) show the convergences of correlation output o_i and ω_{ti} for offset and timing mismatches, respectively. As can be seen, after 25 samples, the offset coefficient $\hat{o}_i$ has converged as in

Fig.7(a). The convergence behavior of the estimated timing coefficients is also very fast. After about 35.10^3 samples, the timing coefficients $\hat{\omega}_{ti}$ has converged.

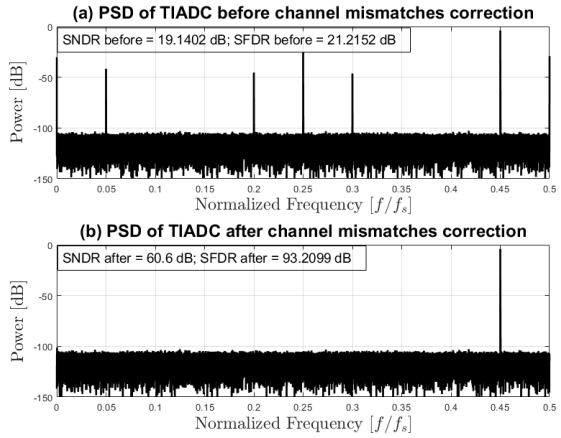

Figure 6. Output spectrum of four-channel TIADC before and after calibration.

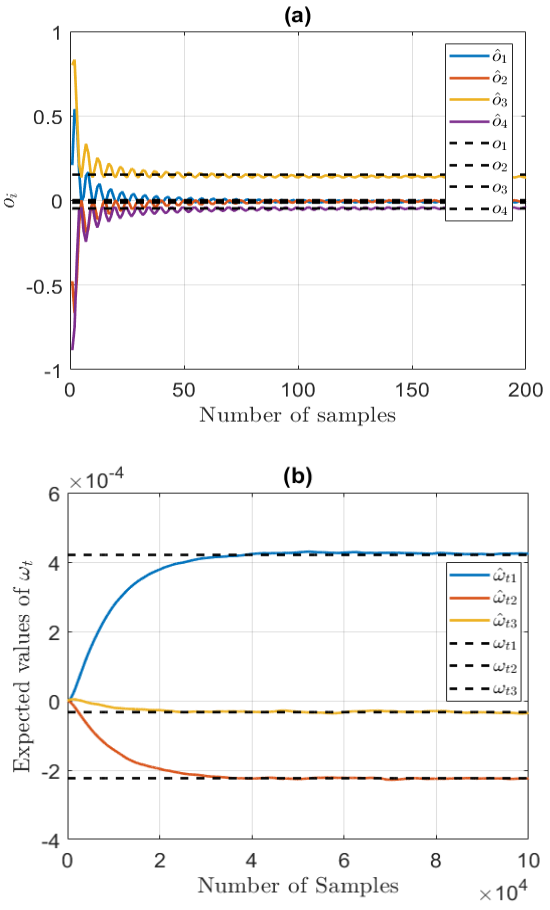

Figure 7. The convergence behavior of channel mismatch coefficients: (a) offset, (b) timing.

The comparison results of the proposed technique with the prior state-of-the-arts is shown in Table 2. The simulation results in this table have clarified the improvement of the proposed technique in both the system performance and the convergence time.

Table 2. A comparison of the proposed with the state-of-the-art techniques

Characteristics	[11] TCAS-I (2013)	[8] TCAS-II (2016)	[18] TCAS-I (2018)	This work
Mismatch types	Gain, timing	Timing	Offset, gain and timing	Offset, gain and timing
Blind calibration	Yes	Yes	Yes	Yes
No. of sub-ADC channels	Any	4	Any	Any
Number of bits	10	11	9	13
SNDR improvement (dB)	62	11	36.55	41.46
SFDR improvement (dB)	30	28	43.72	72
Convergence time (No. of samples)	60k	10k	400k	35k

5. Conclusion

In this paper, an all-digital background calibration technique for offset, gain, and timing mismatches in the *M*-channel TIADC has been presented. The offset mismatch is calibrated by taking the average of output samples of each channel. The gain mismatch is compensated by calculating the power ratio of the sub-ADC with the reference ADC. Finally, the timing skew is compensated by combining the LMS adaptive algorithm and the Hadamard matrix. The simulation results of a 4-channel TIADC have demonstrated a significant improvement in both SNDR and SFDR. In future work, we will consider bandwidth mismatch to further improve the TIADC performance.

References

[1] W. C. Black and D. A. Hodges (1980) Time Interleaved Converter Arrays. *IEEE Journal of Solid-State Circuits*, **15**: 1022–1029.

[2] B. Razavi (2013) Design considerations for interleaved ADCs. *IEEE Journal of Solid-State Circuits*, **48**: 1806–1817.

[3] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi (2001) Explicit analysis of channel mismatch effects in time-interleaved ADC systems. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **48**: 261–271.

[4] C. Vogel (2005) The impact of combined channel mismatch effects in time-interleaved ADCs. *IEEE Transactions on Instrumentation and Measurement*, **54**: 415–427.

[5] P. J. Harpe, J. A. Hegt, and A. H. van Roermund (2009) Analog calibration of channel mismatches in time-interleaved ADCs. *International Journal of Circuit Theory and Applications*, **37**: 301–318.

[6] D. Camarero, K. B. Kalaia, J.-F. Naviner, and P. Loumeau (2008) Mixed-signal clock-skew calibration technique for time-interleaved ADCs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **55**: 3676–3687.

[7] A. Haftbaradaran and K. W. Martin (2007) A sample-time error compensation technique for time-interleaved ADC systems. In *Proceedings of 2007 IEEE Custom Integrated Circuits Conference*. IEEE, 2007, 341–344.

[8] H. Le Duc, *et al.* (2016) All-digital calibration of timing skews for TIADCs using the polyphase decomposition. *IEEE Transactions on Circuits and Systems II: Express Briefs* **63:** 99–103.

[9] H. Le Duc, *et al.* (2015) Hardware implementation of all digital calibration for undersampling TIADCs. In *Proceedings of 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2015, 2181–2184.

[10] N. Le Dortz, *et al.* (2014) 22.5 a 1.62 GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70dBFS. In *Proceedings of 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*. IEEE, 2014, 386–388

[11] J. Matsuno, T. Yamaji, M. Furuta, and T. Itakura (2013) All-digital background calibration technique for time-interleaved ADC using pseudo aliasing signal. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **60**(5): 1113–1121.

[12] C. Vogel, S. Saleem, and S. Mendel (2008) Adaptive blind compensation of gain and timing mismatches in m-channel time-interleaved ADCs. In *Proceedings of 2008 15th IEEE International Conference on Electronics, Circuits and Systems*, IEEE, 2008, 49–52.

[13] S. M. Jamal, D. Fu, N.-J. Chang, P. J. Hurst, and S. H. Lewis (2002) A 10-b 120-msample/s time-interleaved analogto-digital converter with digital background calibration. *IEEE Journal of Solid-State Circuits*, **37**(12): 1618–1627.

[14] H. Le Duc, C. Jabbour, P. Desgreys, O. Jamin *et al.* (2014) A fully digital background calibration of timing skew in undersampling TI-ADC," In *Proceedings of 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)*. IEEE, 2014, 53–56.

[15] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. Van der Weide (2011) A 480mw 2.6GS/s 10b 65nm CMOS time-interleaved ADC with 48.5dB SNDR up to Nyquist. In *Proceedings of 2011 IEEE International Solid-State Circuits Conference*, Feb 2011, 180–182.

[16] E. Iroaga, B. Murmann, and L. Nathawad (2005) A background correction technique for timing errors in time-interleaved analog-to-digital converters. In *Proceedings of 2005 IEEE International Symposium on Circuits and Systems*, May 2005, 5557–5560.

[17] F. Centurelli, P. Monsurrò, and A. Trifiletti (2012) Efficient digital background calibration of time-interleaved pipeline analog-to-digital converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **59**(7): 1373–1383.

[18] Y. Qiu, Y.-J. Liu, *et al.* (2018) All-digital blind background calibration technique for any channel time-interleaved ADC. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **65**(8): 2503–2514.

[19] V.-T. Ta, Y. H. Thi, H. Le Duc, and V.-P. Hoang (2018) Fully digital background calibration technique for channel mismatches in TIADCs. In *Proceedings of 2018 5th NAFOSTED Conference on Information and Computer Science (NICS)*. IEEE, 2018, 270–275.

[20] Y. H. Thi, V.-T. Ta, D. Q. Manh, and V.-P. Hoang (2019) Background calibration of multiple channel mismatches in time-interleaved ADCs," In *Proceedings of 2019 3rd International Conference on Recent Advances in Signal Processing, Telecommunications & Computing (SigTelCom)*. IEEE, 2019, 43–47.

[21] S. Saleem and C. Vogel (2010) On blind identification of gain and timing mismatches in time-interleaved analog-to-digital converters. In *Proceedings of 33rd International Conference on Telecommunications and Signal Processing*, Baden (Austria), 151–155.