challenge in IoT is security and privacy infrastructure when the mobile things move from one area to another.

Paper 4 by Momil Ijaz, Huma Urooj and Muhammad Athar Javed Sethi reports that on-chip bus-based communication has many shortcomings to it, including resource sharing, delay, latency and cost (power and area). Network on Chip (NoC) is an innovation that is planned to eliminate the shortcomings to buses such as compact systems, size, speed, power and area. The goal of working is to design a usable and researchable general-purpose 2x2 mesh NoC architecture, which is not application specific, and optimizes area and power. Desired NoC is coded and deployed on FPGA Spartan-3 kit in a generic mode, with the efficient area and power utilization than traditional deployments.

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We hope you will find this sixteenth issue provoking for your research in the field of context-awareness and being useful to your future work.

About the Editor-in-Chief

Phan Cong Vinh received a PhD in computer science from London South Bank University (LSBU) in the United Kingdom. He finished his PhD dissertation with the title of "Formal Aspects of Dynamic Reconfigurability in Reconfigurable Computing Systems" at LSBU where he was affiliated with the Center for Applied Formal Methods (CAFM) at the Institute for Computing Research (ICR). At present, he is an Associate Professor of Nguyen Tat Thanh University (NTTU) to take on the responsibility of a senior research scientist. He has been author or co-author of many refereed contributions published in prestigious journals, conference proceedings or edited books. He is editor of three books titled, "Autonomic Networking-on-Chip: Bio-Inspired Specification, Development and Verification" (CRC Press, 2012), "Formal and Practical Aspects of Autonomic Computing and Networking: Specification, Development and Verification" (IGI Global, 2011) and "Nature-Inspired Networking: Theory and Applications" (CRC Press, 2018). He has served on many conference program committees and has been general or technical (co)chair and (co)organizer of several international conferences such as ICCASA and ICTCC series. His research interests center on all aspects of formal methods in computing, context-awareness, nature of computation and communication, and applied categorical structures in computer science.