RF power amplifier is an important device not only in wireless communication systems but also in TV transmission, radar systems and RF heating with the amplitude of radio frequency signal increase to high value [4, 5]. Spectral efficiency and linearity are the main elements deriving the design of power amplifier. The most challenging aspect of power amplifier concept is achieving excellent efficiency with linearity [6]. Though, the design of power amplifier has to be accomplished in accordance to the system specifications, such as operating frequency, bandwidth, output power, gain, linearity, efficiency and return loss [7]. According to [8, 9], linearity is required to sustain information for error-free transmission. Efficiency reduces power consumption and improves battery lifespan at the mobile station [5, 10].

The effect of spectral re-growth in power amplifiers has become a major concern in communication systems engineering [11]. This phenomenon causes the apparent presence of nonlinearities in the frequency band which leads to transmission power loss and adjacent channel interference [3]. To reduce the effect of nonlinearity and achieve state-of-the-art system, a power amplifier must be designed carefully to increase high data rate and spectral efficiency for high-speed broadband services. The optimization of these technologies produces higher data rate and higher spectral efficiency from 20MHz signal bandwidth, with a downlink data rates of 100Mbps, and an uplink rate of 50Mbps is obtainable [5, 12].

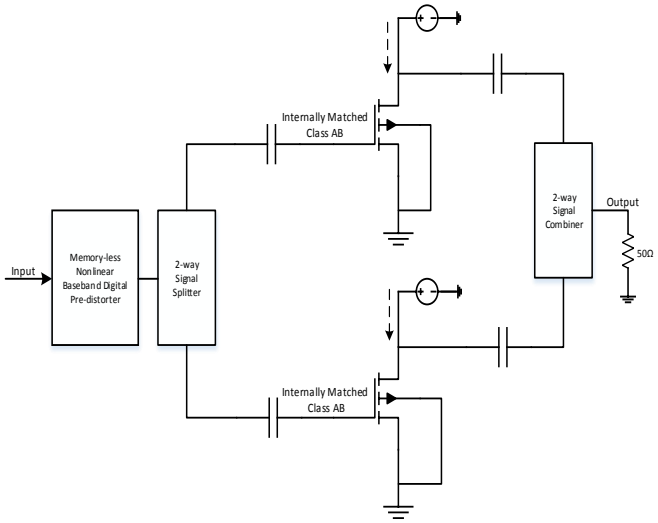

Figure 1. Balanced RF power amplifier architecture

This work discusses the design of a balanced RF power amplifier. The amplitude-to-amplitude and amplitude-to-phase characteristics (AM-AM/AM-PM) of the amplifier used in the modelling of nonlinearities of wireless metropolitan area network IEEE 802.11a OFDM transceiver using Simulink version R2011a configuration is presented. The aim of this study is to design and implement a 5G power amplifier that can have increase in power added efficiency and respond to high linearity. This is in view of the demand to reduce power amplifier energy consumption and the need for increase in battery life span. The objectives of this study is to design the proposed balanced RF power amplifier and implement the prototype. The design simulation and prototype measurement will be performed and compare. Amplitude and phase raw data of the proposed balanced amplifier will be extracted and converted to polynomial for linearization. A pre-distortion technique is proposed for cancellation of the proposed balanced RF power amplifier. Section 2 presents Power Amplifier Linearity, Efficiency and Output Power Requirement. The subsection 2.1 explains the Trade-off between linearity and efficiency. Section 3 describes in detail the circuit design architecture of the balanced RF power amplifier and the proposed system, while 3.1 discusses the circuit analysis of balanced RF power amplifier. Section 4 explains the design and simulation of a balanced RF power amplifier, while 4.1 presents simulation results and discussion. The design was implemented. A prototype for the balanced RF power amplifier has been shown. AM-AM and AM-PM measurement was conducted and is presented in section 4.1 respectively. Section 6 discusses the Linearization of balanced RF power amplifier Using Adaptive DPD. The section also covers the extraction and modelling of AM-AM and AM-PM polynomials in the pre-distorter. The work based on results from simulations and measurements discusses a potential technique to improve the efficiency in wide range linearity. Finally, the paper is concluded with the discussion in Section 7.

2. Power Amplifier Linearity, Efficiency and Output Power Requirement

The 5G-LTE multicarrier systems require a more linear radio frequency amplification and higher efficiency. A balanced power amplifier is employed to provide a multicarrier signal, while putting linearity, efficiency and output power into consideration. The IEEE 802.11a standard for information technology and wireless communication systems have not identify the minimum requirement for the power amplifier intermodulation distortion. However, stated the maximum allowable intermodulation distortion in the system level requirement. These include the adjacent channel power ratio (ACPR), error vector magnitude (EVM) and envelope spectral mask (ESM).

The ACPR is the ratio between the total power transferred to the main channel and the signal power transferred to the adjacent channel. The multicarrier transmitter signal passing through the power amplifier is characterized using a complex RF band. The RF band is overwhelmed by the RF PA nonlinearity called spectral regrowth. This type of power amplifier nonlinearity is measured using the adjacent channel power ratio. There are two ways in which ACPR is measured. The first way is by defining 10*log of the ratio of the total p_{out} to the adjacent channel power expressed by.

$$ACPR_{dBc} = P_{im3} + 10\log\left[\frac{C^3}{A+B}\right]. \qquad (1)$$

where P_{im}^3 is the third order intermodulation distortion, C is the number of carriers or the main channel, A is the upper adjacent channel and B is the lower adjacent channel. The measurement of the total output power and the adjacent channel power are calculated in logarithmic ratio. The second is based on the ratio of the specific output power in a less significant bandwidth around the centre of the carrier to the adjacent channel power. The smaller bandwidth is equal to the bandwidth of the adjacent channel signal, having an equivalent bandwidth of the main channel. The spectral mask is identified by the IEEE 802.11a standard as a metric for passing or failing signal at the output of the power amplifier [13]. The spectral mask provides facts about the dispersal of the modulated channel spectral energy. The test is through if the RF spectrum is within the stipulated limit defined by the mask, while the test fails if the energy level is not beyond the mask limit.

The error vector magnitude (EVM) also estimates the properties of deficiency in the communication system constellation. The error vector *(E(c))* is the variation between the actual transmitted constellation point *(AT(c))* and the ideal constellation point *(I(c))*. The error vector magnitude (EVM) can be expressed in RMS form by.

$$EVM_{rms} = \sqrt{\frac{\frac{1}{N}\sum_{c=1}^{N}|E(c)|^2}{\frac{1}{N}\sum_{c=1}^{N}|I(c)|^2}}. \qquad (2)$$

where N is the total number of constellation points defining the level of modulation. The N is used for *EVM* calculation. $I(c)$ is the c^{th} number of normalised constellation points and $E(c)$ can be expressed by.

$$E(c) = x(c) - y(c). \qquad (3)$$

where $x(c)$ is the measured normalised symbol. The rms value of the error vector magnitude is calculated by taking the average value of all the frames. In the measurement, it is recommended by the IEEE 802.11a for WLAN standard to take a large number of transmitted frames of at least 20 frames [13]. The computation of error vector magnitude for the IEEE 802.11a, WLAN standard is expressed in [13] by.

$$EVM_{rms} = \frac{\sum_{a=1}^{N_f}\left(\sqrt{\frac{\sum_{v=1}^{L_p}(\sum_{n=1}^{52}\{(\boldsymbol{I}-\boldsymbol{I_0})^2+(\boldsymbol{Q}-\boldsymbol{Q_0})^2\})}{52L_p\cdot P_a}}\right)}{N_f}. \qquad (4)$$

let $\boldsymbol{I}$, $\boldsymbol{I_0}$, $\boldsymbol{Q}$ and $\boldsymbol{Q_0}$ sequentially be expressed as: $[I(a,v,n), I_0(a,v,n), Q(a,v,n)$ and $Q_0(a,v,n)]$, where N_f is the frame number, L_p is the packet data length, P_a is the average power of the constellation diagram and n is the OFDM symbol subcarrier. EVM can also be achieved in percentage by using the rms value. In the system level, it is very important figure of merit to evaluate the precision of the OFDM signal. The $EVM_{\%}$ can be expressed by.

$$EVM_{\%} = \frac{\sqrt{\frac{1}{N}\sum_{a=0}^{N_f-1} I_{er}(a)^2 + Q_{er}(a)^2}}{N_r}\times 100\%. \qquad (5)$$

where N is the number of symbols, N_r is the normalized reference of the EVM, a is the symbol index, while

$$I_{error} = I_{reference} - I_{measured}$$

$$Q_{error} = Q_{reference} - Q_{measured}$$

The EVM can as well be measured in decibel (dB) as expressed below.

$$EVM_{dB} = 10\log_{10}\left[\frac{P_{error}}{P_{reference}}\right]. \qquad (6)$$

Where P_{error} stands for the error vector power, and $P_{reference}$ is the reference constellation point power for both single and multiple carrier modulation. It is the average power of the reference constellation. In the IEEE 802.11 standard for LTE, the adjacent channel power ratio (ACPR), envelope spectral mask (ESM) and error vector magnitude (EVM) are demanding as expressed in the existing standard.

2.1. The trade-off between Linearity and Efficiency

The aim of realizing energy efficient power amplifier with excellent linearity is to have a system with high efficiency over a magnificent range of input power. The most challenging task in RF power amplifier design is to obtain high efficiency with a wide range of linearity [14, 15]. However, achieving high efficiency with a wide range of linearity at the same time is a difficult task, except with advent of linearization and efficiency enhancement approaches. At low-level output power, high efficiency can be achieved if the efficiency enhancement method in the linear operation region of RF power amplifier is adopted. Maximum efficiency can, however, be realised once the output power of RF power amplifier reaches almost the maximum saturation level, which is the 1dB compression point. This leads to serious intermodulation distortion where efficiency drastically decreases with the decrease in output power.

However, the RF power amplifier must be in linear mode at the whole dynamic range of time to maintain the level of efficiency. The peak power range can escalate to 8-10dB output power back-off. This is applicable for cascade amplifiers. It is a significant challenge for traditional single-stage RF power amplifier due to the effect of the peak-to-average-power ratio (PAPR) that operates on high output power back-off. RF power amplifiers operating on lager

output power back-off end off with a very low efficiency. A study in [12] has shown that low efficiency must be reduced to conform to the standard or will otherwise affect the operation of other applications.

However, RF power amplifier design has continued to be a challenging task when trying to satisfy this linearity-efficiency and power requirement trade-off. Previous studies have shown that there is no breakthrough in the trade-off. To optimise linearity-efficiency trade-off, more investigation is required on various power amplifier architectures.

3. Balanced RF Power Amplifier Circuit Design Architecture

Figure 1 has shown the balanced RF power amplifier architecture. The balanced power amplifier is a cascaded system with two transistor device opposite to each other. The two amplifiers share the same input and output. They have parallel output power capability, but different in the biasing circuit. The two amplifiers are operating in class-AB with the first one in first carrier stage and the second one in second carrier stage respectively. At this point, the first carrier stage is referred to the first amplifier, while the second carrier stage refers to the second amplifier. The signal from the input is divided equally using a 3dB signal splitter. The splitter is designed with 90^0 phase difference and same amplitude, to drive the two cascaded class-AB amplifiers. The output of both amplifiers are connected to a combiner which collects the amplifiers signals to the final stage of amplification [16, 17].

The balanced RF power amplifier attains high efficiency as a result of output power back-off over the traditional single stage amplifier. Hence, the multicarrier applications are affected by nonlinear distortion due to peak to average power ratio (PAPR), which the efficiency of the power amplifier can be enhanced by the used of efficiency enhancement and linearization techniques.

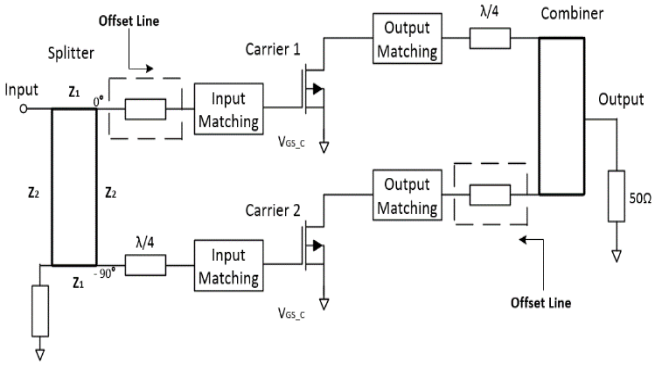

Figure 2. Proposed schematic diagram of the balanced RF power amplifier with offset lines

Figure 2 has shown a proposed balanced RF power amplifier with two amplifiers parallel to each other having equal output power capability. The two amplifiers have the same bias point which means they are both carrier amplifier stage operating in class AB mode. The phase difference between the two amplifiers is 90^0 phase shift. A special signal splitter was separately designed for the input. A coupler was also designed for the output. Independent measurements were taken in term of operational bandwidth and frequency response for both the splitter and the output coupler. In the design, no mode was chosen to behave as the carrier amplifier. Both class-AB modes operate at the same time and capable of improving the efficiency. Resonator circuits are applied to the input of the first carrier and output of the second carrier. These acts as the summing circuits which act as a phase difference signal compensator. The circuits constructively supplement the signal from the two amplifiers to the output load. The quarter-wave transmission line similarly applied to the input of the second carrier and the output of the first carrier. According to the study, the proposed balanced RF power amplifier design complexity increases and equally improve the efficiency with a wide range of linearity which will be discussed in the next section.

3.1. Balanced Power Amplifier Circuit Analysis

This section derives and demonstrates the equation that runs the relationship between input current (I_{in}) and input voltage (V_{in}) to the output current (I_{out}) and output voltage (V_{out}) in the transmission line, showing how the frequency dependent impedance of the material present the attenuation and distortion of the high-frequency signal as expressed in matrix form [14, 18].

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \cosh \pi/2 & z_o \sinh \pi/2 \\ 1/z_o \sinh \pi/2 & \cosh \pi/2 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix}. \quad (7)$$

The source impedance $Z_{in} = V_{in}/I_{in}$, Z_o is the characteristic impedance of the transmission line, while Z_L is the load impedance given as $Z_L = V_{out}/I_{out}$. Hence, the source impedance Z_{in} can be expressed by.

$$Z_{in} = \frac{Z_L \cos \pi/2 + jZ_o \sin \pi/2}{j(Z_L/Z_o)\sin \pi/2 + \cos \pi/2}. \quad (8)$$

From the wave equation to the relationship between voltage and current, quarter wave transmission line source Z_{in} can be defined by.

$$Z_{in} = \frac{V(-l)}{I(-l)} = Z_o \left[\frac{V_o^+ (e^{j\beta l} + \Pi e^{-j\beta l})}{V_o^+ (e^{j\beta l} - \Pi e^{-j\beta l})} \right]. \quad (9)$$

This can be expressed by the impedance function in by expanding the (9) while giving a common source impedance for both voltage and current.

$$Z_{in} = Z_o \left[\frac{\left[e^{j\beta l} + \left(\frac{Z_L - Z_o}{Z_L + Z_o} \right) e^{-j\beta l} \right]}{e^{j\beta l} - \left(\frac{Z_L - Z_o}{Z_L + Z_o} \right) e^{-j\beta l}} \right]. \quad (10)$$

This equation can be expanded by.

$$Z_{in} = Z_o \left[\frac{Z_L \left(e^{j\beta l} + e^{-j\beta l} \right) + Z_o \left(e^{j\beta l} - e^{-j\beta l} \right)}{Z_o \left(e^{j\beta l} + e^{-j\beta l} \right) + Z_o \left(e^{j\beta l} - e^{-j\beta l} \right)} \right]. \quad (11)$$

and this can be extended in sine waveform by.

$$Z_{in} = Z_o \left[\frac{Z_L (\cos \beta l) + jZ_o (\sin \beta l)}{Z_o (\cos \beta l) + Z_L (\sin \beta l)} \right]. \quad (12)$$

Finally, the impedance Z_{in}, looking into the transmission line is given by.

$$Z_{in} = Z_o \left[\frac{Z_L + jZ_o \tan(\beta l)}{Z_o + jZ_L \tan(\beta l)} \right]. \quad (13)$$

The two-stage balanced RF power amplifier is shown in figure 2 with the quarter wavelength at the output of the first carrier and the input of the second carrier amplifier respectively. These act as the basis for the impedance to stay low when the two carriers are on the active stage.

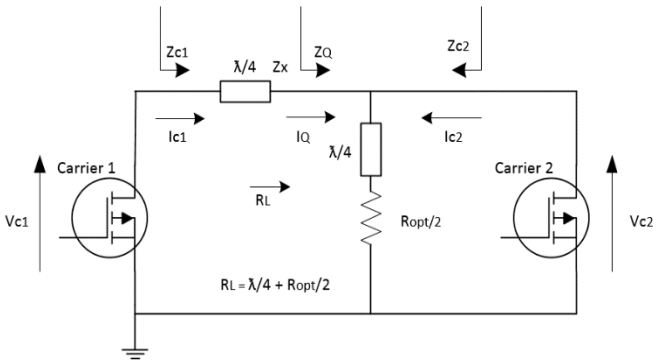

Figure 3. Current and voltage analysis diagram for balanced power amplifier

Figure 3 shows a balanced RF power amplifier analysis diagram which will be used for the current and voltage analysis. The phase output current of the first carrier (I_{c1}) leads the phase output current of the second carrier (I_{c2}) by 90^0. This implies that the phase difference of the splitter is separating the two amplifiers by 90^0 phase shift. Nevertheless, the operating principle of the balanced amplifier two-stage load modulation can be derived by splitting the level of input signal to high-level drive. In this mode, first carrier (I_{c1}) and second carrier (I_{c2}) are set to be turned on and there will be current flow through the circuit. When the balanced amplifier is in ON state, the current envelope can be expressed by.

$$I_{c1} = \frac{I_{\max}}{3}(1+x). \quad (14)$$

$$I_{c2} = \frac{I_{\max}}{3}(x+1). \quad (15)$$

At high-level drive, the x component will have a value of 1, where the two carrier amplifiers will turn on. The effective impedance (Z_Q) will have to pull influence on both carriers at the load as expressed below.

$$Z_Q = R_L \left[1 + \frac{I_{c2}}{I_Q} \right]. \quad (16)$$

and

$$Z_{c2} = R_L \left[1 + \frac{I_Q}{I_{c1}} \right]. \quad (17)$$

where the resistive impedance of the quarter wavelength increases, the two carrier amplifiers acts as load modulation. The quarter wavelength transmission line input, output transformation and the characteristic impedance can be expressed by.

$$Z_{c1} = \frac{Z_x^2}{Z_Q}. \quad (18)$$

The output impedance can be substituted to the effective impedance (Z_Q) and can be seen by both amplifiers. The output impedance is written as.

$$Z_{c1} = \frac{Z_x^2}{\left[R_L \left(1 + \frac{I_{c2}}{I_Q} \right) \right]}. \quad (19)$$

The effective output voltage (V_{c1}) of first carrier amplifier is expressed by.

$$V_{c1} = Z_{c1} \times I_{c1} = I_{c1} \times \left[\frac{Z_x^2}{R_L \left(1 + \frac{I_{c2}}{I_Q} \right)} \right]. \quad (20)$$

Since $I_Q = V_{c1}/Z_x$ then output voltage becomes.

$$V_{c1} = \frac{I_{c1} \times Z_x^2}{R_L\left(1 + \frac{I_{c2} \times Z_x}{V_{c1}}\right)}. \quad (21)$$

I_{c1} *and* I_{c2} have been substituted into Z_{c1} to become.

$$V_{c1} = \left(\frac{Z_x}{2R_L}\right)(I_{\max})(Z_x(1+x)) - 2R_L x^2 + R_L x. \quad (22)$$

But $R_L = R_{opt}/2$. Hence the output voltage will be.

$$V_{c1} = \left(\frac{Z_x}{R_{opt}}\right) (I_{\max})\left(Z_x(1+x) - 2\frac{R_{opt}}{2}x^2 + \frac{R_{opt}}{2}x\right). \quad (23)$$

Then $Z_x = R_{opt}$

$$V_{c1} = R_{opt} + I_{\max}\left(-x^2 + \frac{x}{2}\right). \quad (24)$$

Finally, the mathematical illustration has shown that the output voltage maintains the stability at a high stage when the two carriers remain in the active stage. The output voltage increases negligibly.

4. BPA Design and Simulation

The balanced RF power amplifier has been designed and discussed in this paper, using two transistor models for high data rate, providing efficiency with a dynamic range of linearity. Dynamic load adaptation is conveyed by the use of transmission line impedance inverter of 50Ω quarter wavelength. In the design of this amplifier, there are stages that are followed to achieve high-level performance [19, 20]. The first stage of the design is DC circuit design and simulation. Simulation of the DC circuit determines the bias point and bias network. This is in accordance with the class of operation and power requirement. The bias condition set drain-source voltage (Vds) = 28V, drain-source current (Ids) = 422mA and gate-source voltage (Vgs) = 2.7V. The bias network is designed based on class-AB carrier. The DC simulation results also indicate the class of operation. The main purpose of good biasing is to prevent signal reflection. The DC quiescent current is obtained to prevent signal distortion [5]. The radio frequency signal is prevented from going back to the DC source. For the matching network, this transistor requires no matching process, as indicated in the datasheet of the component, input and output impedance are internally matched. The 21mm length of microstrip line are connected using line-calc from Agilent advanced design system simulator (ADS) with RT 5880 substrates, parameters; Er = 2.2, H = 0.508mm, zo = ohms, T = 3um and TanD = 0.017. The 50Ω impedance of 90^0 open and a short circuit is incorporated to the right angle of the RF blocking transmission lines. A class-AB power amplifier element values have been positioned using tune tool of the ADS simulator for best performance of the proposed system.

Linear and nonlinear simulation was performed for class-AB design. The design and simulation process for class-AB amplifier is necessary in order to prepare the single stage class-AB design into a multiple stage balanced power amplifier. The linear simulation has shown a good flat gain, where the S_{11} is almost 14dB, the return loss, S_{11} and S_{22} are also satisfactory. The nonlinear single tone simulation result of class-AB amplifier was achieved. However, it also produced up to 29% PAE at 39dBm P_{1dB}. A 3dB 2-ways 90^0 hybrid splitter was designed using 100Ω impedance for optimum matching. This is to achieve 90^0 phase difference between the first carrier class-AB and the second carrier class-AB amplifier. For a two-stage balanced PA, the first carrier and second carrier bias points are in the same mode, the input-output matching circuitry and the output impedances are similar as well. For the two-way splitter, various simulation tests were performed such as isolation response over the operating bandwidth, phase difference across port 1-2 and 1-3, and insertion loss response of the splitter [3]. From the 3dB splitter, the insertion loss achieved is reasonably low due to the high return loss, the phase difference of two signals are parallel to each other by 100Ω, which means they are separated by 90^0 and have equal magnitude, and the isolation between 2 and 3, which results to -48.56dB at 2.655GHz centre frequency. Consequently, these results represent a response to protect the amplifier with all the instruments connected to it and allow measurement with reasonable accuracy. At the output of the two-stage amplifier is a combiner coupling the first carrier and second carrier amplifiers signal to the output of the balanced amplifier [3, 21].

Table 1: Performance comparison with selected work based on power amplifiers

Device	Freq [MHz]	PAE [%]	P_{out} [dBm]	Gain [dB]	Reference
LDMOS	2655	51	41	14.6	Balanced
LDMOS	2655	29	39	15	Class-AB
LDMOS	2140	54	48.77	30	[4]
GHEMT	2655	37.14	41.18	12.78	[10]
GHEMT	2125	33.4	34.9	7.7	[11]
GHEMT	2500	48	46	13.4	[13]
LDMOS	1900	50	40	14.5	[14]

Table 1 shows the performance of the current work compared a few selected PA's reported in the literature, taking account of operating frequency, output power, efficiency and gain. In [4] a power amplifier consist of up to 54% PAE at 2.14GHz

operating frequency is presented. The design presented a two-stage line-up of Doherty amplifiers, consisting of a High Voltage HBT Doherty final design cascaded with a 20W LDMOS Doherty driver, exhibiting up to 325W (55dBm) power to improve the gain to 30dB. In the case of [10] a high power hybrid envelope elimination and restoration transmitter were designed using gallium arsenide high electron mobility transistor (GaN-HEMT) at 2.655GHz operating frequency. The design introduced a conventional hybrid switching amplifier with up to 71.2% PAE. However, the efficiency of H-EER transmitter reduced to 37.04% at 41.18dBm P_{out}. In [11] a conventional balanced amplifier with 90^o branch line hybrid coupler (BLHC) was used to achieve power matching rather than maximum high gain. The impedance matching is not excellent and there is inherent out-of-phase characteristic cause from the properties of 90^0 BLHC. To improve the performance and correct the high signal reflection, an auxiliary amplifier was added to the conventional balanced amplifier design, only to increase the PAE to 33.4%. The design for [22] used up to 250W output power at saturation to achieve 60% drain efficiency. The final 40W GaN-HEMT Doherty power amplifier design used a digital pre-distorter to enhance linearity, as a result, experienced a reduction in PAE to 48%. Finally, in [14] a 10W, Si-LDMOS transistor power amplifier was presented with 50% PAE, 14.5dB gain achieved at 41.8dBm saturation within 1.8 to 2.0GHz operating frequency. The drawback of [14] is that heat sink is used due to excessive heating produced by the amplifier, which extensively affects the general performance of the system.

However, the current work presents a simplified balanced amplifier using Si-LDMOS transistor, while achieving up to 53% PAE, 14dB gain at 41dBm P_{1dB}. This design is matched perfectly due to the internal input and output matching network in the transistor device. There is no evidence of leakage or signal reflection from the first stage of the design to the design of balanced amplifier. Another advantage of this design is for its simplicity, requires no auxiliary amplifier or additional cascade Doherty device to improve the efficiency. Additional circuit accounts for extra power consumption, but have negligible impact to the overall efficiency of the amplifier [3].

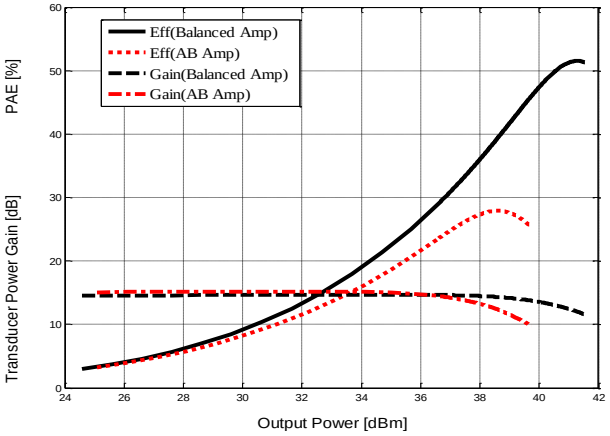

Figure 4. Simulated results of the proposed balanced RF power amplifier and conventional class AB showing PAE and gain characterization

4.1. Simulation Results and Discussion

The proposed balanced amplifier consisting of two similar class-AB amplifiers tested and simulation results are discussed. The results have shown the signal waveforms for best of performance and hence the best choice for LTE base station applications. Figure 4 shows the results of the balanced amplifier in comparison with the conventional class-AB amplifier. This indicates good performance from the balanced amplifier, achieving up to 53% PAE with 14dB gain at 41dBm P_{1dB}, as against the conventional class-AB amplifier with 29% PAE, 39dBm P_{out} and 15dB gain.

These results presented above is based on the linear simulation was conducted for the nonlinear simulation. The results obtained are the gain compression for 1dB compression point. The gain compression result is flat as expected, excellent input and output return loss was also achieved as shown in figure 4 The flat gain, S(2, 1) is almost 14 dB, the return loss, S(1, 1) and S(2, 2) was also achieved at 1 dB compression point. The results have shown quite a few kinds of signal waveforms to characterize the best of performance and the best choice for 2.620-2.690 GHz applications.

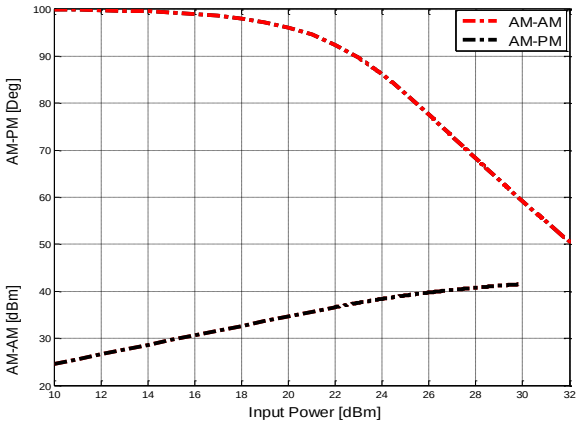

Figure 5. AM-AM and AM-PM characterization of the balanced RF power amplifier

In the one-tone nonlinear simulation test, the obtained AM-AM and AM-PM characterization parameters are shown in figure 5. These are very important parameters in the characterization of PA and demonstrate that AM-AM distortion appears in a nonlinear PA, while the AM-PM distortion appears in MOSFET PA's and produces memory effects.

5. Implementation of Balanced RF Power Amplifier

5.1. Circuit Design Layout

The balanced power amplifier was designed and implemented using ADS software with RF field effect Si-LDMOS 15.5W transistor at 2.620-2.690GHz frequency band. The final stage circuit of the amplifier is fabricated with RT 5880 substrates,

H=0.5mm and relative permittivity of 2.2. Figure 6 shows the layout of the balanced RF power amplifier. In order to experimentally verify the proposed power amplifier circuit topology, the agilent advanced design system generated microstrip layout was used. The layout was exported as Gerber files from ADS and it was milled on a printed circuit board known as PCB. Note that metal pads have been added in the layout as ground plane and power supply connection in the layout. Further, the amplifier has been subjected to following mechanical engineering:

• The length of the cooling ribs was cut to fit the card
• Holes for the transistor was milled out
• A total number of 44 screw holes were threaded into the board
• 4 for the transistors
• 36 for in and outsides of the board
• 4 for each SMA connectors

The screws were tried to be positioned so that they would have minimal impact on scattering field from the lines. At the same time, it was necessary to place multiple screws relatively close to the transistor in order to provide a good signal ground at this point. The same procedure was done with screws at each SMA connector. The components were fitted on the finished circuit board.

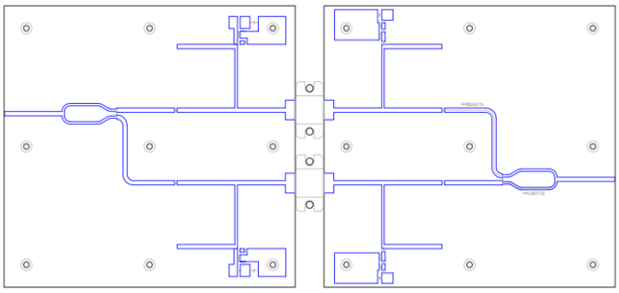

Figure 6. Design layout of balanced RF power amplifier

5.2. Circuit Prototype

The balanced RF power amplifier circuit is fabricated with RT 5880 substrates, H=0.5mm and relative permittivity of 2.2. The RT/duroid 5880 high-frequency laminate from Rogers Corporation is used. The substrate material is good for microstrip and strip-line applications. Because of the uniform dielectric constant over a wide range of frequency and the low dissipation factor of RT/duroid 5880, it extends its usefulness compared to FR-4 substrate in high-frequency Ku-band and above. The Line-Calc application from ADS is able to calculate the width and the length of microstrip line given the characteristics impedance and electrical distance or vice versa at 2.655GHz. Some important characteristics of RT/duroid 5880 such as dielectric constant, the height of board and conductivity are defined in ADS Line-Calc.

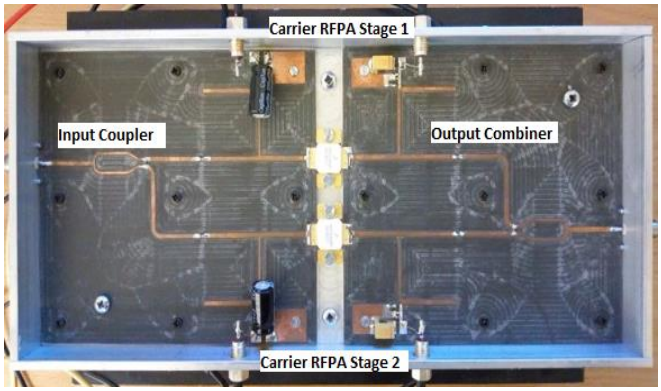

Figure 7. A prototype of the two-stage balanced RF power amplifier Fabricated with FR-4 substrate

While verifying the impedances in schematic and layout, the Gerber files are created from the layout and the circuit is milled on the RT/duroid 5880 board. During the RF operation, heat generation of the transistor would be one of the biggest problems causing performance degradation. Therefore, the transistor has to be mounted right on a heat sink in order to diffuse generated heat. In this project, a large piece of aluminium plate will be used as a heat sink and the skeleton to support the PA. The transistor is mounted on the aluminium plate with thermal paste glued in between in order to maximize heat transfer. The PA consists of two parts, the input board and the output board. SMA connectors are inserted at the input and output terminals. Banana plugs must be used for power connection as required by the competition rules. Vias are created by putting wire through drilled holes or inserting long copper tape through cut slits as connection bridges between the top and bottom ground planes. Vias should cover as much area as possible on the PA in order to provide the same reference level between the top and bottom ground planes. Components are then soldered on the board. 300pF capacitors are used as coupling capacitors at the input and output board. 1pF/1000pF/33pF capacitors are used as a decoupling capacitor in the gate bias. 1pF/1000pF/33pF/ capacitors are put in parallel and used as decoupling capacitors in drain bias.

5.3. Measurement

The design of the proposed balanced RF power amplifier circuit has undergone simulation test and measurement was performed on the fabricated circuit. The measurement result is focussed on the phase variation of the power amplifier using various frequency band to report the differences at some points. The measurement includes determining the linearity of the amplifier by means of looking at the power from the input to the power to the output and also discuss improvement achieved from the measured PAE.

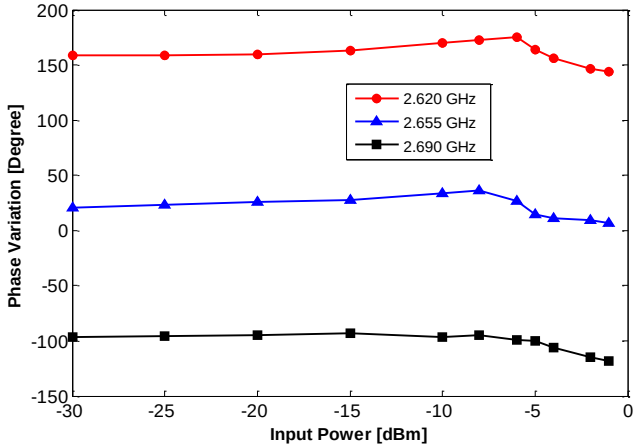

Figure 8. Phase variation of the proposed balanced RF power amplifier

Figure 8 shows the phase variation of the proposed balanced RF power amplifier which was derived as a function of the input power level. The result shows a range of frequency band used which is within the LTE mobile frequency level. The phases of the amplifier path are almost fixed along with bias condition throughout the range of the power used in the amplifier. There is no record of phase variation between the first carrier and second carrier in the low or high power region. The reason behind this development is because the balanced amplifier consists of same class-AB amplifiers in both carriers.

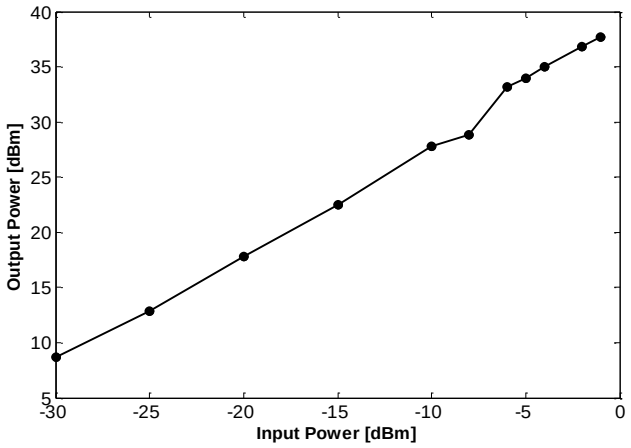

Figure 9. Output versus the input power of the balanced RF power amplifier

Nevertheless, the result shows power derive has increased at the output level when compared with that of input as the phase variation through both carriers path is almost close. It is anticipated a small drop at the full drive and both signals will look equal and disappear. The power that has been used between the input and the output of the amplifier is shown in figure 9. It represents the evaluation of the phase variation of the signal. And this clearly shows how much power has been derived through the amplifier. Up to 37dBm output power has been accomplished at the linear region of the proposed balanced RF power amplifier.

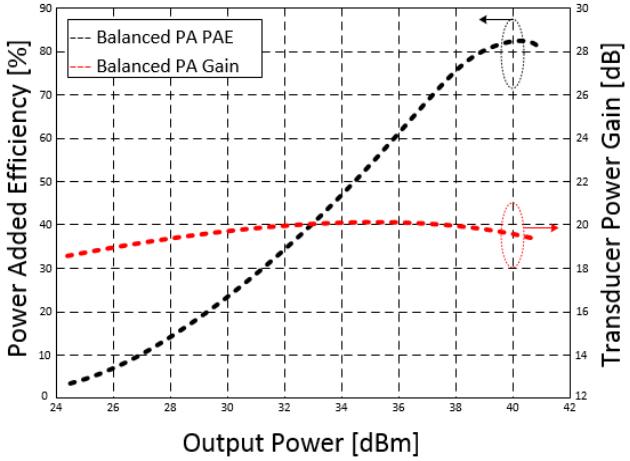

Figure 10. Measured results of the proposed balanced RF power amplifier with improved power added efficiency and gain

Figure 10 shows the performance of proposed balanced RF power amplifier through measured PAE and gain. The same frequency range of 2.620-2.690 GHz has been used for the simulation as well as the measurement. 1dB compression point of the amplifier was used to obtain up to 40dBm of the output power because of the two cascaded class-AB amplifiers working actively at the same time. However, the balanced amplifier output saturation power (P_{sat}) point reached up to 40.90dBm. The power added efficiency of the balanced amplifier at 40dBm and 40.90dBm were 83% and 81.5% respectively. While the gain of the amplifier reached up to 20dB which was reduced to 19.5dB before saturation point. Increase in gain and PAE improves the linearity of the amplifier. This is attributed to the input and output offset lines used in the design and fabrication. This performance shows that the design and fabrication of the proposed balanced RF power amplifier has achieved a substantial improvement in this class of power amplifiers.

6. Linearization of Balanced RF Power Amplifier Using Adaptive DPD

In this section, the balanced RF power amplifier was linearized using the AM-AM and AM-PM transfer functions to generate polynomials in the MATLAB. The extracted AM-AM and AM-PM data are measured in the context of the normalized input voltage as a function of the output voltage. The MATLAB curve fitting generated AM-AM polynomials is expressed as: a_6 = 33.066, a_5 = -85.52, a_4 = 82.06, a_3 = -34.052, a_2 = 2.85, a_1 = 3.21 and a_0 = -0.01. The AM-AM distortion is effected by the device reaching a saturation point. The normalized input voltage as a function of output phase of the balanced amplifier is also considered with the following AM-PM MATLAB fitted coefficients to generate polynomials expressed as: b_6 = 3.5485, b_5 = -5.7836, b_4 = 3.0384, b_3 = -0.8434, b_2 = 0.1826, b_1 = -0.0225 and b_0 = 0.1001. The AM-PM distortion is effected by the device reaching a saturation point. This data will be embedded in the device under test (DUT) of a simulink transceiver system