An SoC Evaluation Platform for Dual Link MIMO-OFDMA Communications

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***Abstract*—In this paper, an efficient and flexible SoC platform integrated with intellectual property (IP) cores for multi-input multi-output orthogonal frequency division multiple access (MIMO-OFDMA) transceiver of IEEE802.16e-2005 standard is presented. The proposed platform supports uplink/downlink and is integrated with the evaluation system. The hardware and software design have been synthesized and verified. The proposed platform provides a complete system design. It is a flexible prototyping for worldwide interoperability for microwave access (WiMAX) communication system. Designers could use platform-based design approach as an effective strategy to cope with product complexity and time-to-market at all levels. For the verification stage, designers can use the hardware/software (HW/SW) co-verification strategy to debug hardware component, which will help designers identify more faster. In this proposed platform, which introduces the figure file to be the transmission media. Designers validate their design in bit error rate/signal-to-noise ratio (BER/SNR) waveforms traditionally. In this proposed platform, designer could verify the decoded results in various environment by LCD panel.**

I. Introduction

To pursue even more high data rate, spectrum efficiency, and mobility, MIMO/OFDMA is a promising technique. WiMAX and LTE both provide such capabilities. For rapid prototyping and efficient evaluation of communications systems, the SoC design platform play an important role. With design reuse concept and good verified intellectual properties (IPs), productivity can be greatly improved. In the previous literature, Field Programmable Gate Array (FPGA) devices [1], development and testing of a mobile WiMAX physical-layer [2], utilizes software radio solution [3], mixed hardware-software testbed [4] have been developed and published. The primary achievements in this paper are as follows: (1) Flexible prototyping, (2) Fast verification, (3)Validate performance clearly, (4) Complete system design.

Compared with others, the proposed platform provides a faster verification flow for a complete performance evaluation. Designers can use the platform-based design for verification in every design stages to cope with product complexity and time-to-market. Moreover, SoC design methodology minimizes verification uncertainties, which greatly reduces design effort and risk. This approach consumes much less time than field testing of the system in all of the possible scenarios.

The organization of this paper is as follows. In section II, the practical platform architecture is proposed. In section III, we introduce the integration and verification flow. In section III, the proposed baseband transmission model is given Section V presents platform emulation results with some related literature comparison. Finally, this paper is concluded in VI.

II. Platform Architecture

A. The Proposed Downlink Transceiver Architecture

The proposed transceiver architecture [5] for 802.16e-2005 downlink system is illustrated in Fig. 1. The proposed 4x4 downlink receiver architecture [5] could be divided into two parts:

I. First part is the initial synchronization circuit, which included frame detection, boundary detection, fractional carrier frequency offset (FCFO) estimation and compensation, CP removing, fast Fourier transform (FFT) and integer CFO (ICFO) estimation and compensation.
II. Second part is the signal processing on the frequency domain, which included subcarrier de-allocation, channel estimation, SFBC decoder and ICI mitigation module.

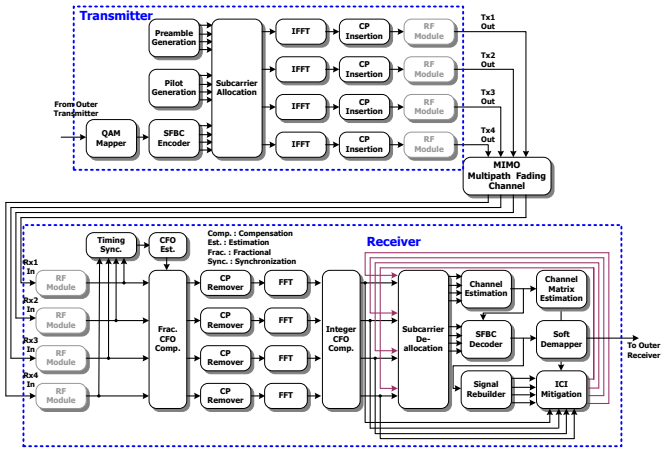

Fig. 1. Proposed 4x4 downlink transceiver.

Fig. 2 shows the logic design for the proposed SFBC decoder. Although the algorithm is simple but lots of multipliers and adders are required. The proposed SFBC decoder is divided into four blocks, and a module with four multiply-accumulate (MAC) cells will calculate the four blocks in different time. A complex multiplier originally needs three

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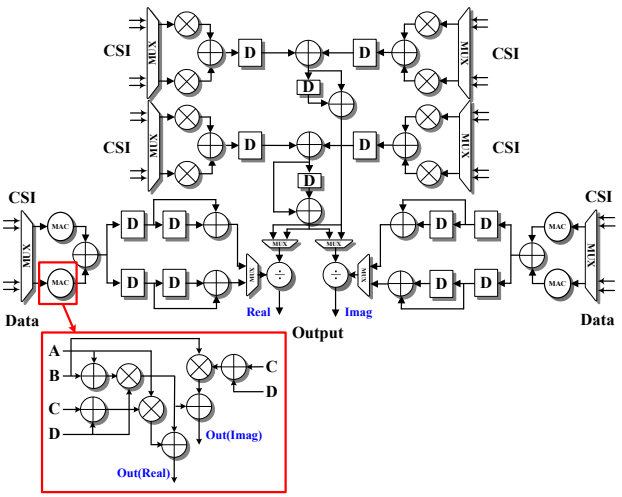

Fig. 2. SFBC decoder logic design.

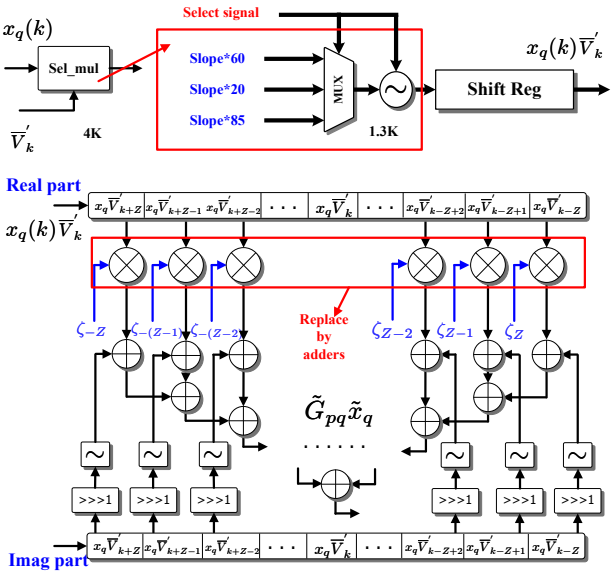

Fig. 3. Proposed channel matrix hardware design.

addition and four real multiplication operation. By rearranging the terms of imaginary part and real part, the original equation can be rewritten in a new form. In this way, the hardware complexity can be reduce to four addition and three multiplication operations.

There are two dividers each with 4 stage pipeline in the proposed design, one for the real part and the other for the imaginary part. The proposed SFBC decoder has a sequential and continuous output which is easy for any module to connect after it.

Fig. 3 shows the block diagram for the channel matrix operation. For the logic design of channel matrix, lots of multiplication and addition are required originally, and have to be simplified for low complexity. We found that $\overline{V}'_{pq}(n)x_q(n)$ is a fixed term in the compensation value calculation. If we separate the channel matrix, $\overline{V}'_{pq}(k) \times x_q(m)$ can be calculated first and a part of the matrix multiplication can be simplified into a vector multiplication. Moreover, for the proposed MIMO 4×4 system, the term

$$\sum_{n=0}^{p-1} \overline{V}'_{p1}(k) \times x_1(m), \tag{1}$$

can be combined before multiplying the ζ_n matrix.

However, $x_q(m)$ is the rebuild signal of the transmitted OFDM symbol which is a combination of mapped data signal and pilot.

Table I shows the complexity comparison for the original algorithm and the proposed hardware design, where Z denotes the ICI compensation tapes, N denotes the usage subcarrier number of one OFDM symbol, D is the data subcarrier number of an OFDM symbol, and p is the antenna number.

TABLE I
COMPLEXITY ANALYSIS

Design	Logic	Original	Simplification
Channel Mat.	**Mul.**	$4Z^2p^2$	0
	Add.	$2(Z-1)N(p^2-p)$	$(12p^2+54p+2Z)N$
SFBC Dec.	**Mul.**	$D10p$	$D2p$
	Add.	$D21p/2$	$D33p/2$
	Div.	$Dp/2$	$Dp/4$

B. The Proposed Uplink Transceiver Architecture

Fig. 4 illustrates the proposed transceiver block diagram[6]. In the transmitter, data and pilot subcarriers of different users are allocated orthogonally in subchannel according to IEEE 802.16e-2005 standard. In the receiver, four main functional blocks are included: FFT processor, memory buffer, ICI canceller and channel estimator. The detailed design can be found

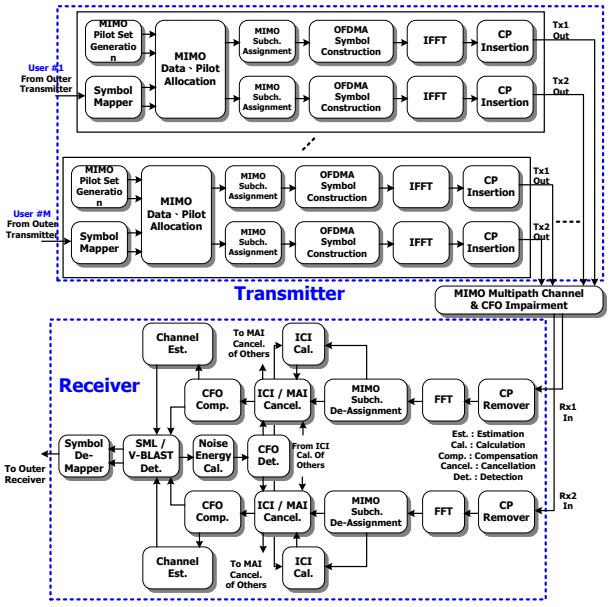

Fig. 4. Proposed 2x2 MIMO-OFDMA uplink baseband transceiver.

in [6].

C. I/O Control Unit

For the integration of the proposed uplink system on SoC platform. An I/O interface will be needed between AMBA bus [7] and the proposed uplink system. The hardware blocks of logic module is shown as Fig. 5. Follow the SoC integration methodology, the proposed transmitter/reciever will be an AHB device through AHB wrapper is shown as Fig. 5. There are two reasons to use the input controller: latency and data width. The latency between every bus transaction is 10 clock cycles and the input timing of the proposed receiver is 4 clock cycles. In the other hand, the AHB bus width is 32-bits which does not fit the input frame width is 44-bits of the proposed receiver.

III. SoC Integration and Verification

In the hardware emulation, the logic design is implemented with Verilog and synthesized by Quartus II tool. After the compilation of Quartus II, which includes the synthesis and automatic place and route flows, the FPGA bit stream will be downloaded to logic module on the SoC platform. For controlling the data flow on SoC platform, the proposed software design uses C code to implement and verify with ARM extended debugger (AXD) tool. The software program image is cross-compiled by compiler tool and downloaded into ARM CPU for SoC HW/SW verification.

A. Downlink System Integration

The proposed testbed hardware architecture is illustrated in Fig. 5. The verification flow and IP used is same as the uplink system. The hardware design is full compiled through Quartus II tool. After downloading the assembled bit stream to logic module. The FPGA emulation and software verification were proceeded simultaneously.

B. Uplink System Integration

The implementation and integration of uplink transceivers [6] is similar to Fig. 5.

IV. Baseband Transmission Model

For more complete baseband platform, a platform-to-platform transmission model is built. The proposed transmission model is based on the IEEE 802.16e-2005 uplink system. The proposed transmission model consists of SoC platform, FPGA board and conducting wires. Fig. 6 shows the photograph of the proposed model. The transmission model could be separated into two part in each hardware platform:

- The proposed uplink MIMO-OFDMA 2x2 transmitter, MAC unit and channel emulator exist in FPGA board.
- The proposed uplink MIMO-OFDMA 2x2 receiver, MAC unit, output controller and other hardware component exist in SoC platform which is illustrated in Sec. II.

The proposed transmission model hardware architecture is illustrated in Fig. 7. The proposed transmission model employs two platform to form the transmission environment.

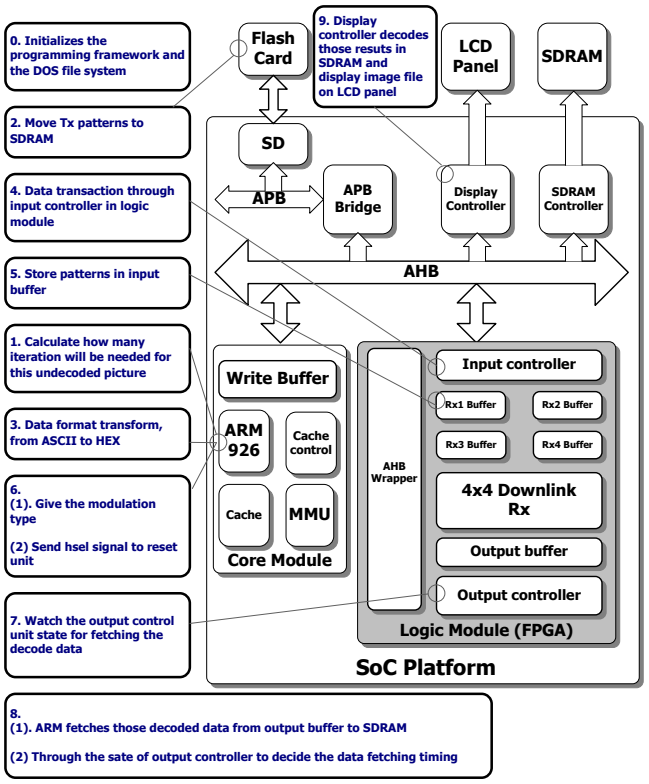

Fig. 5. HW/SW co-verification flow of downlink system.

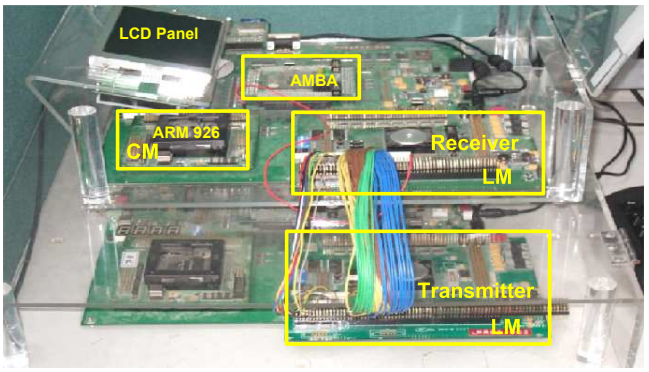

Fig. 6. Photograph of the proposed model.

A. Hardware Implementation

Hardware components in the FPGA board are the proposed uplink transmitter, MAC unit, data source and channel emulator. In the proposed transmission model, the figure file is introduced to be the transmission media. Those RGB 16bpp raw data will be stored in ROM of FPGA board. For the complete emulation of the baseband platform, a channel emulator is needed. The medium access control (MAC) unit is introduced to control the baseband signal transmission. MAC unit is controlled by ARM CPU on SoC platform to decide signal transmission timing. The MAC unit could be separate into two parts: receiver and transmitter.

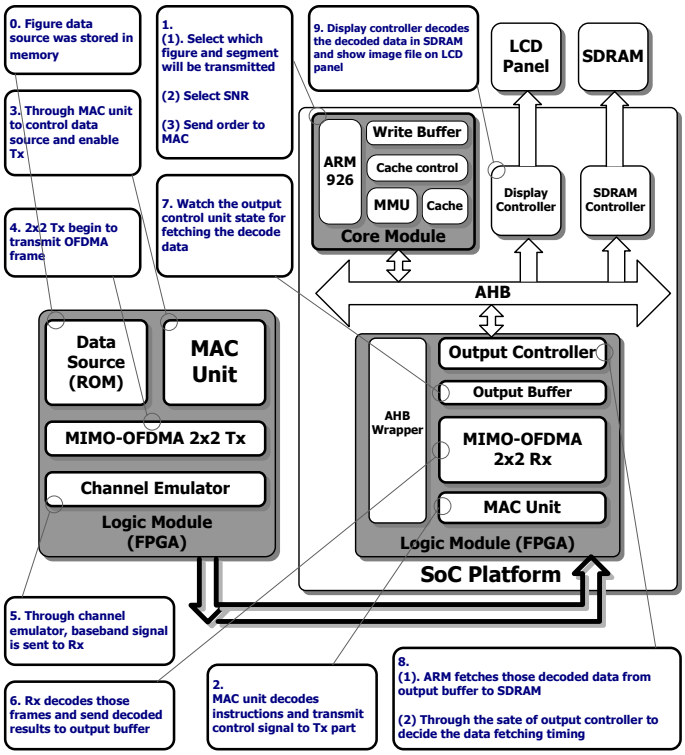

Fig. 7. HW/SW co-verification flow of platform-to-platform transmission.

B. HW/SW Co-verification

In the beginning, the figure data source will be programmed into ROM to accelerate speed of accessing. The transmission conditions are like: which figure, which segment of figure and SNR are selected in software programming. It could be flexible to select environment condition of emulation. After those conditions have been set, MAC unit of Rx part decodes instructions from ARM sent, then send control signals to Tx part. Meanwhile, the whole system is controlled via ARM CPU. After receiving baseband signal, MAC unit of Tx part enable the proposed transmitter and dominate data source input to transmitter. The proposed transmitter starts to generate OFDMA frame and send to channel emulator. The channel emulator generate MIMO effect and add noise on OFDMA frame, afterward these baseband signals is transmitted to receiver. After those frames was decoded by receiver, the decoded results will be moved to output buffer. Afterwards, ARM fetches those decoded data to SDRAM and via the display controller to show the image file on LCD panel. In the process of verification, designers can change their software design to verify the proposed system in different environment. Fig. 7 shows the HW/SW co-verification flow of the proposed model.

V. Performance Measurement of the Evaluation Platform

In this section, the emulation results of the proposed downlink system and baseband transmission model is presented.

A. Downlink System Emulation Results

The proposed platform is suitable uplink and downlink system of the 802.16e-2005 standard. It can be easily applied to downlink system by changing the I/O control unit of uplink system. The interface and software design between IP cores and proposed transceiver were mostly like the uplink system. The downlink system emulation results is shown as Fig. 8. Those results show the proposed downlink receiver in different mobility environment.

Fig. 8. Emulation results in high mobility (a) 300km/h (b) 200km/h.

B. Baseband Model Emulation Results

After the hardware emulation, the emulation results are shown as Fig. 9. The proposed platform is not only provided single platform integration, but also the baseband transmission model. The proposed model provided a flexible and fast verification flow. From this, designers can verify emulation results directly.

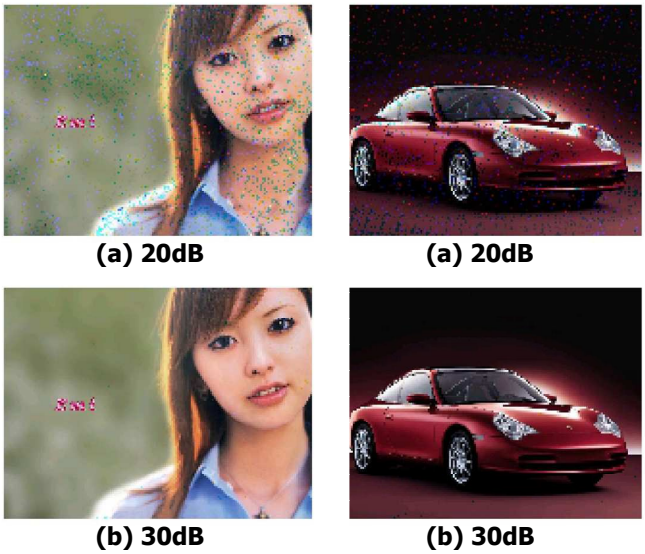

Fig. 9. Emulation results in (a) SNR 20dB (b) SNR 30dB.

C. Comparison

The comparison of the proposed platform and another WiMAX testbed is shown as Table II. Compare to another WiMAX testbed, the proposed platform could apply to uplink and downlink system. Furthermore, the proposed platform is integrated on SoC platform is a complete system design.

TABLE II
COMPARISON WITH ANOTHER WIMAX TESTBED.

	Proposed Testbed	M. Wenk [8]	Qing Wang [9]
Communication Type	Uplink/Downlink	-	Uplink/Downlink
FFT Size	1024	64	256
Throughput(Mbps)	16-QAM: 3.8	BPSK: 15 QPSK: 22 16-QAM: 25	-
Operation Frequency (MHz)	5	20	-
Verification Mechanism	HW/SW Co-verification	Matlab Measurements	Matlab Measurements
Modulation	QPSK 16-QAM 64-QAM	BPSK QPSK 16-QAM 64-QAM	BPSK QPSK 16-QAM
Implementation	SoC Integration	FPGA and RF module integration	SW Simulation and RF integration
MIMO Technique	2x2/4x4	4x4	2x2
Baseband Algorithms	ICI Cancellation Channel Estimation	-	Time Synchronization Channel Estimation Phase Correction

VI. CONCLUSION

The primary achievements in this paper are **flexible prototyping**, **fast verification**, **validate performance clearly** and **complete system design** as compared with previous solutions[1], [2], [3], [4].

- **Flexible prototyping:** In the begging of development, the proposed platform is integrated with uplink system. Through changing I/O control unit and software design, the proposed platform could apply to downlink system. It's a flexible prototyping for uplink and downlink system.
- **Fast verification:** Designers can use platform-based design approach as an effective strategy to cope with product complexity and time-to-market at all levels. Moreover, SoC design methodology will minimize verification uncertainties that greatly reduce design effort and risk. For the verification stage, designers can use the HW/SW co-verification strategy to debug hardware component, which will help designers identify more faster.
- **Validate performance clearly:** In this proposed platform, which is use the figure file to be the transmission media. Designers validate their design in BER/SNR waveforms traditionally. In the proposed platform, designer could verify the decoded results in various environment by LCD panel.
- **Complete system design:** The proposed platform consist of hardware design, software design and SoC platform. The hardware and software design have been synthesized and verified. The proposed platform provides a complete system design.

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