A Low Power Sensor Interface IC for Wearable Wireless Biomedical Devices

Xiaodan Zou
Dept of ECE
National University of Singapore
4 Engineering Drive 3
Singapore 117576
xiaodan@nus.edu.sg

Xiaoyuan Xu
Dept of ECE
National University of Singapore
4 Engineering Drive 3
Singapore 117576
elexxy@nus.edu.sg

Yong Lian
Dept of ECE
National University of Singapore
4 Engineering Drive 3
Singapore 117576
eleliany@nus.edu.sg

Yuanjin Zheng
Institute of Microelectronics
11 Science Park Road
Singapore Science Park II
Singapore 117685
yuanjin@ime.a-star.edu.sg

ABSTRACT
This paper presents a low power, low noise CMOS front-end IC for wearable biomedical sensor devices used in wireless body area network. The IC includes a rail-to-rail low noise amplifier (LNA), a unity gain buffer, and a 12-bit analog-to-digital converter (ADC), which is able to acquire biomedical signals in the range of few µV to 10 mV. The overall system operates under 1V supply voltage, provides 40dB midband gain with 2.4µVrms input referred noise integrated from 0.04Hz to 250Hz, and consumes 1.4µW when implemented in standard 0.35µm CMOS process. The low power is achieved through a newly introduced system architecture that significantly reduces the clock frequency of ADC compared to the design in [4].

Keywords
Biomedical circuits and systems, wireless biomedical device, biosignal acquisition unit.

1. INTRODUCTION
The converging of bioengineering, computers, communications, and nanotechnologies opens the door for integration of wireless communication channel, biomedical sensor devices, and signal processing unit into a single chip, which leads to the introduction of wearable wireless biomedical sensor devices. A collection of these wearable wireless biomedical sensor devices forms the base of a wireless body area network (WBAN). The WBAN not only provides health monitoring to hospital patients but also helps maintain the current state of health of the chronically ill patients and prevents their condition from worsening at home through the telemedicine. It is envisaged that the WBAN will revolutionize the hospital, homecare, and personal health systems and establish a prevention-oriented, consumer-driven model for health care.

A typical WBAN node includes one or more biomedical sensors, a low noise amplifier, an analog-to-digital converter, a digital signal processing unit or microcontroller, and a wireless communication channel. The development of WBAN devices is very challenging due to its small form factor and power constrains. The LNA should provide sufficient gain and deliver a reasonable good noise performance, especially in the low frequency ranging from DC to few hundred hertz. The ADC needs sufficient resolution to resolve the weak bio-signal. The signal processing unit must be well balanced between the processing capability and power dissipation. These requirements are difficult to satisfy due to the flicker noise of CMOS transistors in the low frequency band and tight power budget for the overall device. There are few attempts [1-4] that try to fulfill part of functions required by a WBAN device. One of the impressive solutions was proposed in [4] where a biosignal acquisition system contains a LNA and an 11-bit ADC consuming as low as 2.3µW. However, the conversion clock frequency used in [4] is around 20MHz for a 1KS/s ADC resulting in relative high power consumption. In this paper, a low power, low noise signal acquisition system is presented, which includes a LNA and a 12-bit ADC. The post layout simulation indicates the overall power consumption below 1.4 µW, a 40% reduction in power compared to [4].

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2. SYSTEM ARCHITECTURE
The signal acquisition system in [4] consists of a LNA followed by a successive approximation ADC. The narrowband LNA with less than 250Hz in bandwidth has to drive a large capacitor array in ADC resulting in long linear settling time. In order to achieve acceptable tracking error, the authors decrease the hold period to 1/500 of the sampling period. This leads to a high conversion clock frequency of up to 20MHz for a 1KS/s ADC which significantly increases the power consumption of the overall system. In order to reduce the clock frequency, we propose to insert a buffer between the LNA and ADC, which leads to a new system architecture, as shown in Figure 1. The buffer is designed to have a wide bandwidth and high slew rate to fulfill the charge/discharge requirements of the large capacitive load. By employing this architecture, the hold time is extended to almost 4/5 of the sampling period, which significantly reduces the conversion clock frequency. As a result, the power consumption of the comparator and oscillator in the proposed ADC are only 33% and 40% of those in [4], i.e. up to 700nW saving in power.

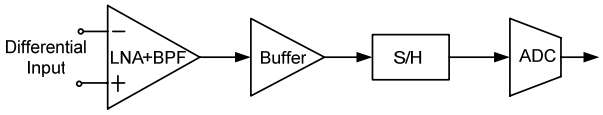

Figure 1. Front-end block diagram

3. CIRCUIT DESIGN AND SIMULATION

The LNA employs the structure proposed in [1]. It employs capacitive feedback and the midband gain is 40dB which is determined by the capacitance ratio. The DC rejection is achieved primarily through enhanced pseudoresistors, which eliminate the need for external capacitors, favoring a reasonable input impedance level. The LNA cutoff frequency at the high end is determined by the ratio of the unity gain frequency of the OTA and the midband gain of LNA. The low noise OTA in [4] is adopted as the first stage. Large size NMOS transistors are chosen as the input pair to achieve low input referred noise. The use of NMOS transistors instead of PMOS is a trade-off between supply voltage and noise performance.

A unity gain buffer is implemented after the LNA block in order to fulfill the linear settling time and slew rate requirement. It employs the similar feedback network as in [1] with the capacitance ratio set to 1. This ensures rail-to-rail input swing for the buffer. The bandwidth of the buffer is designed in the range of kHz. In order to achieve wide bandwidth with considerably low power consumption, an opamp with class AB output stage is chosen to generate a larger output current than the quiescent current [2].

A 12-bit ADC is implemented using the SAR architecture. The sample-and-hold function is realized by the bootstrapped analog switch and capacitor array. The bottom plates of the capacitors are toggled between high and low reference voltages by the SAR logic in order to implement the binary search algorithm, results being reflected on the common node of the array and collected by the comparator.

The overall front-end system has been implemented by standard 0.35µm CMOS technology with Vthp + Vthn = 1.15V. Figure 2 shows the post-layout simulation of LNA frequency response. The midband gain is 40dB. The input referred noise is 2.4µVrms integrated from 0.04Hz to 250Hz, as shown in Figure 3. A comparison of proposed front-end IC and [4] is summarized in Table 1.

4. CONCLUSIONS

We have presented a signal acquisition IC for wearable biomedical devices. It consists of a low power, low noise amplifier with bandpass function, a wide bandwidth and high slew rate buffer, and a 12-bit ADC. The insertion of the buffer greatly improves the system performance and plays a critical role in reducing power. The overall system consumes 1.4µW under 1V supply voltage and achieves 40dB midband gain with 2.4µVrms input referred noise.

5. ACKNOWLEDGEMENT

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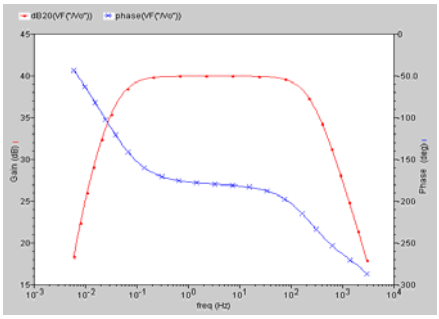

Figure 2. Frequency response of LNA

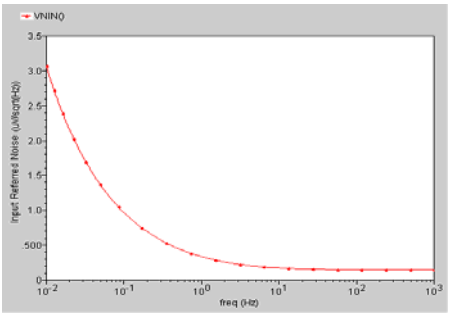

Figure 3. Input referred noise of LNA

Table 1. Comparison of the frond-end IC

Parameter	Design in [4] Measured	Proposed Simulated
Supply voltage	1V	1V
Current (LNA)	330nA	320nA
Midband gain	40.2dB	40dB
3dB Bandwidth	0.003Hz / 245Hz	0.04Hz / 250Hz
Input referred noise	2.7µVms (integrated from 0.05Hz to 245Hz)	2.4µVms (integrated from 0.04Hz to 250Hz)
LNA THD	0.053%	0.023%
CMRR	>60dB (1~250Hz)	>80dB (0~250Hz)
ADC resolution	11-bit	12-bit
ADC sampling rate	1 KS/s	1 KS/s
Total current	2.3µA	1.37µA