Intelligent Electrode Design for Long-Term ECG Monitoring at Home

Prototype design using FPAA and FPGA

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***Abstract*—A personal medical device supporting continuous bio-signals monitoring is presented. The novelty of this paper is to provide an intelligent electrode suitable for long-term ECG monitoring. The proposed intelligent electrode is composed of an ASIC chip and a micro pikes array established on a gauze plaster substrate. By comparing the signal quality, the patient's comfort and convenience, the proposed intelligent electrode could be an alternative to the traditional adhesive electrode. A prototype for the intelligent electrode is built up based on programmable FPAA and FPGA chips.**

Keywords-long-term; ECG monitoring; intelligent electrode; signal extraction; signal digitization; signal transmission; micro pikes; Delta-Sigma modulator; FPAA; FPGA

I. INTRODUCTION

Currently, many countries are suffering population aging problems and consequently facing the increasing costs in their healthcare systems, especially in the area of cardiac diseases. Progress has been made in extending healthcare into the home environment, since this service is more convenient and less expensive [1].

The work presented here is part of a research project aiming to develop a personal wearable medical device for home use. It is a battery operated device which can continuously monitor the user's physiological status including electrocardiograph (ECG) signals, motor activity, sleep patterns, and other health indicators.

The goal of this work is to develop an intelligent electrode, as illustrated in Fig. 1. The proposed intelligent electrode consists of a 20 × 10 mm^2 gauze plaster, a 2 × 2 mm^2 array of micro needles attached beneath, and a 1 × 1 mm^2 Application Specific Integrated Circuit (ASIC) embedded in the middle. The ASIC manufactured with standard CMOS technology features with ultra-low power consumption and small silicon size. Integrated inside a gauze plaster, this ASIC enables ECG signal extraction, digitization and transmission to be performed directly on the intelligent electrode, rather inside a bulky instrument or a portable device [2]. High quality ECG signal could be obtained by integrating a micro pikes array beneath the gauze plaster. Improved electrical contact between electrodes and patient's skin could be achieved by penetrating the dead skin cells with these micro pikes. Each pike is designed with a proper length that patients will not feel any discomfort during the placement of intelligent electrodes.

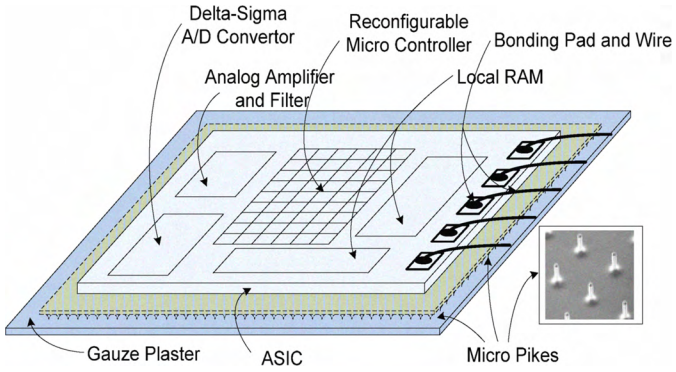

Figure 1. Proposed intelligent electrode composed of a gauze plaster, an ASIC and micro pikes.

A significant challenge addressed by this work is to guarantee that the expected ASIC functionalities could be successfully achieved, owing to the costly and time-consuming ASIC manufacture process. A prototype is built up based on two programmable chips to validate the ASIC functionalities before sending the design out for manufacture. One chip is Field Programmable Analog Array (FPAA) taking charge of on-chip analog circuit, and the other is Field Programmable Gate Array (FPGA) responsible for a reconfigurable micro controller.

In the following sections of this paper, the principle and methodology of prototype design for the intelligent electrode with a FPAA and a FPGA will be described in details.

II. ELECTRODES

The advantages and disadvantages of traditional adhesive electrodes are presented in this section. Accordingly, an intelligent electrode is proposed which could overcome the drawbacks of traditional adhesive electrodes [3].

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A. *Adhesive Ag/AgCl Electrodes*

The most commonly used ECG electrodes in the clinical field are pre-gelled and solid gel silver/silver chloride (Ag/AgCl) adhesive electrodes. These electrodes are simple, lightweight, reliable and cost effective. They provide relatively good signal quality. Due to the stable interface between electrode and electrolyte, very low artifacts are generated. Furthermore, no hygienic problem exists, since they are disposable after use.

However, adhesive electrodes have drawbacks when used in long term monitoring applications. Firstly, mechanical abrasion (skin pretreatment) together with the adhesive gel cause damages to the skin, such as irritations or allergic reactions, especially under long-term monitoring conditions. Secondly, the contact impedance between the electrode and the skin becomes unstable when gelled electrodes dry out. Electrode motion results in electrode contact interference which contributes to the signal noise. Moreover, a considerable number of cables are required to connect electrodes with a central device in most ECG monitoring applications. For example, 3 cables are necessary for a 3-lead ECG monitoring, up to 9 or 10 cables for a 12-lead ECG monitoring. These cables are very uncomfortable for the patient and often restrict the patient's mobility.

Due to the above limitations, the research on discovering alternatives to Ag/AgCl adhesive electrodes is necessary. Here, intelligent electrodes are proposed which could be practical for long term ECG monitoring.

B. *Intelligent Electrode*

As shown in Fig. 1, an ASIC chip works as the most important part of the intelligent electrode. A signal acquisition circuit is integrated on the chip. The analog signal from the patient's skin is firstly amplified and filtered in the analog front-end module, then digitized by a 14-bit Delta-Sigma A/D convertor at a sample rate of 1000 samples per second. The digitized ECG data are stored locally in an on-chip dual port RAM temporarily.

A reconfigurable micro controller is located in the center of the ASIC. An intelligent electrode could be configured either as a master-electrode or a slave-electrode. From the function point of view, the master-electrode takes charge of the whole ECG monitoring system and serially collects ECG data from each slave-electrode, while the slave-electrode carries out the tasks of ECG signal conditioning and digitization. Instead of multiple cables, a single active cable is used to connect all the intelligent electrodes together, over which ECG data and commands are transferred.

The detailed structure of the reconfigurable micro controller and the serial data communication principle of intelligent electrodes could be found from Ref. [4, 5].

Moreover, micro pike technique is adopted in this design to minimize the electrode contact noise which is a transient interference caused by loss of contact between the electrode and the patient skin. These 100-μm-long spikes are fabricated with micro electro mechanical systems (MEMS) technology. By penetrating the outer layer of the skin, more accurate bio-potential could be measured.

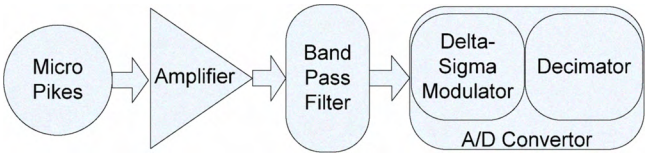

Figure 2. Signal conditioning process at analog front-end.

III. DELTA-SIGMA MODULATOR DESIGN WITH FPAA

A. *FPAA and ECG Signal*

FPAA is an analog device which can be dynamically reprogrammed to provide various analog circuits such as complex amplifiers and filters suitable for the processing requirements of bioelectric signals. In resemblance to FPGA, which contains a large number of configurable logic blocks and routing channels, FPAA chip typically contains a relatively small number of Configurable Analog Blocks (CABs). Generally, each CAB is composed of different types of analog components, such as operational amplifiers, switching capacitor arrays and programmable resistor arrays etc.

The ECG signal amplitude derived from ECG electrodes varies from 0.1 mV to 5 mV with a frequency ranging from 0.05 Hz to 100 Hz. The analog signal conditioning process at analog front-end is illustrated in Fig. 2. The analog signal from micro pikes is firstly fed into the on-chip amplifier and then to the band pass filter. Consequently, a 14-bit wide digital ECG vector is generated at the output port of the Delta-Sigma A/D convertor. As a key component in the front-end circuit, a second order Delta-Sigma modulator is implemented using AN221E04, a FPAA chip from Anadigm, Inc [6].

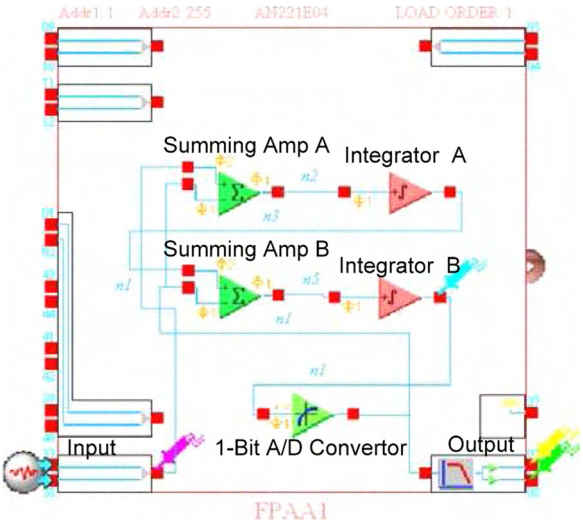

Figure 3. Second order Delta-Sigma modulator implimented with AN221E04.

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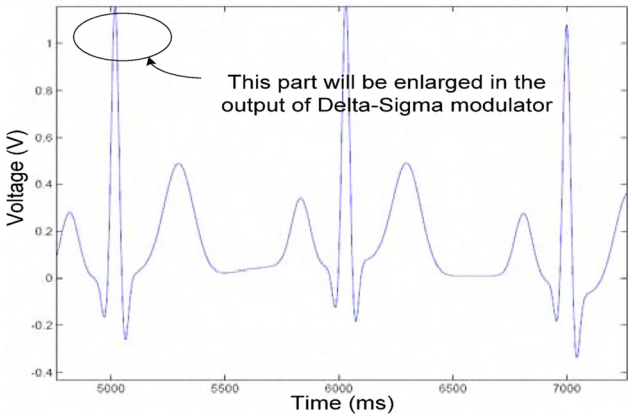

Figure 4. Input signal generated by ECGSYN.

B. *Delta-Sigma Modulator*

The structure of the second order Delta-Sigma modulator is shown in Fig. 3, consisting of two summing amplifiers, two integrators and a 1-bit A/D convertor. Four probes are placed on the key check points for waveform tracing.

The simulated ECG signal is generated by ECGSYN [7], a synthesized ECG waveform generator with a mean heart rate of 60 beats per minute, shown in Fig. 4. For a better output resolution, the amplitude of this ECG signal is amplified 3 times before feeding into the Delta-Sigma modulator.

The Delta-Sigma modulator over-samples the input signal and generates a high speed digital bit stream at its output port. The Decimator reconstructs the original signal from the over sampled bit stream without losing any information. The output of Integrator B is quantized by a 1-bit A/D convertor. This 1-bit A/D convertor also provides a recursive negative feed back to Summing amplifier A and B always in a direction to drive the integrator output towards 0. The average value of the clocked output tracks the input.

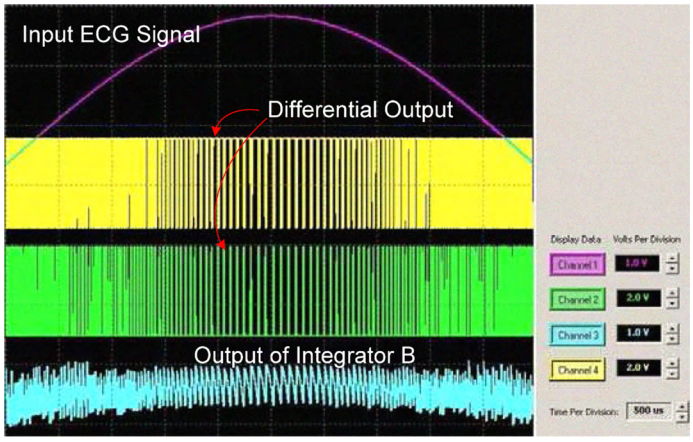

Figure 5. Waveforms at testing points.

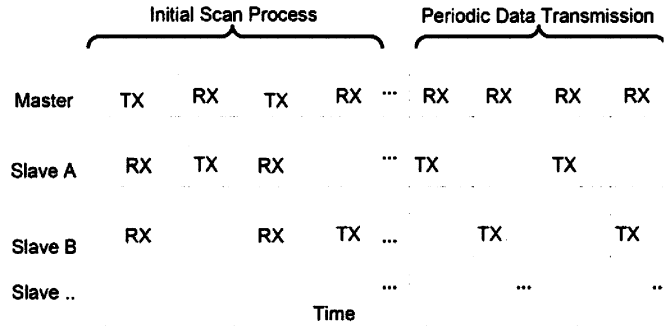

Figure 6. Time division scheme.

By stimulating the Delta-Sigma modulator with the ECG signal generated above, a differential output appears at its output, as shown in Fig. 5. When the input is close to a plus full scale, the output (the upper one of output signals in Fig. 5) is positive (logic 1) at most clock cycles. A similar statement holds for the case when the input signal is close to minus full scale, the output is negative (logic 0) at most clock cycles. In both cases, the average of the modulator output tracks the analog input. When the input is near zero, the value of the modulator output varies rapidly between logic 1 and logic 0 with approximately zero mean.

Due to the reprogrammable architecture of the FPAA chip, an optimized system performance could be achieved easily, simply by fine tuning different sets of circuit parameters, such as values of capacitors, resistors or amplifier gain. Hence, it greatly reduces the design time and is suitable for a fast prototype.

IV. Reconfigurable Micro-Controller Design with FPGA

An indispensible part of the proposed ASIC is the reconfigurable micro controller. Actually, this controller is combined by two controlling units: one provides functional modules for a master-electrode; the other one for a slave-electrode. By switching a specific pin to logic 1 or 0, an intelligent electrode could be configured either as a master-electrode or a slave-electrode.

Once the system powers up, the master-electrode starts an initial scan process. All slave-electrodes connected in the system will be scanned. During this process, the addresses of active slave-electrodes will be recorded. All broadcast commands and ECG data are transferred over a serial bus. ECG data are collected periodically, once every 0.5 second. During this process time division scheme is employed, as shown in Fig. 6.

A. *Test and Experiment*

The micro controller is implemented and verified on Xilinx FPGA boards. To test the desired functionalities of the micro controller, an experiment is designed, shown in Fig. 7. By switching the 'M/S' pin on or off, a Virtex II FPGA platform is configured as a master-electrode while a Spartan 3 FPGA platform is configured as a slave-electrode. Two FPGA

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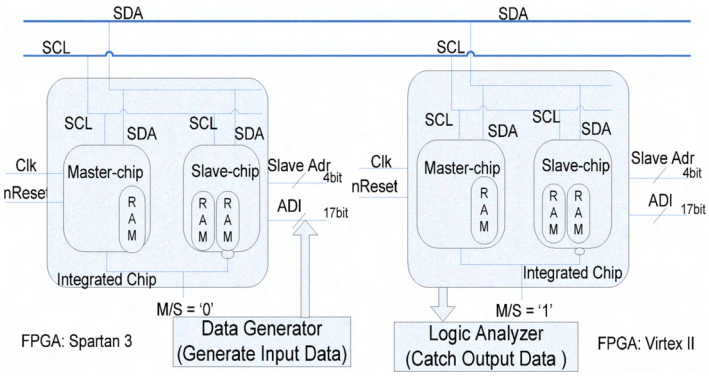

Figure 7. Functionalities test experiment.

platforms are connected by a two-wire serial bus. A Digital Data Generator is adopted as an external ECG data source providing the slave-electrode with various ECG data patterns via A/D interface. The master-electrode obtains the slave-electrode address by initial scan process and collects ECG data from the slave-electrode over the serial bus. The collected ECG data are output to a Logic Analyzer every 0.5 second. By comparing the data generated from the Data Generator with the data displayed on the Logic Analyzer, we can determine whether the desired functionalities are achieved or not.

The experimental result is shown in Fig. 8. A simple data sequence is created by the Data Generator with 1000 samples per second in a binary counting up manner. These data are firstly fed to the slave-electrode, stored in one of its local RAMs, later collected by the master-electrode via serial bus, then stored in its local RAM and finally sent out to the Logic Analyzer. By a comparison, it is found that the system initial scan process and the data transmission are successfully performed. The desired functional modules of the micro controller are achieved.

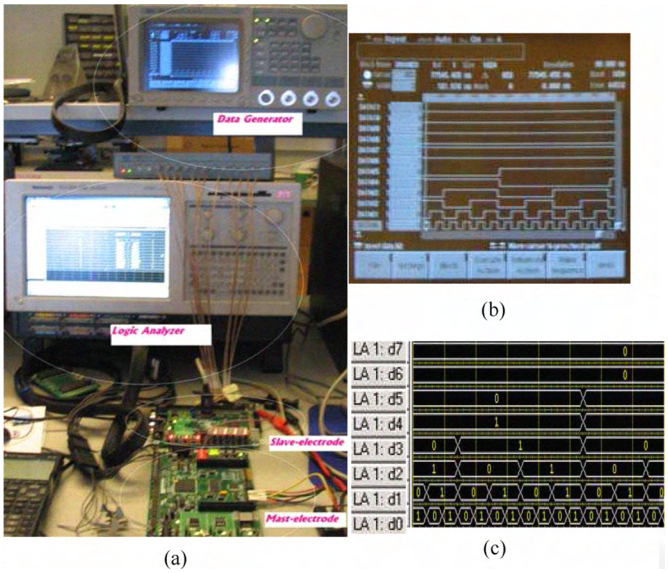

Figure 8. (a)Experiment setup. (b)Data sequence generated by the Data Generator. (c) Data collected by the Logic Analyzer.

V. Conclusion and Future Work

In this paper, the design of an intelligent electrode suitable for long term ECG monitoring is introduced. It is believed that the intelligent electrode could be an alternative to the existing adhesive Ag/AgCl electrodes. A prototype of the intelligent electrode is established based on FPAA and FPGA chips. Preliminary experiments with the aim of functionality verification for the Delta-Sigma modulator and the reconfigurable micro controller are successfully performed.

Future research will be conducted to manufacture the ASIC chip with a standard CMOS technology. In the near future, by expanding the ASIC functionality, the electroencephalograph (EEG) as well as other vital signals could be measured using intelligent electrodes in the meantime.

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