Asynchronous Links for Nanonets

(invited talk at Nanonets 2007)

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Nanometer technology facilitates integration of massive functionalities on a single chip, allowing designers to build multi-processor systems-on-chip. According to industrial estimates, at a very deep submicron level “total interconnect length can reach several meters, with interconnect delay as much as 90% of total path delay, and parasitics from interconnect becoming a dominant factor, which often causes timing issue in chip design” (from J. Lin’s Tutorial at ISSS 2003). There is a gradual realization that inter-block communication interfaces and links are becoming the first victims in the current standard system design methodology, which is based on global clocking. Clock skew becomes a problem for long interconnects, which limits the operating frequency in the channel. Thus maintaining high bandwidth under fully synchronous mode appears to be possible only by increasing the number of wires, wire width and inter-wire spacing (to reduce crosstalk), which is unrealistic because the metal layer area is at a premium on billion transistor chips. Globally clocked interconnect also suffers from the increased power and EMC problems. All this leads to thinking that future links are going to be increasingly self-timed. ITRS’05 predicts 4x increase in global asynchronous signalling by 2012 (8x by 2020).

This talk will focus on some key aspects involved in designing asynchronous links for on-chip communication, starting from the physical level, such as level, transition and pulse-based signalling, delay-insensitive data encoding, handshake protocols, control logic for synchronization buffers. It will then move to the link level circuits, such as FIFO buffers, address decoders and simple routers, paying particular attention to design of arbiters (tree, token-ring, priority etc.). Besides looking at purely asynchronous interfaces, the talk will also discuss async-to-sync links which are meant to be used at links between globally asynchronous channels and locally synchronous processing cores, in order to facilitate SoC desynchronization and construction of GALS systems. Here, problems with designing robust synchronizers will be addressed. The talk will also briefly look at successful examples of self-timed interconnects such as CHAIN, commercialised by Silistix.

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