Dual-Channel Binary-Countdown Medium Access Control in Wireless Network-on-Chip*

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ABSTRACT

Modern System-on-Chip design uses a rapidly increasing number of processing units for advanced information processing. When moving towards a billion-transistor era, ever increasing complexity and density of embedded components exacerbate on-chip communication, which serves as the fabric to integrate these heterogeneous components and provide a communication mechanism among them. In order to bridge the widening gap between on-chip communication needs and projected SoC performance, we propose a self-configurable multihop wireless micronetwork, dubbed Wireless Network-on-Chip, to serve as on-chip data and control communication infrastructure for next-generation billion-transistor SoCs. We present application-specific system architecture design of WNoC with the focus on radio frequency infrastructure. We propose a synchronized and distributed medium access control protocol for WNoC to resolve contentions between RF nodes. Binary countdown-based contention resolution and hidden terminal elimination schemes increase throughput and network utilization. Our simulation results show that DBC-MAC can achieve a promising performance in terms of throughput, latency, and network configuration.

Keywords

Wireless Network-on-Chip, RF Node Distribution, Medium Access Control, binary countdown

1. INTRODUCTION

Modern System-on-Chips pack a wide variety of functionalities (including microprocessors, memories, DSP, FPGA, peripherals and analog modules) on a single silicon. The on-chip communication architecture serves as the fabric to integrate these heterogeneous components, and provides a mechanism to exchange data and control information among them. Shrinking process technology nodes, increasing chip complexity, lower design cost and shorter time-to-market have multiplied the difficulty of designing SoCs. In particular, the increase in volume, density and complexity of embedded components rapidly results in the incompatibility between communication needs and projected SoC performance. Traditional broadcasting or shared-bus architecture have been shown unable to supply billion-transistor SoCs with both sufficient bandwidth and low latency under a stringent power consumption limitation. Network-on-Chip (NoC) [3, 6, 14] has thus been introduced as the interconnect network for multi-processor SoCs where the layered stack architecture design hides communication infrastructure details and facilitate component reuse.

As the interconnect design becomes one of the most challenging tasks, new materials such as copper/low-k dielectric are introduced at an unprecedented pace to meet the projected overall technology requirements. For the long term ($\leq 45nm$) however, material innovation with traditional scaling will no longer satisfy performance demands. Revolutionary interconnect innovation with radio frequency (RF)/wireless will deliver the solution to address future global routing needs and sustain performance improvement [5, 8, 12]. Recently, the technology advances such as microfabricated antenna, on-chip RF integration, and short-range RF communication, are making possible tiny, low-cost antennae, receivers and transmitters to be integrated and dispersed onto a single chip, namely the radio frequency (RF)/wireless interconnect technology. A significant amount of research has studied and demonstrated RF/wireless interconnection for intra-chip communication, such as wireless interconnect for intra-chip clock network to relieve the bottleneck for global signal distribution [10, 16], and intra-chip wireless connection for data communication over a distance of tens of millimeters [7, 11, 13].

Based on the recent development of RF/wireless interconnect technology, we propose a revolutionary on-chip communication infrastructure for gigascale heterogeneous MPSoCs, namely *wireless network on chip (WNoC)*. WNoC will provide higher bandwidth, higher flexibility, reconfigurable integration, and freed-up wiring when compared to NoC. Dispersed chip wide with tiny low-power low-cost radio frequency nodes equipped with wireless interface, the MPSoC can be viewed as a micronetwork of heterogeneous cores with quality-of-service requirement. The chip-based wireless radios will replace the wires to increase accessibility, to improve bandwidth utilization, and to eliminate delay and cross-talk noise in conventional wired interconnects. Envisioning a RF nodes-based on-chip wireless network where packetized data communication takes place. The cores access the network via transparent network interface, and their packets are forwarded to destination through a multi-hop routing path. The WNoC system architecture is designed in a way that decouples communication from computation, and a reconfigurable communication infrastructure is designed to address the heterogeneity of SoC. The layered protocol is specially designed to tackle distinct features of WNoC from conventional wireless networks and to simplify the hardware implementation.

Under a cross-layer design approach, WNoC data transmission

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protocol fulfils the functions of medium access control, network, and transport layers. We have designed an adaptive region-aided routing protocol at network layer [15] to achieve minimum path cost and to guarantee loop-free. The corresponding routing decision logic was implemented with high throughput, low latency and minimum circuit area overhead. When many RF nodes in WNoC communicate over the shared wireless medium, collisions may occur if multiple nearby RF nodes transmit data simultaneously. The system performance significantly degrades as the receiver in the collision domain (i.e., an area where all nodes are within each other's transmission range) cannot receive the data packet correctly. Thus a typical challenge for WNoC is to develop efficient medium access control (MAC) protocol for resolving channel contention and minimizing collision probability.

Wireless MAC protocols have been widely studied, which can be classified into two categories, distributed and centralized according to the type of network architecture, or contention-based and schedule-based according to channel access schemes. Wireless MAC protocols can be non-synchronized or synchronized. Non-synchronized protocols are largely contention-based, where collision nodes back off a random duration before retrying to access the channel [1]. Most synchronized protocols employ a centralized scheduler to make sure that nodes follow some particular schedules to achieve collision-free data transmission [4, 9]. Recently, synchronous and distributed MAC protocols have been introduced to achieve higher performance [17]. While MAC protocols have been extensively researched, a new type of network always stimulates the development of a set of new medium access control schemes. The MAC protocol must be customized for WNoC with two special requirements due to the uniqueness of WNoC. First, the MAC protocol should be implemented with very low hardware cost, which prohibits the use of any conventional MAC protocols. Second, it should achieve very low collision probability and packet delivery delay, in order to meet the quality of service requirement of various applications. In this work we propose a dual-channel binary countdown-based MAC protocol, namely DBC-MAC tailored for WNoC, aiming at making the implementation simple and efficient.

The rest of the paper is organized as follows. We design the RF infrastructure of WNoC in Sec. 2. The proposed DBC-MAC protocol is presented in Sec. 3. We evaluate the performance in Sec. 4. Finally we conclude the paper in Sec. 5.

2. RF INFRASTRUCTURE DESIGN

RF infrastructure design aims at determining WNoC communication architecture interpreted by a collection of RF nodes connected by wireless links. A WNoC consists of two basic components, the *Transparent Network Interface (TNI)* and the *Radio Frequency (RF) Node*. In order to decouple the designs of IP cores and WNoC, a Virtual Component Interface (VCI) [2] is adopted for TNI. With the VCI point-to-point transfer protocol, each core may deem itself directly connected to other heterogeneous cores, as if the WNoC is completely transparent. TNI diminishes the heterogeneity of the cores by transaction mapping and interacts with the network fabric for packet assembly, delivery, and disassembly. Each RF node has a radio-frequency interface (i.e., wireless transceiver) for (two-way) communication among IP cores. In a WNoC, the RF nodes are properly distributed according to various core functionality, non-uniform core size, and different traffic requirements between the cores. Such a flexible network architecture allows that several IP cores share one RF node and thus are grouped into a cluster. Each core may have their own TNI or share a TNI with other cores in the same cluster. With the multihop scheme, some nodes operate not only as a host but also as a router, forwarding data to other nodes in the network.

Although regular topologies such as grid-like structure simplifies network design, the heterogeneous computation requirements, communication workloads, and footprint sizes of the IP cores in different application domains call for the adoption of customized network topology, which involves two major interrelated problems, namely, *RF nodes placement* and *core clustering*. The cores need to be properly clustered in order to minimize the routing cost, to improve network efficiency, and to balance the communication workload accordingly. The cores in a cluster are hard-wired to an RF node via TNIs and share it for data/control communication. When cores are properly clustered, we need to find the minimum number of RF nodes to support communication needs of all cores among clusters and to determine their placement. In order to optimize the RF infrastructure, core clustering is incorporated into the process of RF node placement. We formulate the combined problem into *geometric disk covering* (GDC) [18] where a clustered wireless micronetwork can be abstracted as a set of disks, each centered at a RF node with a radius of R (i.e., the maximum RF node assistant distance within a cluster), that covers clusters of embedded IP cores in the chip plane. As GDC is strongly NP-complete [18], we propose a greedy set covering heuristic to solve it. The basic idea is that at each iteration, we choose the set or cluster that contains the largest number of uncovered IP cores while meeting the workload bound. Thus we obtain a total of N_d disjoint sets, each corresponding to a disk centered at a RF node by radius R. Based on this basic floorplanning, irregular WNoC topology is determined, taken into the consideration of the wireless transmission range, the network degree, and transmission routablity.

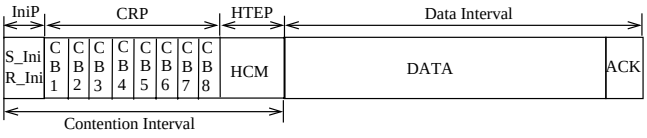
3. DBC-MAC PROTOCOL DEVELOPMENT

In this section, we propose a synchronized and distributed MAC protocol to resolve channel contention. The proposed MAC protocol involves a control channel and a data channel, such that the right to access the data channel is based on the negotiation in the control channel. Such negotiation is carried out by a binary countdown medium access mechanism. We name it as *dual-channel binary countdown medium access control protocol*, DBC-MAC.

To ensure collision-free transmission, DBC-MAC requires that the neighboring RF nodes start competing for the media at the same time. The WNoC system thus needs to be locally synchronized in a way that the asynchrony between the nodes several hops away will not affect or have trivial effect on the functionality of our DBC-MAC protocol. To reach local synchronization, each RF node will initiate and maintain a $syn-clk$ by receiving a $syn-control$ signal from neighboring RF nodes. DBC-MAC also requires a separate control channel and a data channel. The control channels consist of a set of control wires connecting between neighboring RF nodes (within the wireless transmission range) at very low wiring cost. Each RF node needs a set of n control wires for connection to its n neighbors (n is thus named as node degree). Each pair of control wires consists of one input ($Rx[i]$) wire and one output ($Tx[i]$) wire for handshaking between a RF node and its ith neighbor. With dual channels, the multiple access controlling is performed on these control wires while the data are transmitted through the network wirelessly, which involves several benefits. First, we may avoid expensive data synchronization. Only the control signals need to be synchronized. Second, the control logic can be simplified to bit operations and thus faster and simpler to implement. Third, since no control packets are sent through the wireless media, we may ensure 100% wireless channel utilization. Fourth, the DBC-MAC is interleaved in a way that the MAC protocol controlling of next packet can be launched at the same time with the data transmission of current packet.

The DBC-MAC protocol is based on synchronized time frames, which consist of two intervals: the contention interval and the data transmission interval as shown in Figure 1. With dual channels, the RF nodes that have data to sent compete the wireless media of next time frame through the wired control channel. While the

RF nodes that win the wireless channel competition in the previous frame transmit data packet through the wireless channel. Each RF node employs a three-step approach to access the shared wireless channel: initialization, contention resolution, hidden terminal elimination. Accordingly, the contention interval is divided into three periods. It starts with an initialization period (IniP). It is followed by the contention resolution period (CRP), that consists of a series of *k* contention slots used for binary countdown approach to resolve contention. The contention interval ends with a hidden terminal elimination period (HTEP). The operations of each period are described below.



IniP: Initialization Period
CRP: Contention Resolution Period
HTEP: Hidden Terminal Elimination Period

Figure 1: DBC-MAC frame format.

3.1 Initialization

Each RF node maintains a 2-bit status register $SR[1:0]$ which indicates one of four states of a node: TX, a transmitter where $SR[1:0]=(1,1)$; RX, a receiver where $SR[1:0]=(1,0)$; InA, node inactive where $SR[1:0]=(0,1)$; and SND, node state-not-determined where $SR[1:0]=(0,0)$. During the initialization period, any RF node that has data to send is set as a potential transmitter with $SR[1:0]=(1,1)$. All other nodes are initialized in the state of SND by setting $SR[1:0]=(0,0)$. Each node also contains a *n*-bit potential sender record register $PSR[n-1:0]$. If bit $PSR_i=1$, the *i*th neighbor is recorded as a potential sender of the node. A node may have multiple potential senders. The PSR registers are initialized in a way that each sender asserts the only one outgoing TX line connected to the receiver (determined by the routing decision logic) while negating the remaining TX lines. All nodes check their incoming RX lines and all their potential senders are recorded in PSR if the corresponding RX lines are asserted.

For example, 12 RF nodes forms a WNoC as shown in Figure 2(a). Two nodes are connected by a link in the graph if they are within the transmission range of each other. Assuming nodes 1, 3, 5, 7, 9 and 10 have data to send to nodes 7, 4, 8, 1, 6 and 8 respectively. Note that, some nodes compete the wireless channel with other nodes within the transmission range. For instance, node 1 only competes with node 7; node 3 competes with node 5; node 5 competes with nodes 3 and 7; and node 7 competes with nodes 1, 5 and 10. Initially all potential senders such as nodes 1, 3, 5, 7, 9 and 10 are in state of TX while all other nodes in state of SND. A node may change from one state to another according to the state diagram during the contention resolution period.

3.2 Channel Contention

In contention resolution period, all potential transmitters (in TX state) compete for the wireless medium by employing a binary countdown mechanism. All incoming RX lines of RF nodes in the collision domain are initiated to logic zero at the start of CRP. A potential transmitter, say X, generates a *k*-bit random number, i.e., $\{CB_i | 1 \le i \le k\}$. If CB_i=1, node X asserts all its outgoing TX lines $TX[n-1:0]=(1,...1)$ in contention slot CS_i. Otherwise, if CB_i=0, all TX lines are negated, $TX[n-1:0]=(0,...0)$. Each RF node checks all its incoming RX lines at each slot and changes its state according to the state diagram as illustrated in Figure 3. A sender in state TX may change its state or remains as a transmitter when one of the following events occur.

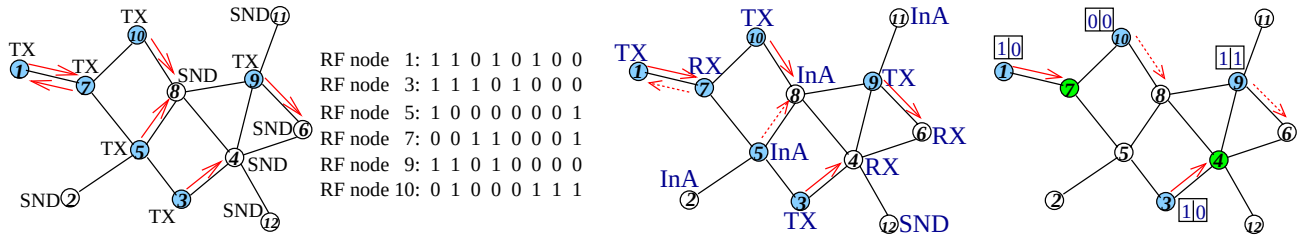
- **Case 1**: If all incoming lines of a potential sender are negated at slot CS_i while the contention bit $CB_i=1$, $Tx.win$ signal is asserted. The node wins the contention at the current slot and remains in TX state. The node will continue binary countdown if its neighbors' states have not been determined (in state of SND).
- **Case 2**: If any of the incoming lines of a potential sender asserts while the contention bit $CB_i=1$ or if all RX lines are negated while $CB_i=0$, $TX.cont$ signal is asserted, no one wins the wireless channel at slot CS_i, thus the contention continues. The node remains as a potential sender (in TX state).
- **Case 3**: If any of the incoming lines of a intent sender asserts while the contention bit $CB_i=0$, the node loses contention in slot CS_i and asserts its $Tx.lose$ signal accordingly. This node gives up its attempt of gaining access to the wireless channel in this frame. The node needs to be further checked if it is a receiver of its neighboring senders. There are three possible state transformations. If only one incoming line is asserted, we compute bitwise AND of $RX[n-1:0]$ and $PSR[n-1:0]$, i.e., $Tx.match$. If $Tx.match$=0, the node is not a receiver of the sender who asserts the RX line and its state is transformed from TX to InA. Otherwise, if $Tx.match$ does not equal to zero, the node is a receiver and its state is transformed to RX. In consequence, its sender is identified by updating its potential sender register $PSR=Tx.match$. If more than one incoming lines assert, the node cannot determine its next state and transfer its state to SND. The node will continue listening to the control channel to determine its state.

In the meantime, the nodes in state SND check their incoming RX lines in each contention slot and determine their state accordingly. If only one incoming line is asserted at contention slot CS_i for node X, a neighboring sender wins the contention. Node X performs bitwise AND of $RX[n-1:0]$ and $PSR[n-1:0]$, i.e., $Tx.match$. Node X is a receiver of the winner if $Tx.match$ is not equal to zero and changes its state from SND to RX. Its sender is identified consequently by updating its potential sender register $PSR=Tx.match$. Otherwise it transforms to state of InA. If more than one incoming RX lines assert, we will compute $Tx.match$ as well. If $Tx.match$=0, node X is not a receiver of any neighboring senders who assert the node's RX lines and its state is transferred from SND to InA. In other words, other neighboring senders have a larger random contention number than node X's potential senders. If $Tx.match$ does not equal to zero, we cannot determine if any of its potential senders wins the contention or not, thus node X remains in state SND and continue listening to the channel.

As illustrated in Figure 2(b), the contention is resolved for the example in Figure 2(a) with the random contention numbers generated for the senders 1, 3, 5, 7, 9 and 10. After the first contention slot CS_1, both nodes 1 and 9 win the contention. While node 7 loses contention and changes to SND. Node 6 identifies itself as the receiver of node 9. Nodes 2 and 8 change their states from SND to InA. Then node 5 gives up and changes to InA while nodes 3 and 10 win the contention in slot CS_2. Node 4 is identified as a receiver of node 3 in slot CS_3 while node 7 changes its state to RX in slot CS_4. Finally, among all potential senders, nodes 1, 3, 9, and 10 are the winners and nodes 5 and 7 lose contention and mark themselves as inactive and receiver respectively. Nodes 4, 6 and 7 are identified as receivers of their potential senders.

3.3 Hidden Terminal Elimination

After contention resolution period, only one potential sender in a collision domain can win if distinct random contention numbers are generated. However, the "hidden terminal" problem has not been addressed yet. For example, as senders 1 and 10 in Figure 2(b) are not within the transmission range of each other, they cannot receive the contention signals from each other. Both of them consider



(a) An example of node contention. (b) Contention resolution. (c) Hidden terminal elimination.

Figure 2: Illustration of DBC-MAC protocol.

themselves as the winner after *CRP*. A "hidden terminal" scenario results when node 10 attempts to transmit data to node 8 while node 1 is transmitting to node 7. similarly, nodes 3 and 9 will also encounter a "hidden terminal" problem. We can efficiently resolve the "hidden terminal" problem by sending hidden terminal clear messages (HCM) in the hidden station elimination period.

At beginning, all incoming lines of any RF nodes have been initialized to logic zero. The HTE period contains two slots and each sender maintains a two-bit hidden terminal clear register $HTCR[1:0]$. In the first slot, all nodes marked as receiver assert the one outgoing TX line connected to their sender as recorded in *PSR* register. All senders check their incoming RX lines by performing logic OR of $RX[n-1:0]$, i.e., $HTCR[1]$. In the next slot, the receivers assert all their outgoing TX lines except that the one connected to their sender is negated. Again, the senders compute $HTCR[0]$ by performing logic OR of $RX[n-1:0]$. Only the sender with $HTCR[1:0] = (1,0)$ can transmit data in the following data transmission interval. Otherwise, the node considers itself as a hidden terminal and gives up its attempt to access the wireless channel in this frame. For instance, after HTE period, nodes 9 and 10 identify themselves as hidden terminals as shown in Figure 2(c). Finally, nodes 1 and 3 will transmit data simultaneously in the data transmission interval.

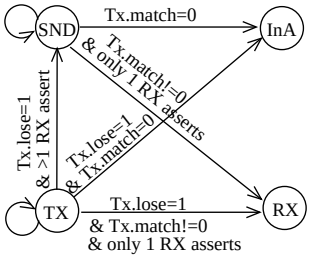


Figure 3: State diagram for the contention interval.

4. PERFORMANCE EVALUATION

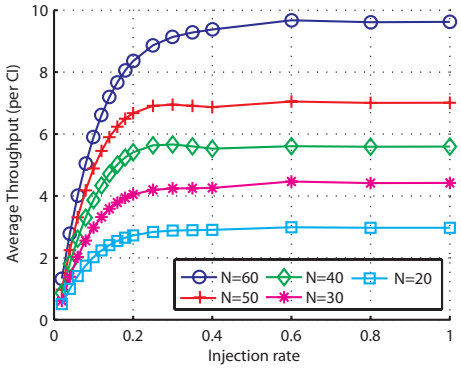
In order to evaluate the performance of proposed DBC-MAC protocol, we run extensive simulations. The SoC models are randomly generated with IP core placement. The WNoC topologies are determined by applying disk covering for core clustering and RF nodes placement. The routing decision at each node is determined by running the region-aided routing protocol as we proposed in [15]. Each RF node is associated with a random traffic generator that uniformly distributes traffic patterns. The number of packets generated per traffic pattern distribution is defined as the *injection rate*. The trade-off between architecture design and network concurrency should be well studied with the consideration of various systems parameters, such as network density (in terms of network degree), the SoC scale (in terms of number of IP cores in the SoC) and network scale (in terms of number of RF nodes in the WNoC). The performance of DBC-MAC protocol is evaluated in terms of network throughput and packet latency. The *network throughput* is defined as the average number of packets transmitted successfully over the network in one time frame. The *packet latency* is defined as the average number of time frames a packet takes to be sent out successfully from the time that it is ready for transmission.

Figure 4 illustrates the network throughput and packet latency vary over the injection rate when the number of RF cores (N) changes from 20 to 60. The network topologies are determined with the average network degree around 3.8. Thus the throughput becomes saturated from injection rate of 0.4 while the throughput increases when the injection rate increases. As we can see from Figure 4(a), the network throughput increases with the increase in network scale. With the same network density, the concurrency of data transmission increases linearly with the network scale. The packet latency is more affected by the network degree rather than the SoC scale and network scale. As illustrated in Figure 4(b), we observe slight differences of packet latency among various network scale. The distribution of network degree will also affect the latency. We define the derivation of any node degree from the average network degree as *degree derivation*. For a particular network, the higher variation in degree derivation tends to result in lower latency. For example, the two WNoC with 20 and 60 RF nodes respectively have the same network degree. As the one with 60 nodes has more diverse degree distribution, which means much smaller contention domains, the latency becomes slightly smaller that the WNoC with 20 nodes.

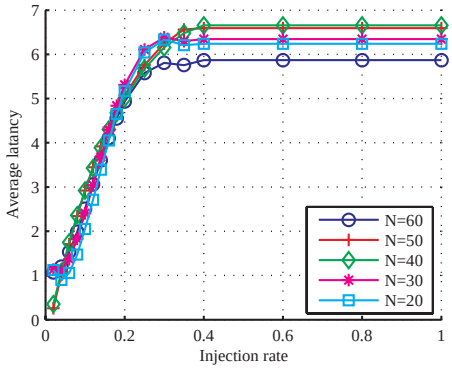
We further evaluate the performance by observing how the throughput and latency vary with the network degree for various network scales with the number of RF nodes changing from 21 to 63. The network degree conveys the information how we design the WNoC communication architecture during RF nodes placement and core clustering and how we determine the topology afterwards by varying the wireless transmission range. In order to illustrate the effect of RF infrastructure design on the network degree, we apply 5 different RF node assistant distances for a same SoC model. Then for each RF nodes distribution, we apply 5 different wireless transmission ranges starting from the minimum required transmission range (to ensure network connectivity). As we can see from Figure 5(a), the throughput declines with the increase in network degree at certain network scale due to the increased contention. The latency is almost linearly increased when the network degree increases as shown in Figure 5(b). Once again, we can see that the network scale only has slight effect on the latency. At any particular network degree, different network scales have pretty much similar latency. It is because the packet latency is mainly determined by the number of nodes in the same contention domain. Thus, similar latency results for different networks with the same network degree.

5. CONCLUSION

In this paper, we have explored an revolutionary wireless communication infrastructure to meet the computation requirements of heterogeneous gigascale SoCs, dubbed wireless network on chip (WNoC). A reconfigurable communication infrastructure has been designed to address the heterogeneity of gigascale MPSoCs. The layered protocol stack has been specially developed to tackle distinct features of WNoC and to simplify hardware implementation.

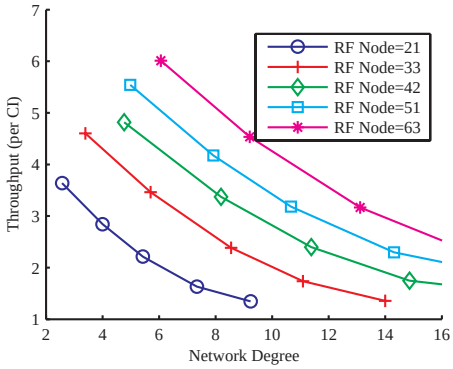


(a) Throughput vs. Injection Rate.

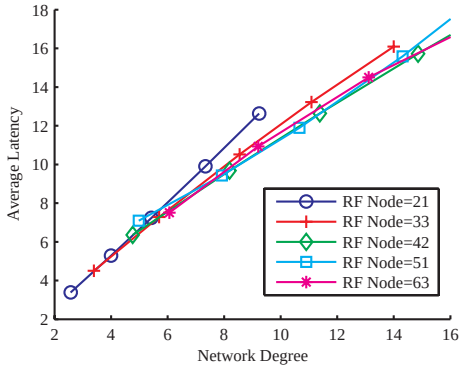


(b) Latency vs. Injection Rate.

Figure 4: Performance evaluation on throughout and latency changing with injection rate.



(a) Throughput vs. Network Degree.



(b) Latency vs. Network Degree.

Figure 5: Performance evaluation on throughout and latency changing with network degree.

We have focused on the design of a synchronized and distributed MAC protocol, namely DBC-MAC, that ensures 100% collision freedom while having the features of high-efficiency, simplicity, robustness, fairness, and quality-of-service capability.

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