Analysis and design of a WLAN OFDM transmitter with digital filters*

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ABSTRACT

This paper introduces a study and an implementation of filters in the digital part of an Orthogonal Frequency Division Multiplexing (OFDM) based transmitter. An efficient computational technique is presented for design with interpolation filters and discusses the corresponding VLSI architecture issues. By exploiting the redundancy into the cyclic prefix part of the OFDM symbol, the computational load of the transmitter is reduced by approximately 20% for the IEEE 802.11 WLAN standard.

Keywords

OFDM, WLAN, digital filters, VLSI architecture

1. INTRODUCTION

The current increase of demand for wireless communications applications, dictates a necessity for high-speed and spectral-efficient communications over wireless highly dispersive channels. Orthogonal Frequency Division Multiplexing (OFDM) has been selected as an efficient solution for high-speed digital wireless communications and is employed in current wireless communication standards, such as IEEE 802.11b in the 5Ghz band and 802.11g in the 2.4Ghz band, for wireless LANs, DVB for digital terrestrial TV broadcasting, WiMax for wireless MANs, 802.15 for wireless PANs *etc.*

In the 802.11 WLAN standard [2] the baseband signal is generated by using the IFFT, then a guard interval (also called a cyclic-prefix-CP) is added to make the system robust to multipath. The IFFT modulation produces a spectra of overlapping subcarriers, where each subcarrier is orthogonal to all other subcarriers. Respectively, the transmitted data are demodulated by an FFT in the receiver.

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In this paper, the study and implementation of filters in the digital part of an OFDM transmitter is presented. We investigate the digital filters that need to be applied at the digital part of the transmitter and propose an architecture where the filtered cyclic prefix part is not explicitly computed; instead it is constructed from the filtering of the useful OFDM symbol part. In this way the proposed algorithm, avoids the filtering of the total OFDM symbol, thus significantly reducing the number of multiplications needed by approximately 20%, for the case of a 64-point IFFT with cyclic prefix of one fourth of the OFDM symbol.

In previous work upsampling with interpolation filters has been discussed. A technique called circular time domain interpolation is applied where the 64-point IFFT result is both pre- and post- extended and then upsampled and filtered requiring additional computations [6]. Construction of the CP after filtering has already been presented in [4]. It is based on a combination of a radix-4 Multipath-Delay Commutator FFT architecture [5] with 4 parallel filters. In this paper we propose an architecture which outperform the previous designs in terms of area, number of computations, and utilization.

The remainder of the paper is organized as follows: In Section 2, a brief overview of the OFDM transmitter is and the analysis for the required digital filters is presented. Section 3 describes the proposed architecture. Results of implementation are discussed in Section 4 and conclusions are given in Section 5.

2. DIGITAL FILTERING IN OFDM TRANSMITTERS

A brief description of the organization of an OFDM transmitter [8], follows. The binary input data are encoded by a forward error correction scheme. The encoded data are subsequently interleaved and mapped onto QAM values. After the pilot tones are inserted, the IFFT modulation is performed to produce the useful OFDM symbol part.

The subcarrier orthogonality in OFDM is retained, when the signal is transmitted over a non-dispersive channel. To deal with the time dispersion, a guard interval is introduced between successive OFDM symbols. In most cases, the guard interval is a cyclic repetition of a number of the last samples of the IFFT output, pre-pended to the symbol part, called the cyclic prefix (CP). Due to bandwidth restrictions the CP is usually limited to less then one quarter of the useful OFDM symbol part. The OFDM symbol, after filtering, is sent to the Digital-to-Analog converter and passes on to the RF part of the modem.

2.1 Analog part of an OFDM system

The baseband complex OFDM signal from the digital part of the transmitter is transmitted using carrier f_c and is given by

$$r_{(RF)}(t) = Re\{r(t)\exp(j2\pi f_c t)\} \qquad (1)$$

where $Re(.)$ represents the real part of the complex variable.

The spectrum of the transmitted signal must be compliant with the specifications that are given by the 802.11 standard [2] and are shown in Fig. 1

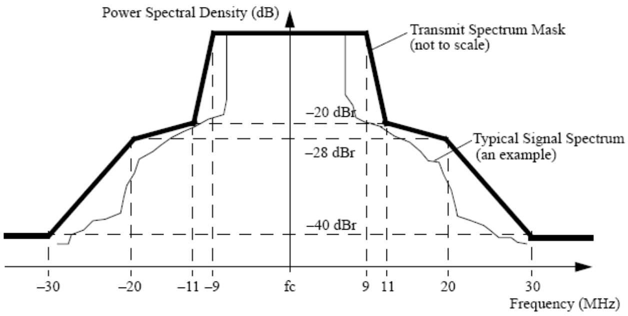

Figure 1: Spectrum of the transmitted signal as defined from the 802.11a standard

According to the standard specifications the number of sub-carriers should be $N = 64$. If a N-point IFFT is used, bandwidth is pretty narrow and the low pass reconstruction filter applied at the receivers end is characterized by very sudden transitions between passband and stopband frequency areas, which increases implementation complexity of the filter. For this reason and to avoid signal aliasing, the sub-carriers produced by the IFFT procedure should be upsampled. This can be achieved by using a double-in-size IFFT, but this enlarges the required area, requires faster D-A converters, and does not achieve reduction of complexity in the analog filter. Thus, there are advantages in the use of interpolation filters after the IFFT [3].

Fig. 2 the block diagram of an OFDM transmitter with interpolation filters is given:

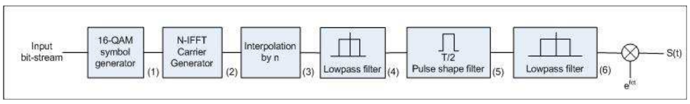

Figure 2: Block diagram of an OFDM transmitter with upsampled subcarriers.

2.2 Selection of the interpolation filter

In order to determine the optimal interpolation filter, simulations were performed. We compared the performance of the system in terms of BER and Peak-to-average power ratio (PAPR) to compare filters for different upsampling factors, namely by 2, 4 and 8. The filters examined were FIR, Chebyshev-I, Butterworth and Elliptic, the length of which differ depending on the upsampling factor.

The simulations include comparison between a system with a double-size IFFT ($N = 128$) and a structure with 64-point IFFT and interpolation filters.

From the simulation results it is concluded that the minimum BER is accomplished by applying upsampling by 2. Additionally minimum PAPR is accomplished for FIR and Butterworth filters with upsampling factor 2 and Chebyshev and Elliptic filters for upsampling factor 4. For each of the above groups of filters we ran simulations to determine the optimal system performance in terms of BER and PAPR respectively.

The simulation results are shown in the figures below. In Fig. 3 the results of measuring the PAPR for the two groups of filters are shown, while in Fig. 4 a comparison in terms of BER of the group of interpolation filters with upsampling factor 2 is shown and in Fig. 5 a comparison in terms of BER of the group of interpolation filters with lowest PAPR is shown.

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-----------------------------------------------------------
                MINIMUM BER RESULTS
-----------------------------------------------------------
BEFORE AND AFTER APPLYING THE INTERPOLATION FILTER

PAPR 2-IFFT                                      7.457054
PAPR 2-FIR(15) INTERPOLATION           6.693758-7.503788
PAPR 2-BUTTERWORTH(17) INTERPOLATION   6.693758-7.466733
PAPR 2-CHEBYSHEV(8) INTERPOLATION      6.693758-8.214316
PAPR 2-ELLIPTIC(5) INTERPOLATION       6.693758-8.285159
-----------------------------------------------------------
                MINIMUM PAPR RESULTS
-----------------------------------------------------------
BEFORE AND AFTER APPLYING THE INTERPOLATION FILTER

PAPR 2-IFFT                                      7.637050
PAPR 2-FIR(15) INTERPOLATION           6.889766-7.683525
PAPR 2-BUTTERWORTH(17) INTERPOLATION   6.889766-7.680486
PAPR 4-CHEBYSHEV(8) INTERPOLATION      6.889766-8.391072
PAPR 4-ELLIPTIC(5) INTERPOLATION       6.889766-8.524840
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Figure 3: Comparison of PAPR for the selected interpolation filters

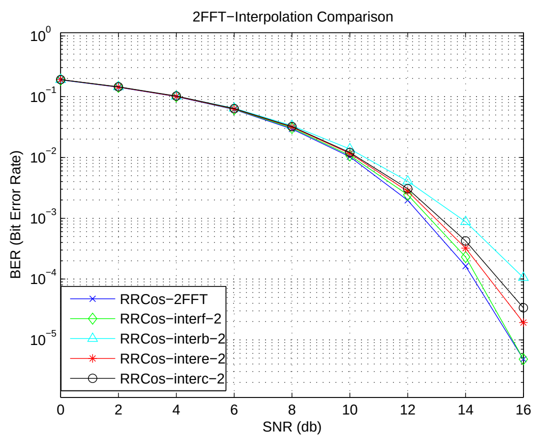

Figure 4: Comparison of BER performance of the iterpolation filters with minimum BER

From the simulation results it can be concluded that lowest BER for the first group of filters is given by a FIR interpolation filter with upsampling factor 2, while in the second group of filters with the lowest PAPR, the Elliptic filter that upsamples by 4 presents the lowest BER but also the highest PAPR (in comparison with the other filters in its group). In contrast, satisfactory results are given by the Butterworth-2 filter in terms of BER and PAPR.

If the selection factor for the interpolation filter is BER

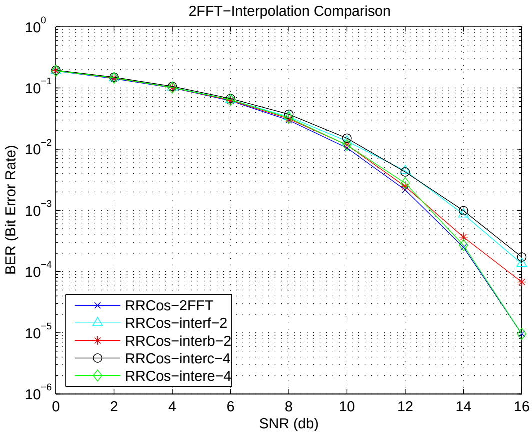

Figure 5: Comparison of BER performance of the iterpolation filters with minimum PAPR

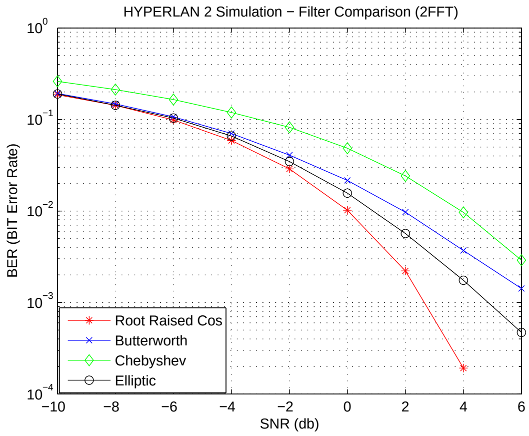

Figure 7: Comparison of low pass filters in terms of BER

performance then the FIR filter with upsampling factor 2 is the most suitable for implementation. FIR filters are very simple and flexible to implement, while the main advantage is the phase linearity, which is essential for an OFDM system in order to prevent PAPR increase (all circuits between modulator and demodulator have to produce as much as possible linear phase [1]). Concluding the analysis the FIR interpolation filter with upsampling ratio 2 is chosen for implementation.

2.3 Selection of the low-pass filter

In this section we determine the optimal digital low pass filter for the implementation. We examine four basic digital low-pass filters Butterworth, Chebyshev I, Elliptical and Root Raised Cosine. The selection of their characteristics (order, cutoff frequency, peak to peak ripple, roll off factor) has been done based on the required spectral mask of Fig. 1.

In Fig. 6 and Fig. 7 comparison of the four low pass filters applied to an upsampled signal of a double-sized IFFT in terms of PAPR and BER respectively is presented.

BEFORE AND AFTER APPLYING THE LOWPASS FILTER	
PAPR Root Raised Cosine(121) 2-IFFT	7.743857-8.458349
PAPR BUTTERWORTH(6) 2-IFFT	7.743857-8.273509
PAPR CHEBYSHEV(4) 2-IFFT	7.743857-8.790591
PAPR ELLIPTIC(3) 2-IFFT	7.743857-8.248007

Figure 6: Comparison of low pass filters in terms of PAPR

Comparing the above simulation results, the optimal low-pass filter with the minimum BER is the Root Raised Cosine(RRC). Considering though the length of the filter which is 121 taps,it is unsuitable for implementation, especially on FPGA where the available resources are limited. Overall the Elliptic filter is more suitable as it presents satisfactory results in BER performance, introduces the lowest PAPR and is small in size-only 3 taps.

To conclude from the analysis and simulation results above for an OFDM system based on the 802.11 specifications with 16-QAM modulation and coding rate $3/4$, is consisted of the 64-point IFFT block and an FIR interpolation filter with 15-taps. Finally the produced oversampled signal, passes through an Elliptic low-pass filter with 3 taps, and then is sent to the DAC.

3. THE PROPOSED ARCHITECTURE

In this paper, an architecture is proposed to construct the final OFDM symbol. This scheme differs from the straightforward technique, regarding the creation of the cyclic prefix part, as the extension by $N/4$ of the input data is not necessary. In contrary, the input data sequence remains the same and the convolution of the first $N/4$ samples is used to compute the cyclic suffix needed to construct the final OFDM symbol. The method used to compute the convolution with the FIR filter is based on the *overlap-add* method ([7]), in which the input sequence is divided in sub-blocks and each sub-block is convolved with the filter coefficients. The final filtered output is produced by adding the corresponding appropriate output samples.

The data coming from the IFFT output are in normal order: $x(0), x(1), \ldots, x(63)$

To apply the upsampling filter, zeros are interpolated between the samples.

As defined in the standard, the $N/4$ first samples of that sequence is used to calculate the cyclic suffix. Thus, using the overlap-add method, the input sequence $x(n)$ can be represented as $x(n) = \sum_{k=0}^{1} x_k(n)$, where

$$x_0(n) = \begin{cases} x(n), & 0 \leq n \leq N/4 - 1 \\ 0, & \text{otherwise} \end{cases},$$

$$x_1(n) = \begin{cases} x(n), & N/4 - 1 \leq n \leq N - 1 \\ 0, & \text{otherwise} \end{cases}, \quad (2)$$

The linear convolution $y(n)$ of the sequence $x(n)$ is then $y(n) = x(n) * h(n) = (\sum_{k=0}^{1} x_k(n)) * h(n) = x_0(n) * h(n) + x_1(n) * h(n)$

If the impulse response of the filter is P samples and the input sequence is N samples (in this case N=128), then the convolution output will be $N + P - 1$. Thus there is a region of $P - 1$ samples over which the first convolution overlaps with the second convolution and the corresponding appropriate output samples must be added resulting in

$y(n),\quad n = 0...N+P-1$. The convolution $y_0(n)$ of the first sequence $x_0(n)$ is actually the convolution of the cyclic suffix and may be used to construct the filtered OFDM symbol y_{OFDM}, by adding the appropriate overlapping samples of the sequence generated by $y(n)$.

The construction of the filtered OFDM symbol y_{OFDM} is given by

$$y_{\mathrm{OFDM}}(n) = \begin{cases} y(n), & 0 \leq n \leq N-1 \\ y(n-N) + y_0(n-N), & N \leq n \leq P+N-1 \\ y_0(n-N), & {\scriptstyle P+N \leq n \leq P+(N+N/4)-1} \end{cases} \tag{3}$$

The computational complexity of the above method is PN multiplications and $(N+2)(P-1)$ additions.

In the straightforward approach, the input sequence to the filter is extended by $N/4$ and the computational load is $P(N+N/4)$ multiplications and $(P-1)(N+N/4)$ additions.

Thus, the gain in computational complexity is $\frac{P(N+N/4)-PN}{P(N+N/4)} = 20\%$, for multiplications, and $\frac{(P-1)(N+N/4)-(N+2)(P-1)}{(P-1)(N+N/4)} = \frac{N-8}{5N}$ for additions. For $N = 128$, in this implementation, the gain for additions is also 20%.

Fig. 8 shows the proposed architecture for implementing the above method.

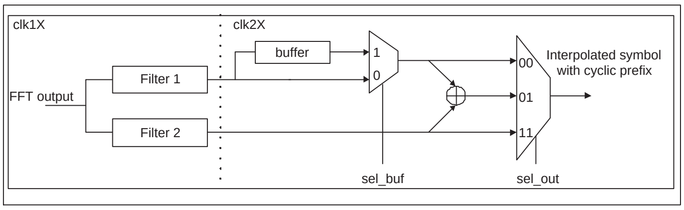

Figure 8: Architecture for computing a filtered OFDM symbol

The output data from the IFFT block, appear in normal order, are sampled by clock $clk1X$, and are fed as inputs to Filters 1 and 2 of Fig 8. In contrary, the filter outputs are sampled by clock $clk2X$ that operates in double frequency of $clk1X$. All references to clock cycles from this point forward are in correspondence to $clk2X$. The control signals `sel_buf` and `sel_out` determine the input and output of the adder, respectively. Filter 1 is used to compute the convolution of sequence $x_0, ..., x_{15}$, while Filter 2 is used for the sequence $x_{16}, ..., x_{63}$. The description and timing for the 1st method are summarized in Table 1.

4. IMPLEMENTATION

Synthesis of the proposed architecture was realized with the Xilinx$^{\mathrm{TM}}$ Ise 5.2i tool and the FPGA device that the design was targeted on was Virtex XCV300 package 352g and speed grade -6. The results of synthesis for the architecture and the IFFT block are summarized in Table 2.

5. CONCLUSIONS

In this paper the analysis and design of interpolation and low pass filters in the digital part of the OFDM transmitter was presented. We introduced an architecture of a 64-point FFT architecture followed by digital interpolation filters. By taking advantage of the cyclic repetition of the guard interval of the OFDM symbol, a significant reduction of approximately 20% of the required arithmetic operations, for the operation of the convolution is achieved for a 802.11 WLAN implementation. The implementation is better than previous designs in terms of computational complexity and requires less chip area.

Table 1: Timing and operation of 1st proposed architecture

Number of cycles	Description
1-32	Filter 1 is activated, output data are stored in a 46-word buffer, while the same elements constitute the output of the system (`sel\_buf=0` and `sel_out==00`)
33-46	Filter 2 is also activated (the two filters are working in parallel), while the output consists of the sum of the outputs of the first and second filter (overlap in time (`sel\_buf=0` and `sel_out==01`). After cycle 46, Filter 1 is deactivated.
47-96	The output of the system is the output of Filter 2
97-110	The output of the buffer is added to the output of filter2 (`sel\_buf=1` and `sel_out==01`)
111-174	The output of the system is provided by the output of the buffer.

Table 2: FPGA resource use and performance of the proposed blocks

Virtex XCV 300	**1st Arch.**	**IFFT (Optimized)**
Number of Slices	73%	51%
Number of Flip-Flops	16%	9%
Number of 4-input LUTs	66%	47%
Number of bonded IOBs	20%	19%
Number of BRAMs	12%	-
Number of GCLKs	50%	25%
Max. Frequency (MHz)	53	55.86

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