Hybrid Contention Resolution in Optical Switching Fabric with QoS traffic

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Abstract— **This paper describes an optical switching fabric which solves contention in a hybrid context, by exploiting both time and wavelength domains through wavelength converters and electronic queues. The relationship between the hybrid nature of the switch and the quality of service requirements of traffic is investigated. Different buffer solutions are proposed depending on the employment of different lasers, possibly with tunable capabilities. The main outcomes of the paper suggest criteria to design feasible high capacity optical switching fabrics, suitable for next generation networks, in synergy with present day technology constraints and QoS requirements. The proposed solutions show how the choices in terms of hardware equipment and packet scheduling will influence the main performance figures, which are packet loss, delay and optical transparency.**

Index terms: Optical switching fabric, Hybrid contention resolution, Tunable wavelength converters, Electronic buffers, Service differentiation

I. Introduction

Optical packet switching is a flexible switching technique to cope with different traffic granularities and requirements related to emerging and future Internet services [1], [2], [3]. Many experiments and researches have been carried out in the last decade with the aim to demonstrate optical packet switching capabilities and feasibility [4]. One of the first significant examples is represented by the KEOPS project which can be considered a real pioneering work in this field [5]. Optical technology is now entering in a quite mature phase that can turn into reality many of the ideas related to optical packet switching.

Key sub-systems to implement optical packet-switched networks are optical buffers, optical multiplexers/de-multiplexers and optical switching devices. The related enabling basic building blocks, such as wavelength converters, optical logic gates and regenerators have been demonstrated in single-gate experiments, performing wavelength conversion at rates over 160 Gb/s or regeneration with bitwise processing capability over 40 Gb/s [6], [7], [8], [9], [10], [11]. The evolution from fiber-based single-gate experiments to more complex all-optical sub-systems is made possible by the development of compact SOA-MZI-based optical gates and flip-flops, that exploit the integration capabilities of hybrid technology.

One of the critical points in the design of optical packet switches is still represented by contention resolution, which is typically enabled in electronic packet switches by Random Access Memory (RAM)-based queues. Optical technology corresponding to electronic RAMs is not yet available, although Fiber Delay Lines (FDLs) or slow light could be used to size limited optical packets [12].

With the aim to answer the need of optical industry to design optical packet switches which employ available components, hybrid switch fabrics can be considered [13], [14]. Contention resolution in the time domain is obtained by means of electronic buffers through optical to electronic conversion. In addition, contention resolution in the wavelength domain is obtained by means of wavelength converters [15]. Balance between optical and electronic components is needed to optimize switch cost and match, at the same time, traffic performance requirements. Examples of how to combine different contention resolution schemes in the same optical packet switch, trying to exploit the advantages arising from the interactions among these different approaches, were presented in [17] and [18] for asynchronous and synchronous environments, respectively. In the latter, the concept of hybrid switch which implements multi-domain contention resolution was firstly introduced through a general scheme, consisting of a non-blocking switching matrix with feedback wavelength converters and electronic buffers. After that, a possible implementation with limited complexity was introduced, based on the switching fabric presented in [15], [16], with some preliminary performance evaluation. In this paper a practical implementation of those concepts is analyzed by considering different optical devices to serve the electronic queues and by considering different scheduling algorithms to manage packet forwarding and queuing. To identify the strong aspects and the weaknesses of the different solutions here proposed and to provide a whole picture of the hybrid switch potential, different performance parameters (loss, delay and optical transparency) are considered. Application needs and traffic mix are considered in the definition of the scheduling algorithm. The approach is for this reason defined as 'application aware'.

The paper is organized as follows. Section II provides a description of the hybrid switching fabric. Section III gives details about buffer equipment and management options. Section IV briefly discusses the traffic differentiation and the scheduling algorithms applied to manage packet forwarding. Section V presents and discusses simulation results. Finally, section VI gives the conclusions of the work.

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II. HYBRID OPTICAL SWITCHING FABRIC

The switch architecture proposed here relies on available optical devices (MUX/DEMUXes, couplers/splitters, optical gates etc...) to implement the space switching fabric. Contention is solved in wavelength and time domains, through wavelength converters (WCs) and electronic buffers (EBs), which are shared among the input fibers. The WCs are organized in r_w blocks. EBs are organized in B line cards of M first-in-first-out (FIFO) queues each (one per wavelength). The switch, named H-EOS (Hybrid-Electro/Optical Switch) is sketched in figure 1, as in the case $N = 2$ input fibers (IFs)/output fibers (OFs) carrying $M = 4$ wavelengths each, $r_w = 1$ WC block and $B = 1$ EB block. It could in principle be exploited in different scenarios, ranging from optical circuit switching (OCS) to optical burst/packet switching (OBS/OPS). Here, the switch is supposed to operate in synchronous OPS environment, so the classic assumption of in-band header with a small guard time between header and payload is considered. Of course, in such a scenario synchronizers (not depicted in the figure) are needed at the IFs in order to align the incoming packets.

This architecture was previously considered in [18] as a feedback architecture. Here that architecture is re-organized to better outline the different subsystems for contention resolution (WC and EB blocks). This new representation highlights the modularity of the proposed architecture. In fact, WC and EB blocks can be easily added (removed) to (from) the architecture, by allowing, for example, a gradual migration from optical circuit switching to more dynamic optical packet/burst switching.

As can be seen in the figure, a packet can be directly sent to the OFs through the switching fabric, otherwise it may exploit either WCs or EBs. Neither queuing after wavelength conversion nor optical wavelength conversion after queuing is possible. Indeed, in WC and EB blocks the outgoing signals are directly sent to the destination OFs. The switching fabric is implemented by means of an array of N^2 Wavelength Selectors (WSs), each consisting of two grating Mux/Demux (or any devices with equivalent functionality) in tandem separated by an array of M optical devices (each dedicated to one wavelength) which are able to operate as ON/OFF gates. This kind of switching stage has been extensively considered in literature and is reported for example in [16]. Each array of gates can be implemented by Semiconductor Optical Amplifiers (SOAs) or Micro-Electro-Mechanical Systems (MEMS) technology, used as optical gates. In this work SOAs are considered given that they provide high extinction ratio, switching time in order of few nanoseconds and quite mature technology.

The switching fabric is exploited to directly connect the IFs to the OFs. The WDM signal coming on an IF, after amplification by means of EDFA (Erbium-Doped Fiber Amplifier), is split into $N + B + r_w$ copies, and N of them are connected to the couplers of the different OFs through WSs. In this way, each IF is connected to all OFs, and an OF may be reached by whatever IF. The WDM signal on output of a coupler is amplified by an EDFA before transmission on the OF. The signal on an input wavelength can be forwarded to the desired OF, by turning ON the corresponding optical gate.

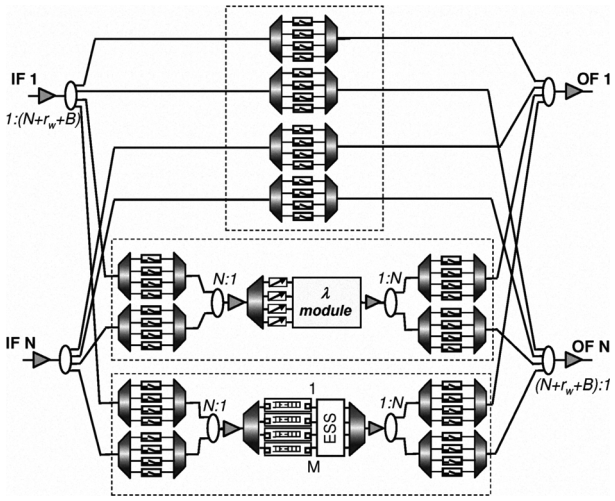

Fig. 1. Hybrid Electro/Optical Switch (H-EOS) with $N = 2$ input/output fiber interfaces carrying $M = 4$ wavelengths each. The switch is equipped with $r_w = 1$ block of M WCs dedicated per wavelength and $B = 1$ EB block, equipped with M electronic queus, one per wavelength, implementing FIFO queues.

This switching stage is wavelength blocking (if two or more packets coming on the same wavelength are directed to the same OF at the same time, one of them is forwarded, the others are blocked), due to wavelength contention.

Now, the subsystems for contention resolution in time and wavelength domains are presented in detail.

III. CONTENTION RESOLUTION IN WAVELENGTH AND TIME DOMAINS

To solve the wavelength blocking previously described, the switch is equipped with r_w shared WC blocks. Each WC block is equipped with M Tunable WCs (TWCs), each dedicated to a different wavelength. This WCs should be all-optical, thus assuring optical transparency, but, due to immaturity of these devices, in a first phase they might be electro-optical devices. The concepts presented in this work are valid for both options, and, if no bit-a-bit operations and 3R regenerations are performed, the optical transparency is anyway maintained. A λ-module combines the M signals in a single WDM multiplex. Each TWC block is equipped with EDFAs at its ingress and egress, to amplify the WDM signal. A more detailed description of this TWC block and λ-module is presented in [16]. Furthermore an analysis of the impact of this particular TWC organization on the scheduling algorithm and performance can be found in [19].

The TWCs in a block are partitioned among the M wavelengths so that r_w TWCs (placed in different blocks) are shared among the packets coming on the same wavelength. The switch applies the shared-per-wavelength strategy, pre-

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sented in detail in [19]. A packet blocked due to wavelength contention on the destination OF can be forwarded to another free wavelength on the same OF by exploiting one of the TWCs dedicated to its wavelength. Due to this particular organization, fixed-input/tunable output wavelength converters can be employed instead of the tunable-input/tunable-output ones, that are supposed to be more complex. To connect the IFs to the TWC blocks, the WDM signal coming on an IF is split into further r_w copies, each one connected to a different TWC block by means of a WS. Similarly, to connect the TWC blocks to the OFs, N copies of the signal outgoing from a TWC block are connected to different OFs through WSs. So, $2Nr_w$ additional WSs are needed to connect the TWC blocks to the IF/OFs.

Wavelength conversion reduces the effect of wavelength blocking, but it is not enough to avoid packet blocking due to output blocking (i.e. lack of free wavelengths on the destination OFs). Furthermore, additional loss will occur when the switch is equipped with an insufficient number of WCs (lack of WCs to perform wavelength conversion).

For these reasons, B EB blocks are available to store blocked packets and solve contention in the time domain. Similarly to TWC blocks, buffer blocks are shared among the IFs. Different technological solutions for an EB block (line card) are plotted in figure 2. All of them use the same demultiplexing, opto/electronic (O/E) conversion, buffering and electronic synchronization stages, while they differ in the last electro/optic (E/O) conversion stage. The EB blocks are equipped with EDFAs at the ingress and egress. Each EB block is equipped with M electronic queues, one per wavelength. First, the WDM signal entering a block is split by means of a DEMUX, and the M signals on different wavelengths are interfaced with the M queues. In each of them, a packet is received on the corresponding wavelength and O/E converted. Then it is stored in a simple FIFO electronic queue, with L packet rooms. At the transmission side, an Electronic Slot Synchronizer (ESS) synchronizes the packets to be forwarded in the current time slot, then they are converted to the optical domain.

To do that, two different options can be considered: the first one is to use Fixed Transmitters (FTs), as in figure 2(a), able to E/O convert the packet in the optical domain on the same wavelength the packet came from, the second one is to exploit Tunable Transmitters (TTs), as in figure 2(b), able to convert a packet in the optical domain on whatever wavelength. This latter solution can also be implemented as in figure 2(c), thus avoiding the use of the TTs but adding an electronic switch before the FTs. The buffer blocks in figure 2(b) and 2(c) provides the same logical functionalities. In the rest of the paper the switch equipped with FTs on the line cards will be referred as H-EOS-FT, while the switch equipped with TTs will be referred as H-EOS-TT (no matter if implemented as in figure 2(c)).

Finally, in both cases the signals after the transmitters are multiplexed in a single fiber. In H-EOS-FT this can be done by a MUX (see 2(a)) or a coupler, while in H-EOS-TT (figure 2(b)), a coupler must be used. Similarly to the TWC block case, B copies of the signal coming on an IF are connected to the buffer blocks by WSs, and the signal at the output of a block is connected to the N OFs. So, $2NB$ WSs are needed.

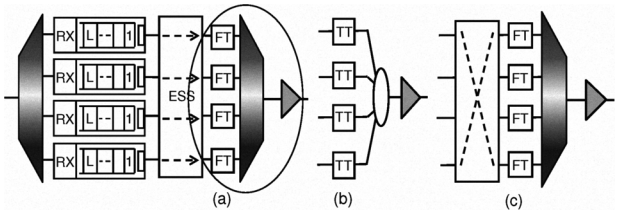

Fig. 2. The electronic buffer block equipped with M line cards dedicated per wavelength; (a) buffer block with Fixed Transmitters (FTs) on output; (b) buffer block with Tunable Transmitters (TTs) on output; (c) alternative implementation of (b) by employing an electronic switch and FTs instead of TTs.

After this description, the number of optical devices needed to implement the switch can be counted. The expressions can be easily evaluated and are presented in table I.

The most complex and expensive devices are the TWCs and SOAs, which are active components. Some considerations about the cost of the switch, in relation to the number of fibers (N), wavelengths (M), WC and EB blocks, can be carried out by observing the values in table I. The number of TWCs needed is of course proportional to the number of WC blocks and to the number of wavelengths in the system. So adding wavelengths to the system means also add WCs to the switch. The number of SOAs is proportional to the number of wavelengths in the system, so the same consideration holds, and it is also proportional to the square of N. So the cost of the switch rapidly increases with the number of IF/OFs, as expected. Also, the number of SOAs increases linearly as the number of WC and EB increases, for given values of N and M. A parametric evaluation of the cost for this kind of architectures, useful to compare different architectures in terms of cost, has been presented in [20]. The work in [20] allows the reader to compare the proposed architecture with others relying on the same optical devices. Furthermore, in [21] a detailed cost evaluation of switching fabrics for terabit packet switches is presented, taking nowadays and foreseeable prices of these optical devices into account.

SOA	$M(N^2+2N(B+r_w))$
TWC	Mr_w
el. queues	MB
MUX/DEMUX	$N^2+2N(B+r_w)$
couplers/splitters	$N+B+r_w$
EDFA	$2(N+B+r_w)$
λ-module	r_w

TABLE I

DEVICE COUNT FOR THE H-EOS SWITCH AS A FUNCTION OF THE NUMBER OF: IF/OFS (N), WAVELENGTHS PER FIBER (M), TWC AND EB BLOCKS (r_w AND B).

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IV. Traffic assumptions and scheduling algorithms

Two different traffic classes with different priorities are considered: CL1 class must be treated with priority with respect to CL2 class in terms of both packet loss and optical transparency.

Packet forwarding must be controlled by a proper scheduling algorithm (SA) which is executed at each time slot within the slot time. A typical organization of such a SA has been introduced in [18] for the general hybrid scheme. Here, different heuristic SAs are presented to manage the H-EOS switch according to the hardware provided (FTs or TTs). For both FT and TT cases, two different options are taken into account: i) schedule the buffered packets first and the others on the IFs later (the corresponding SA is indicated with BF) or ii) schedule the packets coming on the IFs first and the buffered ones later (the corresponding SA is indicated with IFF). A flexible modular organization is here proposed for these SAs. Three different modules are considered: the first schedules the buffered packets, the second schedules the packets coming from outside and the third stores the exceeding packets in the EBs. So, when BF SA must be executed, the right order of execution of these modules is: module 1- module 2 - module 3, while when IFF SA must be executed, the first two modules must be swapped (module 2 executed before module 1). The detailed description of these SAs is out of the scope of this paper, so the three modules are here briefly described (with some references for the reader who wants to go more in detail).
Module 1: schedules the packets stored in the buffer. In H-EOS-FT a packet in the Head Of the Line (HOL) of a queue can be sent if the corresponding wavelength is free in the destination OF. In H-EOS-TT the HOL packet can be sent if there is at least one free wavelength (say k) on both i) the destination OF and ii) the output of the corresponding buffer block. In this phase there is no differentiation among classes, given that buffered packets anyway loses priority. The computational complexity of this module is $O(MB)$ for H-EOS-FT while it is slightly higher (comprised between $O(MB)$ and $O(M^2B)$) for H-EOS-TT.
Module 2: schedules the packets coming on the IFs. The packets are forwarded without wavelength conversion as a first choice, otherwise they exploit the shared TWC blocks. This module corresponds to the SA in the bufferless architecture, presented in detail in [19]. Furthermore, to ensure service differentiation in terms of optical transparency, CL1 packets are scheduled first with respect to CL2 packets. The evaluation of the computational complexity of this module is not trivial, a complete discussion will be found in [19].
Module 3: stores in the EBs the packets coming on the IFs that cannot be forwarded in the current time slot. Due to the organization of the switch, only one packet per wavelength can be stored in a given buffer block, for a total amount of B packets per wavelength in a time slot (similar to the phase three described in [18]). Also in this module, to ensure differentiation in terms of packet loss, CL1 packets are scheduled first. The complexity of this module results in $O(NB)$.
Each of these modules assure the fairness among the fibers and wavelengths through round-robin policies.

V. Performance evaluation

This section illustrates performance evaluation of the H-EOS switch. A simulation tool has been developed, which is able to simulate both H-EOS-FT and H-EOS-TT switches managed by BF or IFF SAs, with either undifferentiated or class-based traffic. Undifferentiated and class-based arrivals are considered as Bernoulli processes. In class-based scenario, CL1 traffic represents a fraction x of the overall traffic, and both CL1 and CL2 traffics are generated as independent Poisson processes. A packet arriving on an input wavelength channel may belong to either CL1 class, with probability x, or CL2 class, with probability $1 - x$. Even if the Poisson process does not exactly reflect the real arrival process as a consequence of packet aggregation at network edges, it represents a simple and effective way to obtain a first analysis of the performance in a synchronous core optical packet switch. Obtained results are useful to carry out some design rules. The simulator is being extended to consider more complex scenarios, such as ON/OFF traffic and mixed optical packet/circuit switched traffic for further in-depth analysis.

The simulator evaluates packet loss probability (PLP), average (AV) and maximum (MAX) delays for the buffered packets, average number of packets leaving the buffers in a time slot and the number of packets transparently forwarded (those which not experience bufferization). So it represents a quite flexible tool to evaluate several traffic performance aspects for these switches.

The results have been obtained by taking into account a switch equipped with $N = 16$ IF/OFs carrying $M = 16$ wavelengths each, with a confidence interval less than or equal to 5% of the mean with 95% probability. The load per wavelength is $p = 0.8$, a quite high value in oder to obtain a high capacity switch. The size of each FIFO queue is 5 packets. It has been verified that, under Bernoulli traffic, this size is enough to ensure no loss due to unavailability of rooms in the buffer blocks, given that only one packet per slot is sent to a particular queue. For this reason, it is useless to increase the number of rooms per queue, while to effectively increase the buffer capability of the switch, some EB blocks should be added.

A. Results for undifferentiated traffic

Figure 3 shows PLP as a function of the number of TWC blocks r_w, varying the number of buffer blocks B. Results are plotted for both H-EOS-FT and H-EOS-TT managed by BF and IFF SAs. Having in mind that the fully equipped switch (in terms of TWCs) would require $r_w = 16$, the figure shows that a limited value of r_w is enough to reach an asymptotic value of PLP, in all cases. This asymptotic value rapidly decreases as B increases, also for this high load ($p = 0.8$). In buffer-less switches ($B = 0$), the asymptotic value is determined by the

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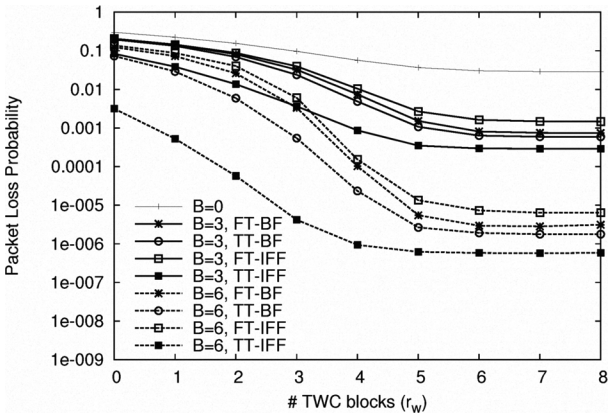

Fig. 3. PLP as a function of the number of TWC blocks, r_w, varying the number of buffer blocks, B, for the H-EOS-FT and H-EOS-TT switches managed by BF and IFF SAs.

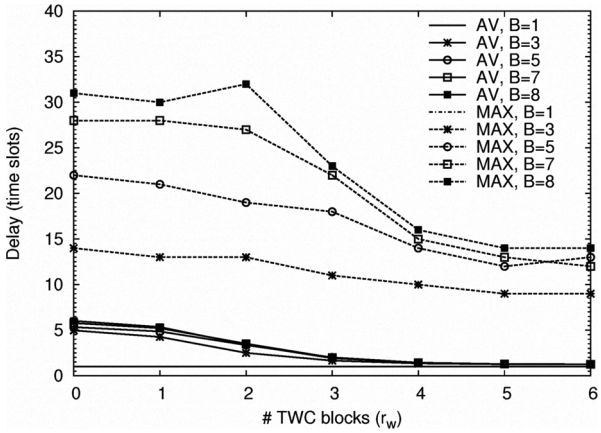

Fig. 4. Average and maximum delays for the buffered packets as a function of the number of TWC blocks, r_w, varying the number of buffer blocks, B, for the H-EOS-FT switch managed by BF SA.

PLP due to output blocking. In buffered switch it is reduced by storing exceeding packets in the electronic buffers. Figure 3 shows that H-EOS-FT switch performs worse than H-EOS-TT in both cases ($B = 3, 6$), as expected. In particular H-EOS-FT managed by IFF SA shows the worst performance in terms of PLP. This is due to the fact that packets coming from outside take resources away from the packets in the buffers, that are scheduled later and do not exploit wavelength conversion. The H-EOS-TT managed by BF SA shows performance similar to H-EOS-FT with BF SA for low number of buffer blocks ($B = 3$), while it allows to obtain some improvements in PLP when the number of buffer blocks is quite high ($B = 6$), especially when r_w is low.

Finally H-EOS-TT managed by IFF SA provides the best performance in terms of PLP, especially when r_w is low (asymptotic value of PLP not still reached). Furthermore, the gain of this solution becomes greater and greater as B increases (in the case $B = 8$, not show here for space reasons, the difference is more than 2 order of magnitude when $r_w < 3$). This improvement is due to the fact that a relevant number of packets coming on the IFs can be sent without wavelength conversion, then other packets are accommodated through wavelength conversion, and finally buffered packets can be sent by exploiting the TTs, until the OFs are not congested. This is not possible when the buffers are considered first (BF SA), given that the packets coming from the buffers are sent in some output channels, so the packets coming on the IFs will see these output resources as busy, and some of them cannot be forwarded due to the low number of shared TWC blocks available.

Figure 4 plots the MAX and AV delays for the buffered packets as a function of r_w, varying B, for the H-EOS-FT switch managed by BF SA. The AV delay is almost invariant with respect to the total number of buffer blocks B, and, in any case, it is lower than 6 time slots, while it is near to 1 time slot if enough TWC blocks are available. The MAX delay shows a high dependence on the number of buffer blocks B, especially when r_w is low (lower than 3). Its value decreases as r_w increases and it is lower than 20 time slots almost independently from B when r_w is high enough (> 3).

As the MAX and AV delays for the H-EOS-TT switch managed by BF SA are concerned, in all the simulations performed, under different switch configurations and loads, both values resulted to be equal to 1 time slot, meaning that a packet stored in a buffer block always leaves the switch in the next time slot. This is obtained thanks to a careful definition of the BF SA, that tries to avoid output congestion by storing packets directed to different OFs (which does not collide) in the different buffer blocks, when possible. This is a quite surprising result that validate the definition of such SA, and makes the switch in this configuration really interesting, due to the very low maximum delay.

Figure 5 shows the AV and MAX delays for H-EOS-FT managed by IFF SA, as a function of r_w and varying B. The AV delay is bounded between 10 and 20 time slots, almost independently of r_w and B. The MAX delay tends to rapidly increase as the number of TWC blocks r_w becomes high, leading to very high values (higher than 50 time slots). These values of delay seem to be very high, this makes the interest of this solution very limited. This delays can be explained taking into account that when r_w increases, more and more packets can be forwarded from the IFs to the OFs; as a consequence, buffered packets see less resources available for possible forwarding, and have to wait next time slots to be transmitted.

The AV and MAX delays for H-EOS-TT managed by IFF are plotted in figure 6, as a function of r_w and varying B. The trend is the same as in the previous figure, but the values are much smaller. The AV delay is very near to one time slot, not matter the number of buffer blocks. The MAX delay becomes higher and higher as the number of buffer blocks B increases,

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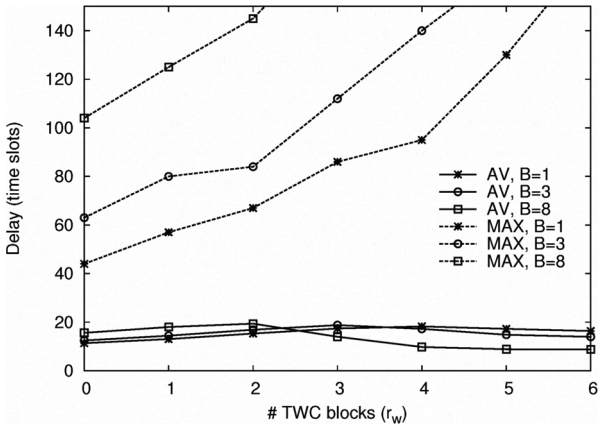

Fig. 5. Average and maximum delays for the buffered packets as a function of the number of TWC blocks, r_w, varying the number of buffer blocks, B, for the H-EOS-FT switch managed by IFF SA.

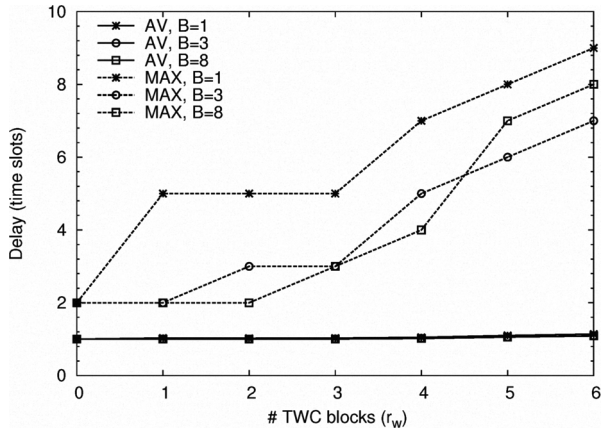

Fig. 6. Average and maximum delays for the buffered packets as a function of the number of TWC blocks, r_w, varying the number of buffer blocks, B, for the H-EOS-TT switch managed by IFF SA.

and it also increases as r_w increases. Thanks to the TTs, the MAX delay is lower than 10 time slots with $r_w = 6$ TWC blocks (please note that this value allows you to obtain the asymptotic value of PLP) even when a high number of buffer blocks is considered.

B. Results for class-based traffic

Next figure 7 presents the PLP for CL1 and CL2 packets as a function of the number of TWC blocks r_w, varying the number of EB blocks B, for H-EOS-FT switch managed by BF SA, as in the case 30% of CL1 packets with respect to the total. As you can see, low PLP ($1e-6$) for CL1 packets in bufferless switch ($B = 0$) can be obtained with quite high values of r_w ($r_w = 5$, while fully equipped switch would require $r_w = 16$), while in buffered switch $B = 5$ this value of PLP can be obtained with few TWC blocks ($r_w = 3$). Furthermore, for bufferless architecture $B = 0$, at least two TWC blocks should be employed to obtain good differentiation among classes. In

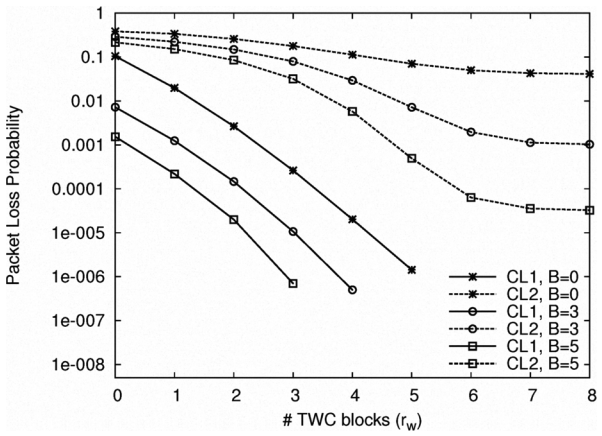

Fig. 7. PLP for CL1 and CL2 classes as a function of the number of TWC blocks, r_w, varying the number of EB blocks, B, for the H-EOS-FT switch managed by BF SA, as in the case 30% of CL1 packets.

this case, the PLP for CL2 packets is very high even for high values of r_w. For buffered switch, good differentiation is obtained even when no TWC blocks are provided.

Figure 8 presents the PLP for CL1 and CL2 packets as a function of the percentage of CL1 packets, varying the number of EB blocks B, as in the case $r_w = 6$. Very good

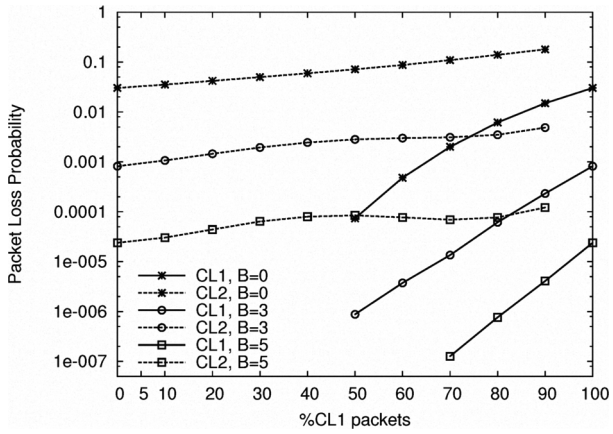

Fig. 8. PLP for CL1 and CL2 classes as a function of the percentage of CL1 packets, varying the number of EB blocks, B, for the H-EOS-FT switch managed by BF SA, as in the case $r_w = 6$.

differentiation between CL1 and CL2 packets is obtained even when the percentage of CL1 packets is high (50-60%). Furthermore, this differentiation is obtained in both bufferless ($B = 0$) and buffered ($B = 3, 5$) switches. As expected, 100% and 0% of CL1 packets cases provide exaclty the same performance, with every value of B.

The differentiation between the two classes should also be evaluated in terms of percentage of Packets Transparently Forwarded (%PTF). This %PTF represents the mean between the number of packets forwarded without bufferization and the total number of packets which are effectively forwarded (so,

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the packets which are discarded are not considered). Figure 9 illustrates %PTF for CL1 and CL2 packets as a function of r_w for H-EOS-FT switch managed by BF SA, varying B as in the case 60% of CL1 packets. The figure shows that the %PTF for

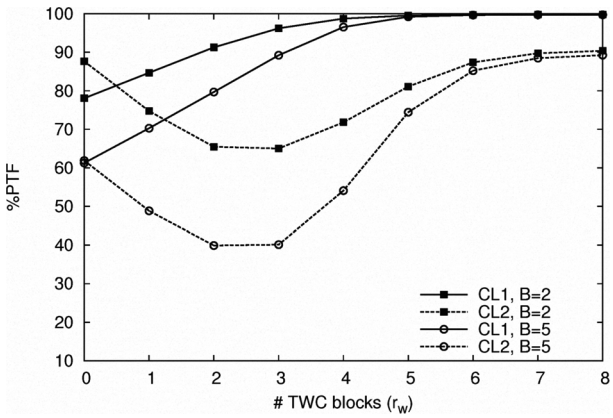

Fig. 9. Percentage of CL1 and CL2 packets transparently forwarded, for H-EOS-FT managed by BT SA. The percentage is plotted as a function of the number of TWC blocks, r_w, varying the number of EB blocks B, as in the case 60% of CL1 packets.

CL1 packets is in any case very high if r_w is high enough, that is exactly what we want to obtain to provide priority to this class. Differentiation among CL1 and CL2 packets is obtained for both values of B (2 and 5), assuming that anough TWC blocks are provided ($r_w > 3$). Quite surprisingly, the %PTF of CL2 class initially decreases. This can be explained by taking into account that when no wavelength conversion is available ($r_w = 0$), the CL1 packets exploits the available EB blocks first, and many CL2 packets are lost (these packets are not considered in the evaluation of %PTF). Indeed when few TWC blocks are available, they are all exploited by CL1 packets, which are considered first, and they occupy the channels on the OFs. When CL2 are considered, no more TWC are available, so these packets must be sent to the EBs, losing transparency. Finally when r_w becomes high, both CL1 and CL2 packets can exploit wavelength conversion, so %PTF for CL2 packets starts increasing.

Similar results as figure 7, 8, 9 have been obtained for all the other cases presented in this paper, confirming that all the proposed solutions provide good differentiation among classes, thus providing priority to the CL1 packets.

VI. Conclusions

A practical solution for high capacity information switching in future multi-service optical networks has been presented. Feasible employment of optical and electronic technology has lead to an hybrid solution that can be designed with present-day hardware and software technologies. A careful study of multi-service support for this kind of hybrid switch has been given, to forward an adequate fraction of high quality traffic in transparent way. Electronic buffers have been shown to be effective and crucial in tuning the packet loss probability to the low values required by semantically transparent services. As far as the optical sub-system, the switch architecture has been thought to be implemented by available photonic devices and to ensure future proof concepts by taking advantage of new components with enhanced functionalities. Different scheduling procedures have been applied and evaluated. In particular, the H-EOS-TT switch managed by IFF SA seems to be the best solution when the number of TWC blocks is limited, due to the very good PLP and the limited values of average and maximum delays. The H-EOS-TT switch with BF provides very good results for the delays and good results for the PLP, so it seems to be a good solution if equipped with an adequate number of TWCs.

As future works, the simulator is being extended to consider more bursty arrival processes such as ON/OFF traffic. Another open issue is the evaluation of the level of out-of-sequence introduced by queuing policies. This problem has to be solved at the edges of the network, so architectures which limits this effect should be preferred, when possible. This work can be a reference platform for further implementation and trials of hybrid optical switches.

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