6H-SiC Based Power VJFET and Its Temperature Dependence

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Abstract. In this paper 6H-SiC VJFET has been shown and the s device characteristics are also shown. Further the optimization is also carried out with respect to the breakdown voltage. 6H-SiC VJFETs breakdown characteristic is also plotted and the parameter dependence of breakdown voltage is also shown. Electric field across the channel and across the channel and across the device length is also plotted.

Keywords: Breakdown voltage, VJFET, channel, doping, SiC.

1 Introduction

Silicon Carbide (SiC) is a new material in the field of power devices. Before the advent of SiC this field was mainly occupied by the Silicon (Si). Now this ubiquitous material (Si) has to share the spot light. Since the Si limit has almost reached in the power applications so the advent of the SiC is good news for power devices industry. For the power applications we need higher band gap energy and higher value of critical electric field which results in higher value of breakdown voltage (BV) and at the same time we need lower value of specific on resistance which further demands higher value of critical electric field and higher value of carrier mobility. SiC has almost 3 times band gap energy than Si and also almost 10 times higher value of critical electric field than Si and these make SiC as material of choice for power devices. Also the SiC has thermal conductivity almost 3 times than that of Si. For the same value of breakdown voltage SiC needs thinner device than Si. All these properties make SiC superior than Si. Many SiC devices like Schottky Diode, VJFET and MOSFET have already arrived to the market. But MOSFETS and IGBT etc., of Si dominate over SiC. Despite the recent advances, the quality of fabricated oxide layer in SiC technology is inferior to that in Si, which adversely affects the mobility of carriers in the channel of the device and hence increases the on-state resistance. Also the reliability of oxide at elevated temperature is still a point of concern. Because of the oxide reliability problem SiC loses the importance of operation at higher temperature.

SiC JFETs, on the other hand, are free of gate oxides. Therefore, they can fully benefit from the superior properties of SiC without being compromised with the poor

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quality of material interfaces. In recent years a number if designs have been developed for the power JFET structures in SiC. A number of these involve a horizontal current control channel above the drift region whilst others use a purely vertical structure. There are two types of JFET namely normally-on and normally-off using the depletion and enhancement mode channel respectively. Normally-on devices are unsuitable for the applications where the power is applied at the start up, such as power supplies and low power drives, where normally-off devices are preferred. The development of enhancement mode VJFETs is necessary for high temperature and high power applications. SiC is said to have more than 200 poly type. The poly type whose wafer is available in the market are 4H, 6H and 3C and the 4H poly type is most matured in terms of device fabrication because of higher value of mobility parallel to c-axis than all other poly type. Table 1 compares the properties of Si and three SiC poly type. 6H-SiC has high value of critical electric field than 4H-SiC and all other poly type and material.

The band gap energy (E_G) in 6H-SiC, as a function of temperature, is approximated by equation (1). Reduced band

$$E_G(T) = 3.0\text{-}3.3\text{x}10^{-4}\,(T\text{-}300)\ \text{eV} \quad (1)$$

gap at higher temperature results in larger intrinsic carrier densities, larger leakage currents in p-n junctions, poorer junction rectification in power switching devices, and poorer device isolation by reverse-biased junctions.

2 VJFET

This is a new device for the new material SiC but not for the Si. Because of the reliability issues related to the SiC/SiO_2 interface at elevated temperature SiC based MOSFETs are not matured fully. So VJFET is a suitable candidate for switch.

Table 1. Electrical and Physical properties of silicon and silicon carbide

Property	**Material**			
	Si	***3C SiC***	***6H SiC***	***4H SiC***
Dielectric Constant	**11.8**	**9.7**	**9.7**	**9.7**
Energy gap (eV)	**1.1**	**2.39**	**3.03**	**3.26**
Critical field E_c (MV/cm)	**0.3**	**1.5**	**3.2**	**3.0**
Electronics mobility μ_n(cm^2/Vs)	**1400**	**`750**	**370**	**800**
Electron Drift Velocity v_{sat} (×=10^7 cm/s)	**1**	**2.5**	**2**	**2**
Thermal conductivity $_k$ (W/cm K)	**1.5**	**5**	**4.9**	**4.9**

operation. Similar to the MOSFET depletion mode VJFET, operates at zero gate bias and negative gate to source voltage is needed to turn it off. The enhancement mode device (JFET) has channel has no channel when V_{GS} = 0V because the depletion regions formed by the gates reduce the conducting channel width and a positive bias turns the device on by creating the channel in the device.

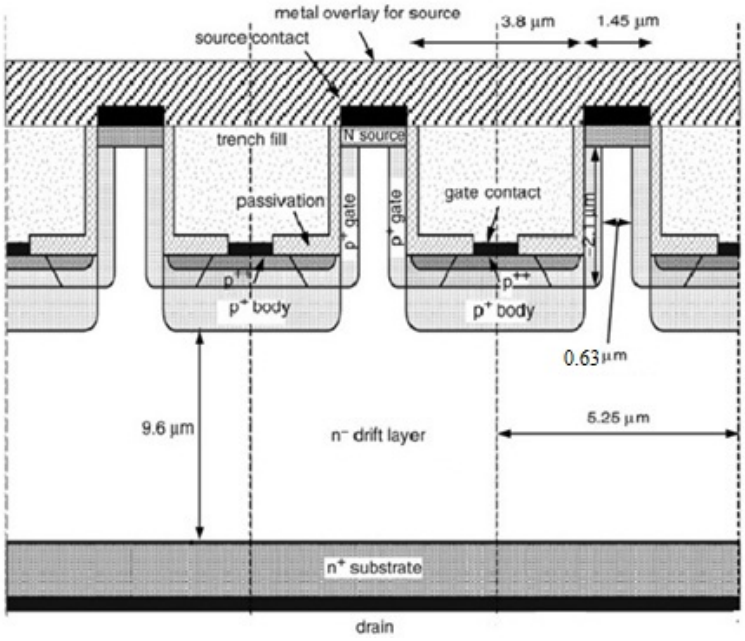

Fig. 1. Cross section of TIVJFET

In order to maintain the unipolar conduction and avoid the significant gate leakage in the on state the maximum allowable gate to source bias should not be more than the 3V which is the built in potential in the case of SiC.

Enhancement mode VJFET is normally-off and is mainly used in the fail-safe operation. In the ON-state majority carriers (electrons) flow vertically from source to drain. To control current through the device gate terminal is subjected to voltage which modulates the depletion width at the junction of n-type channel and p-type gate.

A. Breakdown Voltage (BV)

The breakdown phenomenon ascertains the highest voltage that can be applied and also limits the maximum power it could withstand. In the normally-off device BV is the maximum voltage that can be applied to drain under the condition that gate voltage is kept at 0V, after which the device starts conducting heavily. Breakdown voltage depends on the device parameter like length of the device. Channel width, doping concentration etc. Increasing the length of the device causes the increase in the BV because the JFET sustain this voltage across the drift region. Also reduction in the

doping of the drift region causes the increase in the breakdown voltage as drift region has lower number carriers and breakdown voltage increases. Reduction in the width of channel causes the increment in the breakdown voltage because of the reduction in carriers supplied by source for same drain voltage. These all parameters need to design carefully to fully optimize the device.

B. Fabrication

The device parameters used for the fabrication of the SiC VJFET are to be selected carefully. For the demonstrated VJJFET the active area of the device is 320x293 μm^2. Drift region (n^--type) doping is kept at $6.5x10^{15}$ cm^{-3}. To make the SiC n-type nitrogen and phosphorus are more preferred than other n-type dopant because of smaller size. Doping concentration of source and drain (n^+-type) is kept same at $2.0x10^{19}cm^{-3}$. The trench region is comprised of 50-nm thick thermal oxide, followed by 200-nm thick silicon nitride layer and remaining portion is filled with oxide. The vertical channel is designed to have an opening of 0.63 µm and the length of the blocking layer (drift region) is kept approximately 9.4 µm. Designing of VJFET is done for these values and with the variation of these parameters and temperature optimization of VJFET will be carried out with respect to breakdown voltage.

3 Simulation Results

For the nominal values mentioned above the device simulation is carried out and the breakdown characteristic of is shown in the figure 2. Figure shows that the breakdown takes place at a drain voltage of 1150V. Before breakdown we can see that drain current density is almost zero making it near ideal switch.

As already discussed breakdown takes place under off condition for a gate to source voltage equal to 0V. As the gate voltage is zero there is no channel created and depletion width covers the channel and hence no current flow in the device. Also device can withstand larger voltage across the source and drain. As the drain voltage continue to increase, at the breakdown point suddenly a large current density is created in the device and device starts conducting heavily. For the actual value of the breakdown voltage we have included the impact ionization which is modeled by van Overstraeten-de Man for the 6H-SiC.

Figure 3 shows the I_d-V_d characteristic of the 6H-SiC VJFET for the said parameters for different values of gate voltage (source is kept grounded). Drain current is zero for zero gate voltage and increases with increase of gate voltage for same drain voltage. VJFET starts conducting sufficiently for gate voltage greater than 2V. Id-V_d curves are drawn for gate voltages greater than 3V because of drop in the contact resistances. Higher value of drain current is needed which is achieved at higher value of gate potential. Although the value of drain current is still small but this is sufficient to keep device in the on-state.

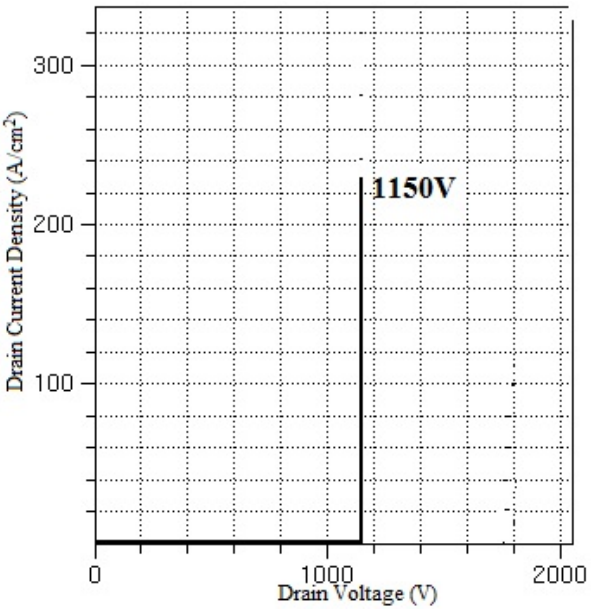

Fig. 2. Breakdown Characteristic of 6H-SiC VJFET

Figure 4 shows the variation of the gate current for different gate voltages. We want this leakage current as small as possible because it hinders the controllability of the drain current (main current) of the device. Logarithmic value of gate current is plotted with drain voltage for different gate voltages increment in the value of gate current is from the order of 10^{-4} to 10^{0} which is very large. The increment in the gate current is because of the forward biasing of p^{+}-n^{-} diode (formed between gate and drift region) becomes more and more forward bias. The increment in the gate voltage is advantageous for the drain current but the corresponding increase in the gate current is unwanted. We want higher value of drain to gate current ratio. For 6H-SiC VJFET at 300K this ratio comes out to be 1798 for a gate voltage of 2.5V. This ratio is good enough at 2.5V. But this ratio decreases with increase of gate voltage.

A. Temperature Dependence

The advantage of the SiC is its operability at elevated temperature. There are variations in the different parameters with temperatures but these variations are smaller than Si and also the range of temperature wider

Figure 5 shows the different I_d-V_d curves at different temperature at a constant gate voltage of 2.5V. Increment in the drain current with the increase of temperature is because of ionization of carriers increases with the increase of temperature as all impurity atoms are not ionized at room temperature. This increase in carriers results in increment of drain current.

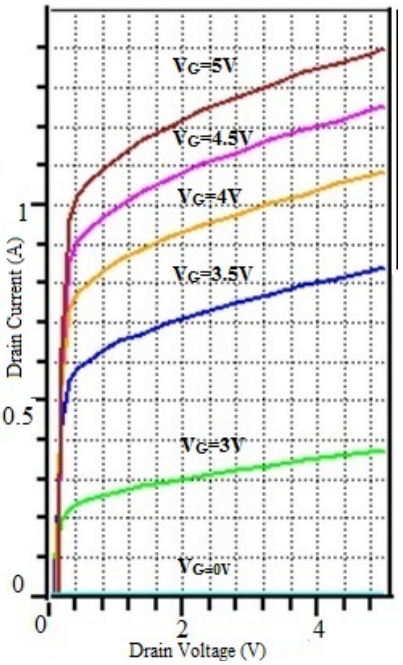

Fig. 3. Id-Vd characteristic of 6H-SiC VJFET

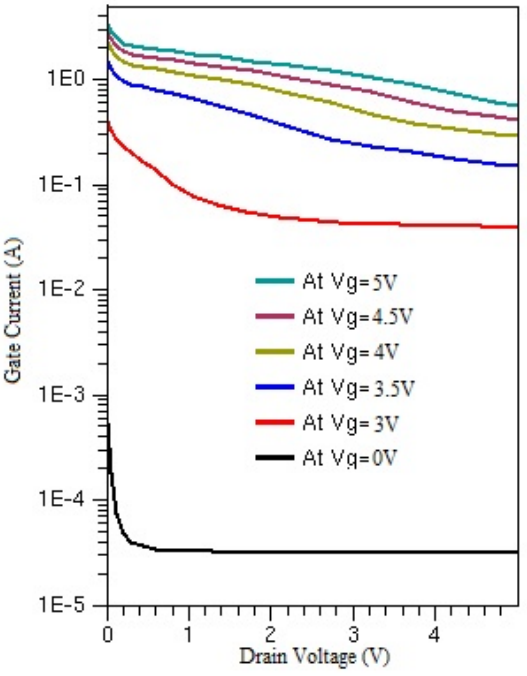

Fig. 4. Gate current at different gate voltages

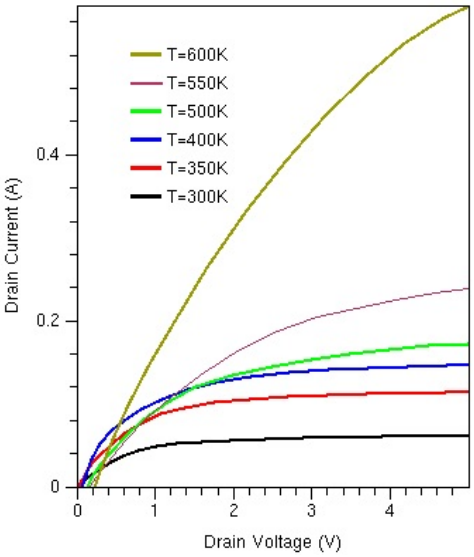

Fig. 5. Id-Vd characteristic variation with temperature

Figure 6 shows the variation of gate current with temperature at a gate voltage of 2.5V. Increase in the temperature results in the increase of ionized carrier and reduction of depletion region which results in the increase in gate current with increase in temperature.

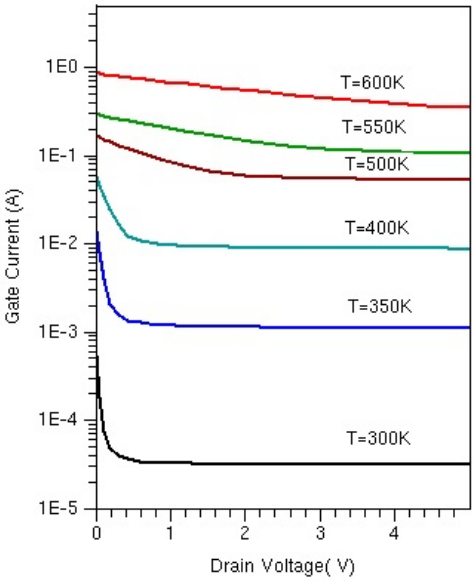

Fig. 6. Gate current at different temperature

4 Conclusions

6H-SiC VJFET is created with the Sentaurus TCAD. Breakdown voltage is found to be 1150V. I_d-V_d characteristic is plotted for different gate voltage. Gate current is also plotted at different gate voltage. The optimum gate voltage is found to be 2.5V as the increase of gate voltage causes the increase of drain current and gate current both. Increase of drain current is positive for the device but there should not be increase in the gate current. Variation of drain and gate current with temperature is shown.

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