An Analog Front-End and ADC Integrated Circuit for Implantable Force and Orientation Measurements in Joint Prosthesis

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Abstract. The paper presents an analogue front-end and ADC integrated circuit for processing signals of sensors implanted into joint prosthesis. The circuit is designed to be operated with Wheatstone bridge sensors, such as strain gauges, pressure, Hall Effect, magneto-resistive sensors, etc. It performs sensor supply multiplexing, sensor signal amplification with chopper modulation, offset compensation and 14-bit analog to digital conversion in a single chip. It can operate simultaneously up to eight sensors at an overall bandwidth of 8 kHz, and can be directly interfaced to a remotely powered RFID system in order to constitute a complete multi-sensor, low-power, small size and externally powered micro-system. Integrated into a 180 nm CMOS process, it measures 5 mm^2, is supplied with 1.8 Volt and consumes 1.8 mW.

Keywords: kinematics, prosthesis, strain gauge, telemetry, front-end, integrated circuit, ADC, monitoring, implantable, electronic.

1 Introduction

In vivo biomechanical monitoring of joint prosthesis and orthopedic implants has gained interest in the last years [1], [2] as a mean to detect premature implant failure, which could avoid harmful and costly revision surgery. It is also of interest during implantation operation, for improving the insertion accuracy, and in the long-term for monitoring the aging of the prosthesis and its impact on the surrounding tissues. The parameters of interest to be measured are the forces applied to the joint, the kinematics of the prosthesis (relative orientation and movements), and its micro-motions and vibrations, which can give indication on the interface between the prosthesis and the surrounding tissues. The first difficulty in the design of such an implant is to find an adequate set of sensors and their efficient placement in the insert to get good sensing accuracy without changing the mechanical and biocompatible properties of the prosthesis, submitted to strict regulations. The second difficulty is to design a compact electronics that does not change significantly the prosthesis properties, and that can be powered and monitored remotely so as to avoid batteries.

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This implies to use a high level of integration, and to minimize the power consumption for allowing small antennas for inductive powering of the system. Finally, the kinematics measurement of the prosthesis from the inside of the body is a challenge; while forces can be measured using strain gauges positioned on the joint interface, and vibrations are detected with accelerometers, the prosthesis kinematics cannot be sensed with traditional methods, due to the impossibility of electrical or optical communication between the two joint parts of the implant. A solution is to use a local magnetic field generated by a permanent magnet located in one part of the prosthesis, and to measure its field intensity by multiple magnetic sensors located in the other part and sensitive to different directions [3]. The 3D relative orientation of the two prosthesis parts can then be computed by merging the different sensor signals.

This paper presents an integrated circuit designed to operate force and magnetic sensors for a microsystem inserted into a joint knee prosthesis. The circuit can power and operate up to eight sensors arranged in a Wheatstone bridge configuration, such as strain gauges, anisotropic magneto-resistive (AMR), and Hall-effect. It embeds a low-noise, high-gain amplification chain, and a 14-bit ADC. It has also a 12-bit DAC for sensor offset compensation. It is powered at 1.8 Volt and consumes 1.8 mW. It can be directly interfaced to an RF communication and power supply system (RFID).

2 Sensors Configuration

The considered prosthesis is a total knee prosthesis, made of a femoral and a tibial part, separated by a polyethylene bearing plate. This plate, of a thickness of 8 to 10 mm, is the ideal location for sensors and electronics. Metallic film strain gauges placed in a Wheatstone bridge were selected for force sensing, and placed at the contact points of the femoral part on the plate (Fig. 1). Depending on the bridge connection, the force difference between the two bridge branches, or the total force, can be measured. This is especially useful for the knee, to measure either force unbalance between two joint sides, or the total force on the joint. The strain gauge signals are weak (in the order of 50 μV) and need amplification by a factor of >1000 to get useful signal for ADC conversion.

There exist several magnetic sensors. The two considered for miniaturization and power consumption reasons are the magneto-resistive and the Hall-effect sensors. Although they use different physical principles, they are relatively similar in terms of input and output impedance (typically 1 to 3 kΩ), and output signal amplitude (a few tenths of mV), considering the targeted magnetic intensity to be measured (10^{-3} to 10^{-2} gauss). Therefore, they do not require high amplification. Regarding their number, like in all triangulation measurements, a higher number of sensed directions and channels increase the accuracy. In the present case, six channels were selected to be a good compromise between accuracy and hardware complexity. Experimental measurements were carried out with a knee simulator and six AMR sensors to validate the accuracy of the proposed orientation sensing principle [3]. A difference of 0.6° RMS was obtained in the dynamic angle estimation compared with an external optical measurement with vicon cameras (Fig. 1).

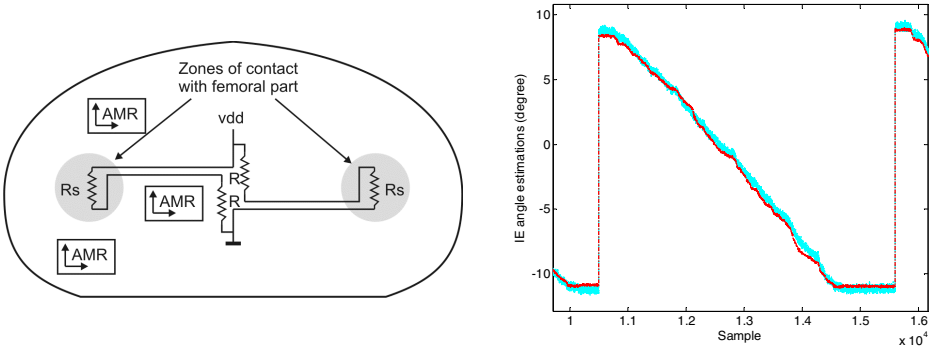

Fig. 1. Left: Location of strain gauge resistors Rs and typical location of three 2-axis AMR sensors in the insert. Right: comparison of two angle measurements of a knee prosthesis placed in a simulator; one with the AMR, and the other with external vision camera system. The RMS difference is 0.6°.

The use of strain gauges to sense efforts in the joint prosthesis determines the parameters for signal conditioning. First, the bandwidth is chosen to be 500 Hz per channel to allow sensing short shocks. Then, the SNR of strain gauge signals is set to 40 dB (100:1) to allow reasonable accuracy measurement at full bandwidth. This sets the input-referred noise density to about 22 nV/Hz$^{0.5}$. For magnetic sensors, an ADC of 14-bit of resolution is needed to fully exploit the sensor sensitivity.

3 Amplification Chain

The architecture of the amplification chain is show in Fig. 2. It includes three stages for high gain, high speed and low power consumption amplification, and input and output chopper switches for flicker noise cancellation.

The first stage is built around a Differential Difference Amplifier (DDA) [4] having a Miller two-stage structure with resistive feedback to provide a programmable voltage gain between 2 and 16. Since its noise is the dominant contribution in the chain, it is carefully designed to provide a low thermal input-referred noise density of 12 nV/Hz$^{0.5}$, and a flicker noise corner frequency at around 15 kHz. The unit capacitor R is 750 Ohm to provide low thermal noise contribution.

The second and third stages are built around a two-stage Miller Differential OTA with capacitive feedback C of 0.6 pF. The input capacitor is programmable from 1.2 to 9.6 pF to allow an overall voltage gain between 2 and 16. In order to set the input common-mode voltage of the amplifiers, a feedback resistor is implemented by means of a switched capacitor circuit with a small capacitor Cr of 10 fF and two switches clocked with non-overlapping phases 1 and 2 at twice the chopper frequency.

The chopper modulation is applied at the input with four switches controlled by signal m, and the demodulation is applied at the output by the same switch arrangement. A second-order passive low-pass filter with a cutoff frequency of 20 kHz (not shown) is present after demodulation to attenuate harmonics resulting

from the modulation. The chopper frequency is programmable, from 25 to 35 kHz. Table 1 shows the key parameters of the amplification chain obtained from simulations.

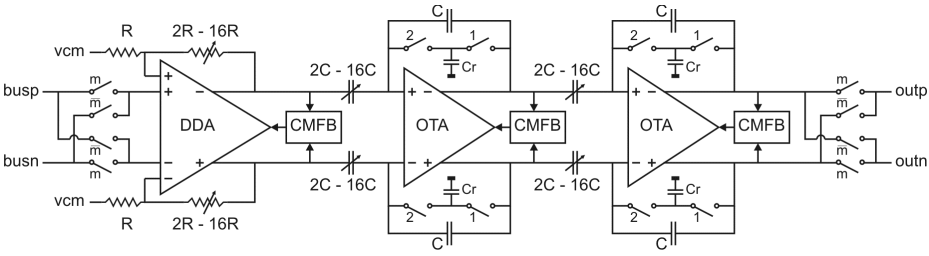

Fig. 2. Amplification chain schematic diagram

Table 1. Performance of amplification chain with chopper modulation

Parameter	Value	Unit
Voltage gain	8 to 4096	
Input bandwidth	10	kHz
Input-referred noise, 0 – 10 kHz	30	$nV/Hz^{0.5}$
Input impedance	>1	MOhm
Max. differential input swing	70	mV
Input common-mode range	0.8 – 1.2	V
Current consumption	600	µA

4 Analog to Digital Converter

To reach 14-bit of resolution, a Sigma-Delta Modulator structure was chosen, whose structure is shown in Fig. 3. It is a third-order modulator with a multi-bit resolution of 4 bit in the feedback path. A multi-bit implementation allows reaching a better SNR for the same oversampling ratio, therefore permits lower power consumption. The modulator includes feed-forward paths on all stages that reduce the signal dynamic, thus strongly relaxes the linearity requirements of the integrators. The 4-bit quantizer includes also passive feed-forward at its input stage. On the feedback path, the 4-bit DACs are implemented on each stage input with a capacitive network of 15 unit capacitors.

Normally, the SNR of a multi-bit Sigma-Delta modulator is limited to 10 bit by the linearity of the first stage DAC, if no linearization technique is used. In order to reach 14-bit, two techniques are implemented. The first uses dynamic element matching, and consists of a scrambling logic on the digital feedback path that selects different DAC unit elements at each conversion, in a way that their mismatch is averaged and the resulting non-linearity is strongly reduced. Data-Weighted Averaging [5] is the chosen algorithm as scrambling law.

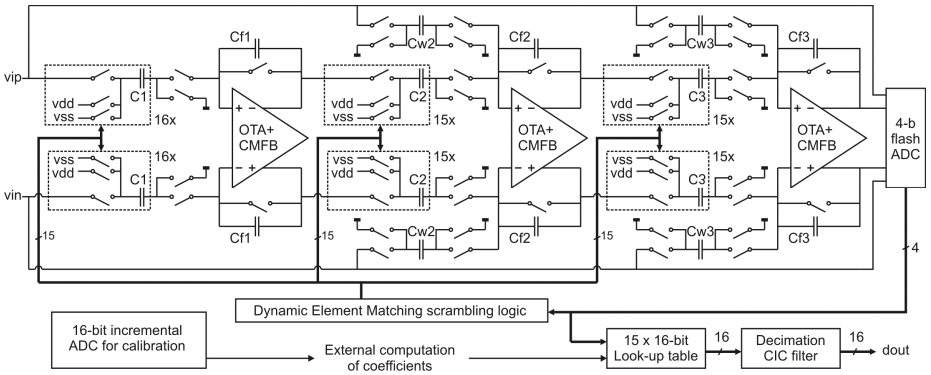

Fig. 3. Analog to Digital Converter schematic diagram

The second linearization technique is based on a background calibration that can be run continuously during circuit operation [6]. The 4-bit DAC of the first stage is made of an array of 16 elements. Each one of these elements can be disconnected from the bank and connected to an incremental 16-bit ADC that measures the capacitor value against a reference capacitor. The correction coefficients can then be computed by the host processor, and written back in a 15x 16-bit Look-Up Table placed before the ADC output decimation filter.

The ADC decimation filter is a standard Cascaded Integrator Comb structure with 5 stages, allowing attenuation of 85 dB before down-sampling by a factor of 32. The output sampling rate is 52 kHz, while the modulator is clocked at a frequency of 1.695 MHz. The ADC modulator consumes 160 µA, and the DEM logic and CIC filter consume together 60 µA. The SNDR of the modulator was simulated at 87 dB.

5 DAC for Sensor Offset Calibration

Since their resistors are subject to mismatch, Wheatstone bridge sensors are affected by offset, which needs to be compensated before amplification. For this, a simple offset compensation scheme is used, consisting of biasing one of the two bridge branches with a resistor and a voltage from a DAC. Choosing an appropriate DAC output voltage allows to modify the DC voltage of the branch and to compensate for sensor offset. The on-chip implementation relies on a programmable resistor whose value can be tuned between 10 and 160 kOhm by steps of 10 kOhm to accommodate for various sensor impedances and offset variations, and on a 12-bit DAC for having a small quantization error. The schematic diagram of the DAC with programmable bias resistor is shown in Fig. 4. Since the DAC is used in a calibration procedure, its integral non-linearity is not critical but the differential non-linearity must remain below 1 LSB. A sub-ranging structure is proposed, made of a first resistive voltage divider with 64 resistors of 3.4 kOhm (6 most significant bits). A 6-bit decoder and a double switch array allow to select the upper and lower point of a given resistor, and to pass the corresponding voltages to voltage buffers. These buffers power a second

resistive divider, with 64 resistors of 3.4 kOhm. A second 6-bit decoder and switch array permit the selection of the final output voltage, which is buffered before being applied to the programmable bias resistor. The DAC has a DNL level of 12-bit, consumes 140 µA and has a bandwidth of 20 kHz.

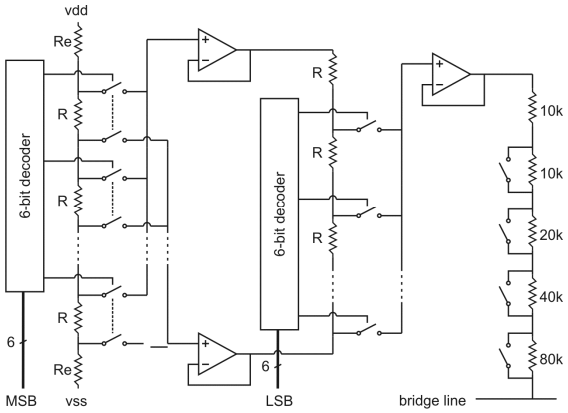

Fig. 4. Offset compensation DAC with programmable bias resistor

6 Chip Architecture

6.1 Input Switches

Fig. 5 shows the internal switches performing multiplexing and powering for the eight sensor channels. To obtain low system power consumption, the sensors must be supplied only when they are read out. For this, the circuit includes one supply line for each sensor, active when the sensor is addressed (signal s active). Two channels are equipped with a 4-wire configuration allowing to swap the resistors of one half bridge to perform summing (signal a active) or differential (signal a inactive) readout modes.

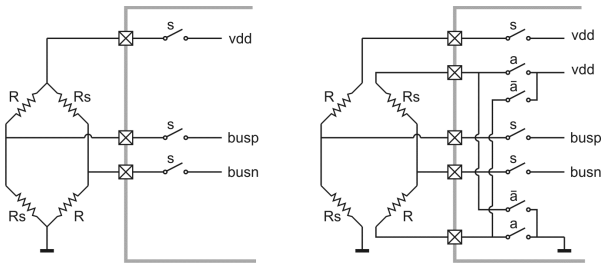

Fig. 5. Internal switches for sensor selection and powering. Left: 2-wire sensor, right: 4-wire sensor for summing or differential readout modes.

6.2 Top-Level

The circuit overall architecture is represented in Fig. 6. Up to 8 sensor bridges can be connected, two of them in a 4-wire configuration. After channel multiplexing, one of the signal bus lines is connected to the offset compensation DAC through the programmable bias resistor. The sensor signal is fed to the amplification chain, the low-pass filtering, and the Sigma-Delta modulator. An on-chip PTAT current reference provides the analog blocks with biasing. The circuit includes digital functions related to ADC (decimation filter, dynamic element matching logic), control logic and a bank of 64 x 8-bit registers which can be read through an SPI interface. The channel selection is controlled through the same SPI. The registers contain individual gain and offset settings for all channels, allowing fast channel switching.

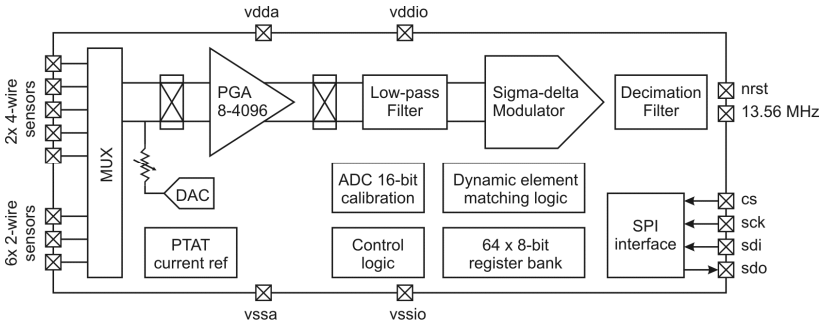

Fig. 6. Top-level circuit architecture

6.3 Layout and Performance Summary

The circuit was integrated into a CMOS 180 nm process technology. The layout is shown in Fig. 7. The circuit expected performances are summarized in Table 2.

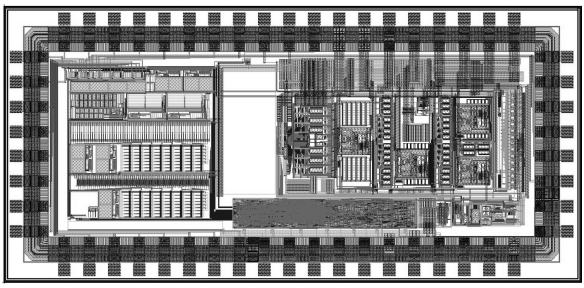

Fig. 7. Circuit layout. Dimensions are 3.2 x 1.6 mm

Table 2. Circuit main parameters and expected performances

Parameter	Value	Unit
Voltage supply	1.8	V
Input clock	13.56	MHz
Current consumption	1	mA
Max. bandwidth per channel	1	kHz
SNR, strain gauges, BW = 500 Hz	40	dB
SNR, magneto-resistors	80	dB

7 Conclusion

The paper presented an integrated circuit for operating 2 strain gauge and 6 magneto-resistive sensors in a knee prosthesis for in vivo force and orientation measurements. The circuit will contribute to high level of integration, small size and low power consumption of the implant.

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