Testing of Reversible Combinational Circuits

Y. Syamala, A.V.N. Tilak, and K. Srilakshmi

Gudlavalleru Engineering College, Gudlavalleru
{coolsyamu,slkaza06}@gmail.com
avntilak@yahoo.com

Abstract. Reversible logic is becoming one of the emerging technologies because of its applications in low power design, quantum computing, quantum dot cellular automata and optical computing. As a result, design of reversible logic computing has been gaining more and more attention from researchers, since, under ideal physical circumstances the power dissipation of reversible computing is zero. Conventional decoder and encoder circuits which found applications in memories, processors, communications etc., are power inefficient. In this work, a decoder, encoder and priority encoder are realized using reversible logic to reduce power dissipation. A reversible linear feedback shift register and multiple input signature register are designed to facilitate built – in self-test based on signature analysis. The proposed circuits are tested for single stuck-at, single missing gate and multiple missing gate faults.

Keywords: Low power design, reversible logic, fault models, testing, signature analysis**.**

1 Introduction

Now a days, power dissipation plays an important role in the design of VLSI circuits, especially when there is an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking these circuits with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer [1], irreversible logic computation results in energy dissipation due to power loss. This is because, erasure of each bit of information dissipates at least KTln2 joules of energy, where K is Boltzmann's constant and T is the absolute temperature at which the operation is performed. If Moore's law continues to be in effect, it is predicted that by year 2020 this will become a substantial part of energy dissipation.

Further, Bennet [2] had shown that the energy dissipation problem of VLSI circuits designed using conventional (irreversible) logic gates can be overcome by using reversible logic gates. This is due to the fact that reversible logic naturally takes care of heating, since, in reversible circuits, the input vectors can be uniquely recovered from its corresponding output vectors.

Reversible computation requires reversible logic circuits and synthesis of these circuits differs significantly from its irreversible counterpart because of different factors [3]. Reversible circuits are designed using reversible gates which are logic

gates that can generate unique output vector from each input vector, and vice versa, i.e., there is a one-to-one mapping between the input and the output vectors. A number of reversible gates such as the Fredkin, Toffoli, Peres, and Feynman, etc., are available for the synthesis of reversible logic circuits. Synthesizing a logic circuit using reversible logic gates should satisfy the following features: minimum number of reversible gates and constant inputs, with a few garbage outputs. Two restrictions that have to be followed while designing reversible circuits are i) fan out is not considered and ii) feedback loops are not permitted in the system.

Decoders and encoders are some of the basic building blocks of complex combinational circuits and they play an important role either to derive a number of control signals from a binary coded signal or to generate a number of outputs based on single – bit information.

Testing and failure analysis of logical circuits are very important during and after the design and manufacturing, to ensure their functionality and durability. The testing problems posed by irreversible circuits are very challenging due to the complexity of their normal and faulty behavior models [4], [5], [6]. However, the complexity of test generation is lower for reversible circuits than for conventional irreversible ones; viz. all multiple stuck-at faults are covered by a complete test set for single stuck-at faults [7].

Faults can be located at several places in a circuit and it is difficult to determine at which place errors would likely to occur because there does not exist a commonly agreed upon technology for building reversible logic circuits. In order to test for all likely faults accurately, different fault models, such as stuck-at, single missing gate, and multiple missing gate fault models [8] are applied for the reversible decoder, encoder, and priority encoder circuits realized using Fredkin gates.

Built-in self-test (BIST) is well known for it's faster, less expensive and on-chip test process for testing integrated circuits [9]. An algorithm is proposed for fault localization by preset method, and testing of the designed circuits to determine the fault coverage is carried out by making use of reversible linear feedback shift register (LFSR) [10] and multiple input signature register (MISR) techniques.

The remainder of the paper is organized as follows: section 2 gives the realization of decoder, encoder and priority encoder using Fredkin gates. Fault models and testing aspects are discussed in section 3 and finally section 4 concludes the paper.

2   Realization of Proposed Circuits using Reversible Gates

Reversible decoder, encoder and priority encoder circuits are realized using Fredkin gates. The Fredkin gate as shown in Figure 1(a) is a (3, 3) reversible gate with (A,B,C) and (P,Q,R) as the input and output vectors respectively. The outputs are given by $P=A$, $Q= \overline{A}B \oplus AC$, and $R= \overline{A}C \oplus AB$. Figure 1(b) gives the quantum representation of the Fredkin gate shown in Figure 1(a). Its quantum cost as estimated from Figure 1(b) is 5.
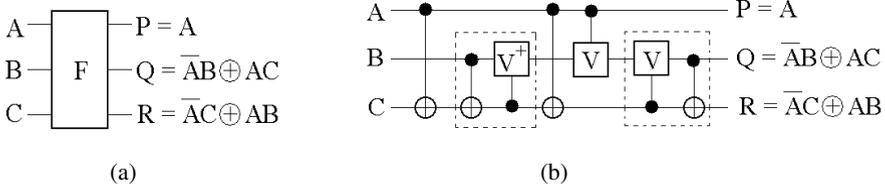
(a)   (b)

Fig. 1. (a) Fredkin gate (b) Quantum representation

A reversible 2 to 4 decoder circuit realized using three Fredkin gates is shown in Figure 2. The logic expressions for the four outputs (Y_0, Y_1, Y_2, Y_3) of the decoder are given by

$$Y_0 = En.\overline{I_0}.\overline{I_1} \tag{1}$$

$$Y_1 = En.\overline{I_0}.I_1 \tag{2}$$

$$Y_2 = En.I_0.\overline{I_1} \tag{3}$$

$$Y_3 = En.I_0.I_1 \tag{4}$$

where En is the enable input; I_0 and I_1 are the inputs. It makes use of three constant inputs and produces two garbage outputs, G_1 and G_2. The quantum cost and depth for the circuit is 15.
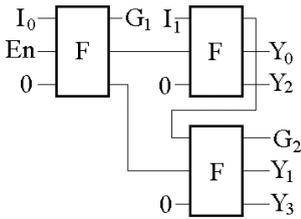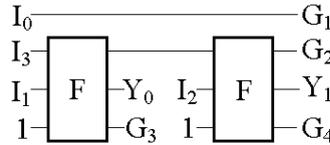

Fig. 2. Reversible 2 to 4 decoder   **Fig. 3.** Reversible 4 to 2 encoder

Figure 3 shows the implementation of reversible 4 to 2 encoder with only two Fredkin gates. The encoder with I_0, I_1, I_2 and I_3 as inputs and Y_0, Y_1 as outputs is characterized by

$$Y_0 = I_1 + I_3 \tag{5}$$

$$Y_1 = I_2 + I_3 \tag{6}$$

This makes use of two constant inputs and the number of garbage outputs is 4. Its quantum cost and depth is 10.

The output logic expressions of the 4 to 2 priority encoder are given by

$$Y_0 = I_3 + I_1\overline{I_2} \tag{7}$$

$$Y_1 = I_2 + I_3 \qquad\qquad (8)$$

where I_0, I_1, I_2 and I_3 are the inputs and Y_0, Y1 are the outputs. A reversible 4 to 2 priority encoder shown in Figure 4 makes use of 3 Fredkin gates and 3 constant inputs, producing 5 garbage outputs. The quantum cost and depth for the circuit is 15.
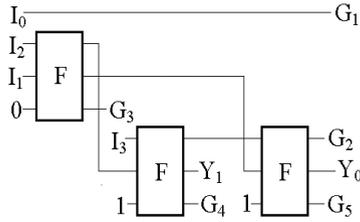

Fig. 4. Reversible 4 to 2 priority encoder

3   Testing

An important aspect of testing of reversible circuits is to determine what kinds of faults are possible and where they are likely to occur. This work is focused on fault detection as well as fault localization to locate stuck-at, single missing gate, and multiple missing gate faults [11], [12] for the proposed circuits.

The stuck-at fault (SAF) model assumes that there is a problem with one of the horizontal wires on the circuit. A passing bit can either get stuck at value zero, or stuck at value one. A circuit with n bits and m stages will have ((m+1)*n) locations where a fault might occur. Since the stuck-at fault model covers two types of faults at each location where a fault might occur, the total number of faults covered by the model is ((m+1)*2n).

The missing gate fault (MGF) model assumes complete removal of a gate operation, or equivalently, replacement of the gate by a set of wires. When a control on a controlled gate in a reversible circuit is damaged in such a way that it can never be turned on, the gate that is being controlled cannot be activated. An equivalent circuit diagram would look the same, but with one gate removed. Missing gate faults can be either single missing gate or multiple missing gate faults. Single missing gate fault (SMGF) model is defined by the removal of a single gate whereas multiple missing gate fault (MMGF) model assumes the removal of more than one gate.

Localization of faults [13] can be achieved either by preset method or by adaptive tree method. Preset method considers the analysis of the localization in tabular manner only, whereas adaptive method adds the graphical tree approach to preset method. The two methods will give the same result. A general algorithm for fault localization using preset method is given below.

Algorithm 1.   Fault localization – Preset Method

```
Fault_localization (i, m, T, Test_set, Minimal_test_set)
{
   m = number of inputs;
   i = 0 to (2^m - 1);
   Test_set = {T_i};
   Minimal_test_set = { };
   For each i in T_i
   {
      If (essential (T_i) = = 1)
      /* Essential  test  vector  is  the  vector  that  only
covers a particular fault*/
      {
         Minimal_test_set = {(Minimal_test_set) U T_i};
         Test_set = {(Test_set) - T_i};
      }
      Else
      {
         Minimal_test_set = Minimal_test_set;
         Test_set = Test_set;
      }
      End if;
      i = i+1;
   }
   While (Test_set (! empty))
   {
      If (dominating_row (T_i) = = 1)
      /* A test vector is said to be corresponding to a
dominating  row,  if  it  covers  all  the  faults  that  are
covered by another test vector*/
      {
         Minimal_test_set = {(Minimal_test_set) U T_i};
         Test_set = {(Test_set) - T_i};
      }
      Else
      {
         Minimal_test_set = Minimal_test_set;
         Test_set = Test_set;
      }
      End if;
   }
   Return Minimal_test_set;
}
```

In the algorithm given, Test_set contains the input combinations and Minimal_test_set contains test vectors that cover all the faults. The first loop of the algorithm is to find the essential test vectors, and the second is to find the test vectors corresponding to dominating row. Both loops executes until the input Test_set becomes empty which indicates that all the test vectors are tested for faults. The minimum number of vectors that are required for covering all faults is obtained from Minimal_test_set and are tabulated in Table 1 for the realized circuits.

Table 1. Comparison of various fault models with preset method

Reversible circuit	No. of test vectors required with		
	SAF	SMGF	MMGF
2 to 4 decoder	5	2	1
4 to 2 encoder	--	1	1
4 to 2 priority encoder	4	2	1

It is to be noted that it is not possible to model the encoder circuit using stuck–at fault model, because the encoder circuit is designed under the assumption that only one input should be active at a time.

Testing of proposed circuits is carried out using BIST technique to determine their fault coverage by introducing the stuck-at, single missing gate, and multiple missing gate faults.
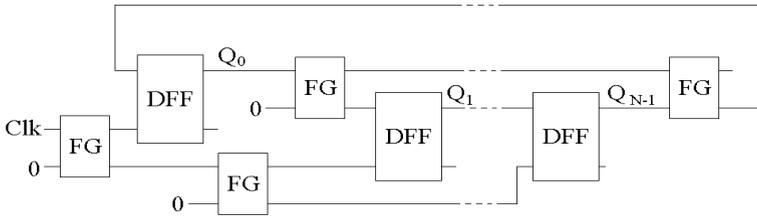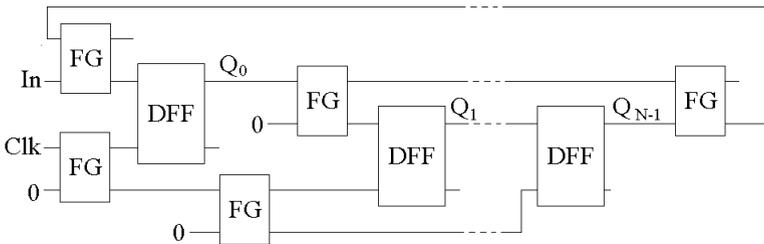

Fig. 5. An N-bit reversible LFSR

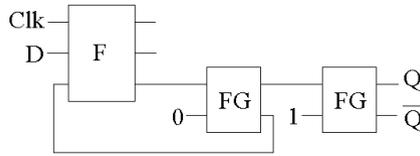
Fig. 6. An N-bit reversible MISR

Fig. 7. Reversible D flip-flop

An N-bit reversible LFSR and MISR are shown in Figures 5 and 6 respectively. The reversible D flip-flop used in LFSR and MISR is given in Figure 7. The MISR produces signature which is said to be good if the circuit is not faulty. Now under testing process, the faults are introduced in the circuit under test (CUT), and the outputs produced from the CUT are given as inputs to MISR, thereby producing signatures. For each fault, the signature produced is compared with good signature. If both are not same, the fault is said to be detected, otherwise not detected.

Table 2 summarizes the testing results obtained through BIST. Good signature is the signature obtained from signature analyzer for the fault-free circuit and is shown for the three types of faults in binary form.

Table 2. Testing results of proposed reversible circuits using BIST

	Reversible circuit	2 to 4 decoder	4 to 2 encoder	4 to 2 priority encoder
	Good signature	0110 (6)	11 (3)	10 (2)
SAF	Total no. of faults	20	12	16
	Detected faults	17	12	12
	Fault coverage (%)	85	100	75
MGF	Total no. of faults	3	2	3
	Detected faults	3	2	3
	Fault coverage (%)	100	100	100
MMGF	Total no. of faults	4	1	1
	Detected faults	2	1	1
	Fault coverage (%)	50	100	100

The number within brackets indicates the decimal equivalent of good signature. The Table 2 lists the number of faults detected out of the total number of faults created and the percentage fault coverage for each of the three fault models considered. The fault coverage is found to be 85% with SAF model and 50% with MMGF model for the reversible 2 to 4 decoder and is only 75% for priority encoder using SAF model. In all other cases it is found to be 100%.

4   Conclusions

Reversible 2 to 4 decoder, 4 to 2 encoder and 4 to 2 priority encoder are synthesized using Fredkin gates. Three different fault models are considered and the circuits are tested using preset method and BIST. The test results indicates not only the number of test vectors can be found by using various fault models but also can achieve greater amount of fault coverage.

References

1. Landauer, R.: Irreversibility and Heat Generation in the Computing Process. IBM J. Research and Development 5, 183–191 (1961)
2. Bennet, C.H.: Logical Reversibility of Computation. IBM J. Research and Development 17, 525–532 (1973)
3. Shende, V.V., Prasad, A.K., Markov, I.L., Hayes, J.P.: Reversible Logic Circuit Synthesis. In: International Conference on Computer – Aided Design, San Jose, California, USA, pp. 125–132 (2002)
4. Kvill, E., Laflamma, R., Ashikhmin, A., Barnum, H., Viola, L., Zurek, W.H.: Introduction to Quantum Error Correction. Los Alamos Science, 188–221 (2002)
5. Nielsen, M.A., Chuang, I.C.: Quantum Computation and Quantum Information. Cambridge Univ. Press (2000)
6. Obenland, K.M., Despain, A.M.: Impact of errors on Quantum Computer Architecture. Tech. Rep, University of Southern California (1996)
7. Patel, K.N., Hayes, J.P., Markov, I.L.: Fault Testing for Reversible Circuits. IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems 23(8), 1220–1230 (2004)
8. Hayes, J.P., Polian, I., Becker, B.: Testing for Missing-gate Faults in Reversible Circuits. In: Proceeding of 13th Asian Test Symposium, Taiwan, pp. 100–105 (2004)
9. Schiniger, A.: Testing and Built-in Self Test – a Survey. Journal of Systems Architecture 46, 721–747 (2000)
10. Chen, J., Vasudevan, D.P., Popovici, E., Schellekens, M.: Reversible Online BIST Using Bidirectional BILBO. In: Proceeding of ACM International Conference on Computing Frontiers, pp. 257–266 (2010)
11. Polian, I., Fiehn, T., Becker, B., Hayes, J.P.: A Family of Logical Fault Models for Reversible Circuits. In: Proceeding of 14th Asian Test Symposium, pp. 422–427 (2005)
12. Vasudevan, D.P., Lala, P.K., Parkerson, J.P.: CMOS Realization of Online Testable Reversible Logic Gates. In: Proceeding of IEEE Annual Symposium on Computer Society, VLSI, pp. 309–310 (2005)
13. Ramasamy, K., Tagare, R., Perkins, E., Perkowski, M.: Fault Localization in Reversible Circuits is Easier Than for Classical Circuits. In: Proceeding of the International Workshop on Logic and Synthesis (2004)