Comparative Study of Crosstalk Reduction Techniques for Parallel Microstriplines

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Abstract. Reduction of crosstalk among interconnects and PCB traces to a tolerable level are an important goal in circuit design. This paper present the comparative study of crosstalk reduction techniques for parallel microstriplines. Parallel microstrip line is treated as a symmetrical network with four ports Here the affection of the guard trace with vias and serpentine trace with vias to the function of the parallel microstriplines. are analyzed and simulated in terms of S parameters From the S parameters the effect of guard trace is analyzed. Simulation results are presented in terms of coupling strength.

Keywords: Crosstalk, Parallel Microstriplines, Guard Trace, Vias, Serpentine Trace and Coupling Strength.

1 Introduction

Microstrip lines are widely used for chip to chip interconnect on printed circuit board (PCB) mainly for low cost. In the two parallel microstrip lines, a large impulse type far end crosstalk voltage appears at one side of the victim line, when a digital signal is applied at the opposite side of the aggressor line. This far end crosstalk voltage is induced by the difference between the capacitive and inductive coupling ratios of two microstriplines [1] Although there is no far end crosstalk induced in the strip lines. The strip lines are more costly than the microstrip lines because strip lines need more PCB layers. To reduce the far end crosstalk in the microstriplines, the extra dielectric material can be deposited over the microstrip lines. This extra material deposition is a cost adding process One of the method to reduce the far end crosstalk is widening the spacing between the strip lines. But it increases PCB routing area. One new method is to set a guard trace with vias between these parallel microstrip lines. This solution has been taken in many applications many PCBs designers use guard trace with vias to reduce coupling. This via stitch guard imposes the restriction on the PCB backside routing due to via holes. In this work a guard trace with the serpentine form was proposed to reduce crosstalk effectively and also this paper presents the comparative study of guard trace with vias and serpentine trace.

2 Parallel Microstripline

Fig 1 shows the cross section of a coupled microstrip line pair in the inhomogeneous medium with the top side exposed to air. In the geometry of the microstripline, W represents width of conducting strip, h is the substrate height, t is the thickness of the conductor, s is the spacing between the two microstriplines and 1 is the length of the microstripline. An isolated transmission line can be modeled by the uniformly distributed self capacitance (C_s) and self inductance (L_s). A pair of coupled transmission lines can be modeled by the uniformly distributed mutual capacitance (C_m) and mutual inductance (L_m) in addition to the self capacitance (C_s) and the self inductance (L_s)[3], as shown in Fig 2.

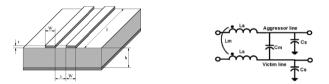


Fig. 1. Parallel Microstriplines Fig. 2. Model of the parallel Microstriplines

3 Proposed Structure

In this paper, work is focused on how to reduce the coupling strength between the parallel microstrip lines. The schematic diagram shown in Fig 3(a) for parallel microstrip line without guard trace. In the simulation experiment, the structure of parallel microstrip line is treated as a four port symmetrical network and which with a guard trace is also treated as such a network. Fig 3 gives various parallel microstripline structures. The parameters of the simulated structures are the two

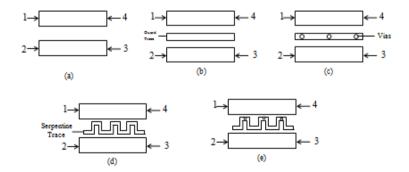
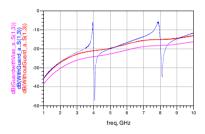


Fig. 3. Schematic Diagram of (a) Parallel Microstriplines (b) Parallel Microstriplines with Guard Trace (c) Guard Trace with vias (d) Parallel Microstriplines with Serpentine Trace (e) Serpentine Guard Trace with Vias

microstrip line length is 21.5234mm and the width of the microstrip line is 1.809mm the Spacing between the microstripline is 1.5mm. Width off the guard trace is 0.5mm, the distance between the transmission line and the guard trace is 0.5mm, the diameter of the via is 0.4 mm the distribution of the vias in the guard trace is always homogeneous the length of the guard trace is the same with that of the microstripline. Each port is matched a resistance 50Ω . The proposed structure of the serpentine trace width is 0.5mm and the length is 22mm the spacing between the microstripline and the serpentine trace is 0.5mm. The simulation method is momentum method and the frequency range is 1-10GHz.

4 Result and Discussions

Here the simulation results were obtained from commercial simulated software ADS. Table 1 shows the parameters taken for simulating parallel microstrip lines and various structures [4].



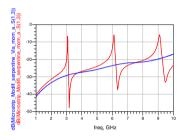


Fig. 5. Simulation Results of Without Guard With Guard and Vias

Fig. 6. Simulation Results of the Serpentine Trace and Serpentine Trace with Vias

Fig 5 and Fig 6 shows the simulation results obtained by using the simulation tool ADS. Parallel microstrip line with guard trace is treated as a four port symmetrical network. If port 1 is a input port, port 2 is a cutoff port, port 3 is a coupling port and port 4 is a transmission port . Because of the symmetry S13 = S31. The results are obtained in terms of S parameters. From the S parameters coupling between the lines are analyzed. Therefore S13 is the main parameter for analysis. when the distance is 1.5 mm without guard trace the coupling degree will increased from -30dB at 1 GHz to -10dB at 10GHz, if a suspended guard trace is put between these two microstrip lines, the coupling intensity will increase at some frequencies, because at those frequencies resonance will be generated in the guard trace. A standing wave will be generated in the guard trace so the coupling between the parallel lines increases. Table 2 gives the comparison of Coupling Strength for the different microstripline structures.

Structure	Frequency	dB(S(1,3)) (Coupling Strength)
Without Guard Trace	10 GHz	-7.992 Max
With Guard Trace	7.858 GHz	-4.805 Max
Guard Trace with Vias (9 Vias)	10 GHz	-18.332 Max
With Serpentine Trace	9.096 GHz	-5.894 Max
Serpentine Trace with Vias (5 Vias)	10GHz	-16.929 Max

Table 1. Comparison of Coupling Strength for the Different Microstripline Structures

5 Conclusion

From the simulation result, guard trace with vias is helpful to decrease the coupling intensity. Serpentine guard trace reduces the far end crosstalk. Guard trace with vias is a good solution. The same result is achieved in serpentine gurad trace with less number of vias, compared to the conventional guard trace. So, serpentine trace helps to reduce the coupling strength. This work may extended to design a optimum dimensions of microstriplinewith serpentine trace by using Particle swarm Optimization.

References

- Lee, K., Jung, H.-K., Chi, H., Kwon, H.J., Sim, J.-Y., Park, H.J.: Serpentine Microstrip Lines with Zero Far End Crossstalk for Parallel High Speed DRAM Interfaces. Proceedings of the IEEE 33(2), 552–558 (2010)
- Lee, K., Lee, H.B., Jung, H.-K., Sim, J.Y., Park, H.J.: A Serpentine Guard Trace to Reduce the Far End Crosstalk Voltage and the Crosstalk Induced Timing Jitter of Parallel MicrostripLines. Proceedings of the IEEE 31(4), 809–817 (2008)
- Sohn, Y.S., Lee, J.C., Park, H.J.: Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board. IEEE Trans. Adv. Packag. 24(4), 521–527 (2001)
- Li, Z., Wang, Q., Shi, C.: Application of Guard Traces with Vias in the RF PCB Layout. Proceedings of the IEEE (2002)
- Lee, K., Lee, H.-B., Jung, H.-K., Sim, J.-Y., Park, H.-J.: Serpentine guard trace to reduce far-end crosstalk and even-odd mode velocity mismatch of microstrip lines by more than 40%. In: Electron. Compon. Technol. Conf., Reno, NV, pp. 329–332 (2007)
- Lee, H.-B., Lee, K., Jung, H.-K., Park, H.-J.: Extraction of LRGCmatrices For 8-coupled uniform lossy transmission lines using 2-port VNA measurements. IEICE Trans. Electron. E89-C(3), 410–419 (2006)