Design of Low Power Enhanced Fully Differential Recyclic Folded Cascode OTA

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Abstract. In the literature, Recyclic Folded Cascode (RFC) and Improved RFC (IRFC) Operational Transconductance Amplifiers (OTAs) are proposed for enhancing the DC gain and the Unity Gain Bandwidth (UGB) of the Folded Cascode (FC) OTA. In this paper, an enhanced RFC (ERFC) OTA which uses positive feedback at the cascode node is proposed for increasing the DC gain and CMRR without changing the unity gain bandwidth (UGB) . For the purpose of comparison, RFC, IRFC and ERFC OTAs are implemented using UMC90nm technology in moderate inversion and studied through simulation. From the simulation, it is found that the DC gain of ERFC OTA is higher by 6dB, 1dB compared to that of RFC and IRFC OTAs respectively. The CM gain of ERFC OTA is lower by 31dB, 34dB compared to that of RFC and IRFC OTAs respectively for the same power and area.

Keywords: Folded Cascode, Recyclic, Common-mode, CMRR, positive feedback.

1 Introduction

High performance A/D converters and switched capacitor filters require Operational Transconductance Amplifiers (OTAs) that has both high DC gain and a high unity gain bandwidth (UGB). The advents of deep sub-micron technologies enable increasingly high speed circuits. As the technology scales down, the intrinsic gain $g_m r_o$ of the transistor decreases which makes it difficult to design OTAs with high DC gain. In low voltage CMOS process, Folded Cascode (FC) amplifier is one of the most preferred architectures for both single stage and the multi stage amplifiers (in the first stage) due to its high gain and reasonably large output signal swing. Moreover, the FC with PMOS input pair is preferred over its NMOS counterpart due to its higher non-dominant poles, lower flicker noise, and lower input common mode range [1].

A number of techniques have been proposed in the literature to enhance the gain of the FC OTA. One of these techniques presented in [2], [3] enhances the DC gain by providing an additional current path at the cascode node. This converts the current source into active current mirror which raises the output current to be above its quiescent value during slewing. Another technique proposed in [4], enhances the DC gain and UGB by modifying the bias current sources of the conventional FC. In the conventional FC these current sources don't contribute to DC gain. A recycling technique

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is proposed to overcome this disadvantage. This OTA is referred to as Recyclic Folded Cascode (RFC).

2 Recyclic Folded Cascode Ota

The bias current sources in the conventional FC [1] consume high current, and have large transconductance. However, these current sources don't contribute to the DC gain. In [4], the input transistors of FC are split into two parts (M1a, M1b, M2a, M2b) which conduct fixed and equal currents of Ib/2. Next the current source transistor in the FC is replaced by current mirrors M3a:M3b and M4a:M4b at a ratio of K: 1. This architecture is called as the RFC OTA and is shown in Fig.1.

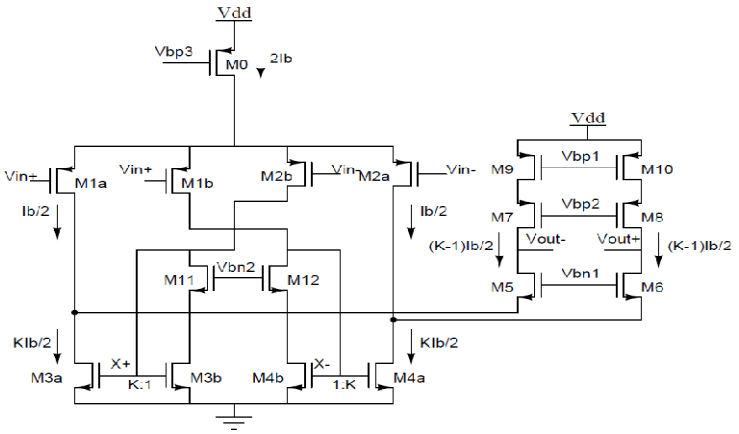

Fig. 1. Recyclic Folded Cascode OTA

2.1 DC Gain

$$A_v = G_m * R_{out} \tag{1}$$

Where G_m is the transconductance and R_{out} is the output impedance.

The transconductance G_m is given by

$$G_m = I_{out}/V_{i+} \tag{2}$$

Where the output current I_{out} is given by

$$I_{out} \approx g_{m1a}V_{i+} + g_{m3a}V_{x+} \tag{3}$$

From Fig.1, it can be seen that transistors M2b and the diode connected transistors M11 and M3b act as a common source amplifier with a voltage gain of approximately -1. Since, the input applied to M2b is in opposite direction, the node X_+ (or X_-) is in the same phase of V_{i+} (or V_{i-})

Where

$$V_{x+} \approx -g_{m2b} R_x V_{i-}$$

and

$$R_x = {}^{1}/_{g_{m3b}}$$

Hence $V_{x+} \approx V_{i+}$

Substituting V_{x+} in (3)

$$I_{out} = g_{m1a} V_{i+} + g_{m3a} V_{i+} \tag{4}$$

Substituting (4) in (3) gives the small signal transconductance G_m.

$$G_m = g_{m1a} + g_{m3a} \tag{5}$$

Where

$$g_{m3a} \approx K . g_{m1a}$$

The output impedance R_{out} of the RFC OTA is given by

$$R_{out} = g_{m5} r_{05} (r_{01a} || r_{03a}) || g_{m7} r_{07} r_{09} \tag{6}$$

Using (5) and (6) in (1), Av is given by

$$\mathrm{A_v} \approx \mathrm{g_{m1a}(K+1).g_{m5} r_{05} (r_{01a} || r_{03a}) || g_{m7} r_{07} r_{09}} \tag{7}$$

3 Enhanced Rfc Ota

In Fig.1, the input impedance Z_C at the cascode node C of the RFC OTA is given by (8)

$$Z_c = \frac{1}{g_{m5}} \left(1 + \frac{g_{m7} r_{07} r_{09}}{r_{05}}\right) \cong \frac{g_{m7} r_{07} r_{09}}{g_{m5} r_{05}} \tag{8}$$

In [3], the cascode node of the FC OTA is modified and the current sources are replaced with an active inverting current mirror. The same approach is adopted for the RFC OTA at the cascode node. The modified half circuit of RFC OTA is shown in Fig.2. The active load of the conventional RFC OTA comprising (M7, M9) is modified into an active inverting current mirror comprising *(*M7*,* M9, M14, M16, and the inverters). A normal current mirror creates a copy of a current of equal magnitude and in the same direction. The inverting current mirror creates a copy of any incremental currents that is equal in magnitude, but opposite in direction. The inverting incremental currents for M7 and M9 can be obtained from M2a and hence the inverters shown in Fig.2 are not required. Therefore, M12, M14 and M16 are attached to the drain of M2a. The fully differential enhanced RFC OTA is shown in Fig.3. The gain from the cascode node to the output node is given by (9). Thus the modified input impedance Z_C at the cascode node is given by (10),

$$\frac{v_{out}}{v_c} \cong (g_{m5} + g_{m12})r_{o5} \tag{9}$$

$$Z_c \cong \frac{g_{m7}r_{07}\,r_{09}}{2g_{m5}r_{05}} \tag{10}$$

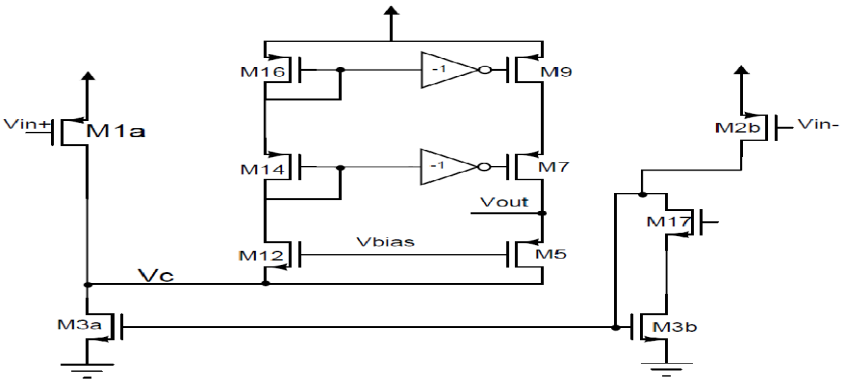

Fig. 2. Half circuit of ERFC

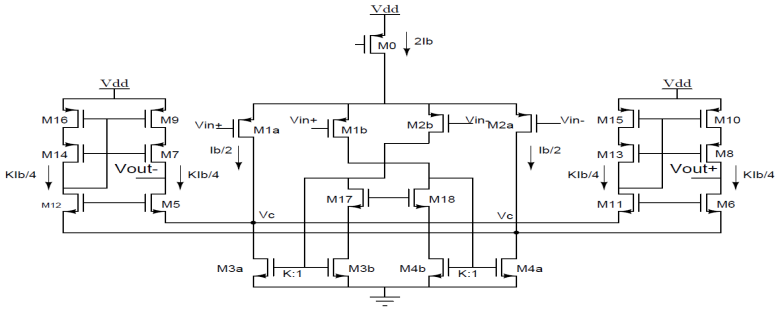

Fig. 3. Proposed Enhanced RFC OTA

3.1 DC Gain

$$R_{out} \approx \left((g_{m5} + g_{m11})r_{05} + 1\right)\left(r_{01a}||r_{03a}||\left(\frac{g_{m7}r_{07}r_{09}}{2g_{m5}r_{05}}\right)\right) \tag{11}$$

$$A_0 \approx \quad G_m R_{out}$$

$$G_m \approx g_{m1a}(1+k)$$

$$A_0 \approx g_{m1a}(1+k)\left((g_{m5} + g_{m11})r_{05}\right)\left(r_{01a}||r_{03a}||\left(\frac{g_{m7}r_{07}r_{09}}{2g_{m5}r_{05}}\right)\right) \tag{12}$$

3.2 Frequency Response

The proposed op amp has three poles: the dominant pole at the output node and the non dominant poles at the cascode node (at the drain node of the input transistor (M1, M2) and a pole at current mirror node. Frequency response of the op amp can be analyzed using the differential half-circuit shown in Fig. 3.

Dominant Pole:
Because of high impedance (R_{out}) and large capacitance (C_{out}) at the output node, the dominant pole occurs in this node.

The dominant pole frequency ω_{p1} is given by

$$\omega_{p1} = \frac{1}{R_{out}C_{out}} \tag{13}$$

where

$$R_{out} \approx (2g_{m5}r_{05} + 1)(r_{01a}||r_{03a}||\frac{g_{m7}r_{07}r_{09}}{2g_{m5}r_{05}}) \tag{14}$$

and

$$C_{out} \approx C_L + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

Where C_{out} denotes the equivalent load capacitance that includes the external capacitance C_L, as well as all the parasitic junction capacitances associated with the output node.

4 gm/I_D Methodology

The g_m/I_D methodology [6] relates the small signal parameter g_m to large signal parameter I_D. There are three degrees of freedom in this methodology - inversion coefficient, drain current and channel length of the transistor. The g_m of the OTA is determined by the unity gain bandwidth (UGB) and the load capacitance. The expression for g_m is given by

$$g_m = \omega_t C_L \tag{15}$$

The g_m gives the transconductance of the input transistor M1a in fig.4, ω_t which is the UGB and c_l is the load capacitance. The different regions of operation give different values of g_m/I_D. The g_m/I_D value is high in weak inversion and the value decreases as we move from weak to strong inversion. Since, the g_m/I_D ratio doesn't depend on the gate width, drain currents I_D achieving any prescribed bandwidth product (for a particular UGB) can be derived from the expression given by (16)

$$I_D = \frac{g_m}{g_m/I_D} \tag{16}$$

The transistors are traditionally biased in the saturation region in the analogue circuits. But, they can be operated in strong inversion or moderate inversion or weak inversion . Transistors biased in weak inversion provide higher transconductance and higher gain with a smaller current [6].Diffusion current and drift current dominate in weak inversion and strong inversion regions respectively. For short channel devices biased in strong inversion, velocity saturation and other small geometry as well high-field effects, reduce the drain current

$$v_{eff} = v_{gs} - v_t \tag{17}$$

The moderate inversion offers high transconductance efficiency and low drain-source saturation voltages compared to strong inversion. Moreover, it results in smaller gate area and capacitances which in turn results in higher bandwidth compared to weak inversion. Hence, as the technology scales down, it is better to operate in moderate inversion. The closed form equation for the drain current in moderate inversion is not available in the literature. An interpolated equation for this region is reported in [6]. In [6], range of effective gate to source voltage (Veff given by (17)) required for each region of operation are given by inequalities (18), (19) and (20). In (18), RHS is taken as -72mv by assuming the substrate factor (n) as 1.4 and U_t as 25.9mv at 300K.
Weak Inversion

$$vgs - v_t < -0.72 \tag{18}$$

Moderate Inversion

$$-0.72 < vgs - v_t < 0.25 \tag{19}$$

Strong Inversion

$$vgs - v_t > 0.25 \tag{20}$$

Gm_{RFC} depends only on the transconductance gm_{1a} of the input transistor. Hence using (7) and (15), Gm_{RFC} can be written as

$$Gm_{RFC} = gm_{1a}\,(1+k) = \omega_t c_l \tag{21}$$

Using (21), gm_{1a} can be found by assuming the UGB of the RFC (ω_t), load capacitance (C_L) and K(which is taken as 3). For an UGB of 110 MHz and a load capacitance of 5.6pF (which is the same as that used in [4]), gm1a becomes 967.61us. The value of gm/Id may be chosen depending on the region in which the transistor is required to operate. Knowing gm and gm/Id, the drain current can be found using (16)

The transconductance values of other transistors can be obtained as follows: As per the architecture, the transconductance values of M1a, M1b, M2a, M2b, M3b, M4b, M11, and M12 in fig.2 should be same. The transconductance of M3a and M4a is k times that of the M3b. The current for M3b can be found using (16). For finding the width and length (W3b, L3b) of M3b, we need to take the ratio of drain current and unary drain current given by (22). The unary drain current is the current flowing

through a transistor when aspect ratio is 1. The unary drain current for M3b transistor is 187.835nA. Similar design procedure is followed for other transistors. [6]

$$\frac{W_{3b}}{L_{3b}} = {}^{I_{d3b}}/_{I_{du3b}} \tag{22}$$

5 Simulation Results

The ERFC OTA, RFC OTA, and IRFC OTA reported in the literature [4][5] are simulated using the UMC 90nm CMOS process with a supply voltage of 1.2 volts. The load capacitance C_L for all the OTAs is 5.6pF. For all three OTAs, parameter K in the bias current source is assumed to be three. The OTAs discussed are implemented and simulated using Cadence SPECTRE Simulator. The area required is the same for all the three OTAs as the transistor widths of M5, M7, and M9 are divided into pairs of M5/M11, M7/M13, M9 and M15. It can be verified from the Table.1 that the size of M5/M7/M9 are 2 times that of the M5/M11/M7/M13/M9/M15. The improvement in common mode rejection ratio can also be analyzed from the Fig.5. Designing a CMFB circuit is difficult for fully differential RFC [4] but that need is eliminated in ERFC. The various parameters of the OTAs such as DC Gain, UGB, Phase Margin, CMRR, slew rate are given in Table.2.

From Fig.4 and Table.2 the following observations may be made:

- The gain of the ERFC OTA is higher by 6dB, 1dB respectively compared to conventional RFC and IRFC OTAs.
- The CM gain of ERFC OTA is lower by 30dB, 34dB compared to that of RFC and IRFC OTAs respectively. This also implies that the CMRR of ERFC OTA is higher by 49dB compared to that of RFC and IRFC OTAs respectively.

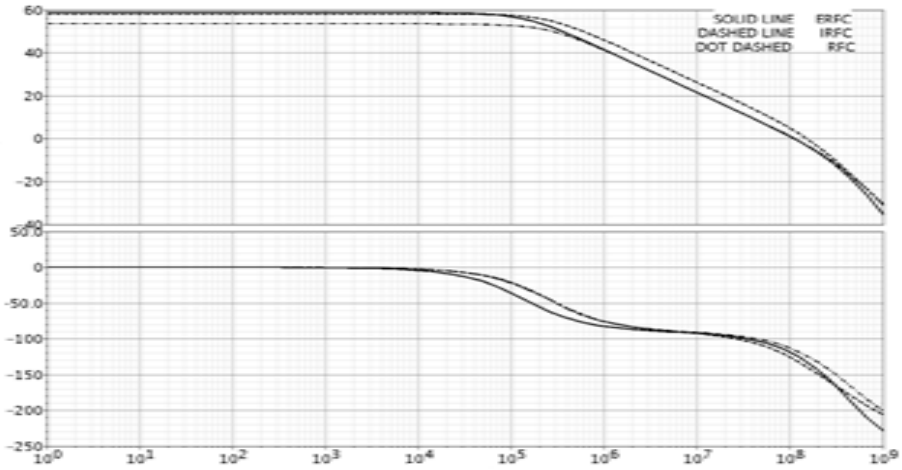

Fig. 4. D.C. Gain and Phase

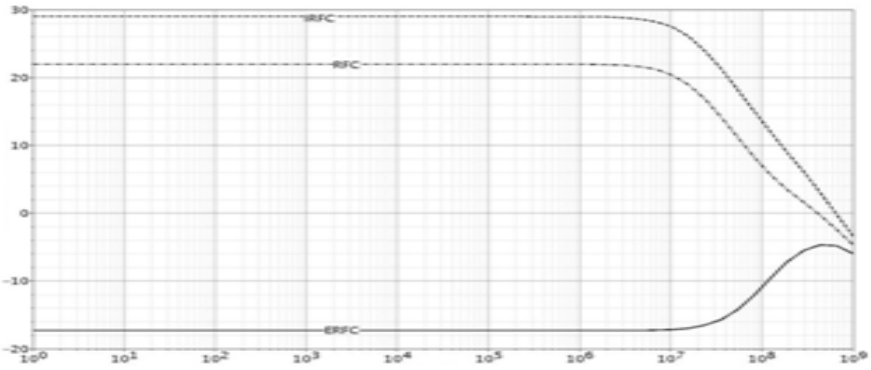

Fig. 5. Common Mode Gain for RFC, IRFC and ERFC

Table 1. Device Sizes of ERFC, RFC and IRFC

Device Sizes	ERFC	RFC	IRFC
M0	53/0.35	53/0.35	53/0.35
M1a/M1b/	268/0.35	268/0.35	268/0.35
M3a/M4a	272.67/0.18	272.67/0.18	272.67/0.18
M3b/M4b	107.14/0.18	107.14/0.18	107.14/0.18
M3c/M4c			12.1/0.35
M5	53/0.35	106/0.35	106/0.35
M11	53/0.35	-	-
M7	4.41/0.35	8.82/0.35	8.82/0.35
M13	4.41/0.35	-	-
M9	12.23/0.35	24.46/0.35	24.46/0.35
M15	12.23/0.35	-	
M11a/M12	12.01/0.35	12.01/0.35	6/0.35
M11b/M12b	-	-	6/0.35

Table 2. Device parameters of ERFC, RFC and IRFC

Device	ERFC	RFC	IRFC
Power	480uW	480uW	480uW
DC Gain	59dB	53dB	58dB
Load	5.6pf	5.6pf	5.6pf
open	60	60	55
GBW[MHz]	108	108	151
Slew Rate(V/uS)	34	31.5	40
CMRR(dB)	76.5	31	29

6 Conclusion

The fully differential enhanced RFC OTA proposed in this paper and RFC as well as IRFC OTAs reported in the literature have been designed and simulated in UMC 90nm CMOS technology. The increase in the low frequency DC gain is achieved by positive current feedback technique. This in turn results in symmetric slew rate and high common mode rejection ratio. The fully differential Enhanced RFC OTA achieves a higher DC Gain and lower CM gain compared to the other two OTAs. The need for CMFB circuit is also avoided.

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