Modified Low-Power Multiplier Architecture

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Abstract. In this paper, we have implemented a modified version of the Bypass Zero Feed A Directly (MODBZ-FAD) multiplier architecture based on shift-and add- method. This architecture has considerably low power than the other multiplier architectures. In this architecture we have reduced the power consumption and propagation delay of the circuit. This has been done by removing Bypass register,dflipflop & multiplexers. The synthesis results shows that the switching activity had been lowered up to 78% and power consumption up to 22% when compared up to BZ-FAD architecture.

Keywords: MODBZ-FAD, Bypass register, D flip-flop, multiplexers, Switching activity, BZ-FAD architecture, power consumption.

1 Introduction

Power dissipation of VLSI chips is traditionally a neglected subject. In the past, the device density and frequency were low enough that it was not a constraining factor chips. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation [2].

2 Related Works

In the previous papers [1] they had proposed about the modifications done to the conventional architecture. The work has been done towards a low power shift-and-add multiplier, and has been proved that BZ-FAD architecture uses low area and low power compared to the conventional architecture. Simulation results shows that architecture lowers the total switching activity up to 76% and power consumption up to30% when compared to the conventional architecture [7].

3 Low Power Multiplier Circuits

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. With

V.V. Das and J. Stephen (Eds.): CNC 2012, LNICST 108, pp. 172–178, 2012.

advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. Thus making them suitable for various high speed, low power, and compact VLSI implementations. Hence in this paper we have tried to design three different architectures of multipliers

1. Conventional Shift-and-Add-Architecture.
2. Bypass zero feed A directly (BZ-FAD) Multiplier Architecture.
3. Modified Bypass multiplier architecture

3.1 Conventional Shift and Add Multiplier Architecture

Conventional shift-and-add multiplier architecture has a simple design and hence occupies simple area. But the major disadvantage of this circuit is its power dissipation. This is due to the many switching activities taking place inside the circuit.

By removing or minimizing any of these switching activity sources one can lower the power consumption [1].

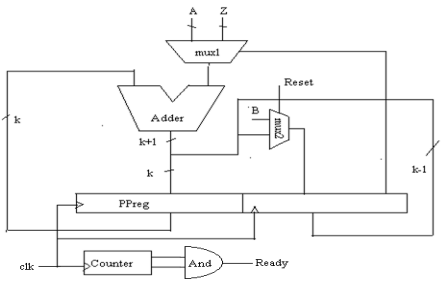

Fig. 1. Conventional shift-and–add multiplier

3.2 BZ-FAD Multiplier Architecture

To get low power architecture, sources of switching activity have been reduced. This involves the shifting of B register ,switching activity of the adder , shifting of the PP register etc [4].

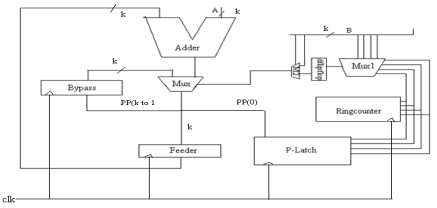

Fig. 2. BZ-FAD multiplier

3.3 Modified BZ-FAD Multiplier Architecture

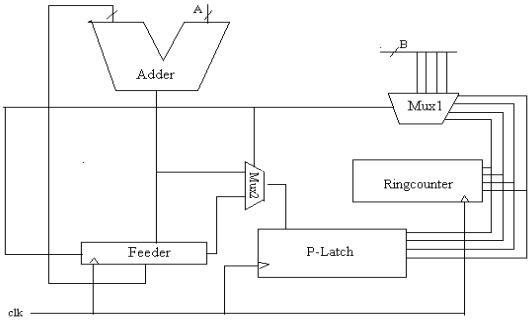

Fig. 3. Modified BZ-FAD multiplier

The above figure shows the modified version of the BZ-FAD architecture. In this architecture we have eliminated some of the components from the previous one which can further reduce the area and the power consumption in the multiplier circuit [3]. A bypass register and mux are eliminated to reduce the shifting activities in the circuit.Similiarly the d- flip-flop and mux2 has been eliminated to reduce the delay. Instead a mux has been introduced to select the LSB between feeder register and the adder block.

The working of the given architecture is described as follows. When B (0) bit of the mux1 equals to one then the MSB of the adder register is loaded into the feeder register and the LSB of the adder will be loaded into the mux2 block else the content of the feeder register itself is right shifted by one bit and the LSB of the feeder will be loaded into the mux2 block. This will be finally stored in the latch. The MSB of the final product will be obtained from the feeder register whereas the LSB will be obtained from the latch.

In previous case the bits of the multiplicand B reaches the main mux only after passing through d-flip flop and mux2.This will increase the delay of multiplier circuit. The d-flip flop and mux2 of the previous architecture has been removed and a direct connection from mux1 to mux2 and feeder register is given here to decrease the delay of the circuit. So along with the power reduction, there is a substantial decrease in the area and delay also.

4 Comparison between BZ-FAD and Modified Architecture

To compare the power dissipation of modified version of the multiplier with that of the modified BZ-FAD multiplier the table reports the power consumption of common components of multiplier.

From the table it is evident that the absence of the multiplexer and bypass register help to reduce the total power consumption of the multiplier. Notice that in modified multiplier the power consumption of the feeder register increases as a result of extra operation in the feeder block. Even if feeder register has increased power, compared

Table 1. Comparison of power consumption of common components of modified multiplier and BZ-FAD multiplier

Component	BZ-FAD	Modified BZ-FAD
Partial Product register	0.4462	0.4462
Adder	0.1256	0.0874
Multiplier	5.686	-
Bypass Register	0.51314	-
Feeder Register	0.2514	5.572

to the total power consumption of both the multiplexer and bypass, the power consumption of feeder is very low. Even the adder in the modified BZ-FAD multiplier consumes less power. So the total power consumption of the Modified BZ-FAD consumes less power.

5 Results and Discussions

In this paper we have given the simulation results of the proposed modified architecture. We used Synopsys Design Compiler for the area and delay analysis and Xilinx ISE 10.1 for timing analysis. To evaluate the efficiency of the proposed architecture, we have implemented two other architectures namely, multiplier using state machine and radix-2 booth multiplier. Both the state machine and the booth multiplier architecture consumes more power and area than the proposed architecture because there are lot of switching activities and signal or state transitions.

We have compared the power consumption of the different multipliers and have found that the modified BZ-FAD architecture consumes 22% lower power than the BZ-FAD architecture. The BZ-FAD architecture has 18% more area than the proposed architecture.

5.1 Simulation Results

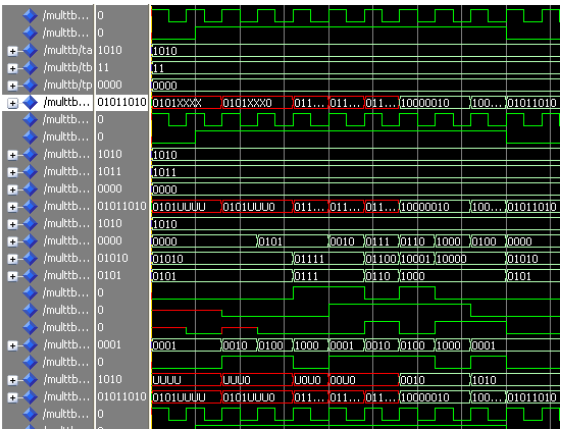

Fig. 4. Simulation Results

5.2 Synthesis Results

Synthesis report in Synopsys and Xilinx 10.1 for each architecture is given below

Table 2. Timing Analysis for different Multipliers

Architecture	Minimum period(ns)	Maximum frequency(MHz
Conventional multiplier	8.208	21.832
BZFAD multiplier	7.122	140.410
Modified BZFAD multiplier	5.969	167.532
Multiplier using state machine	10.291	97.172
Radix-2 Booth multiplier	7.436	134.472

Table 3. Power Analysis for different Multipliers

Multiplier Architectures	Dynamic Power(uW)
Conventional multiplier	21.3590
BZFAD multiplier	16.5663
Modified BZFAD multiplier	12.9959
Multiplier using state machine	20.6566
Radix-2 Booth multiplier	114.2207

Table 4. Area Analysis for different Multipliers

Architecture	Number of cells
Conventional multiplier	6
BZFAD multiplier	9
Modified BZFAD multiplier	6
Multiplier using state machine	168
Radix-2 Booth multiplier	121

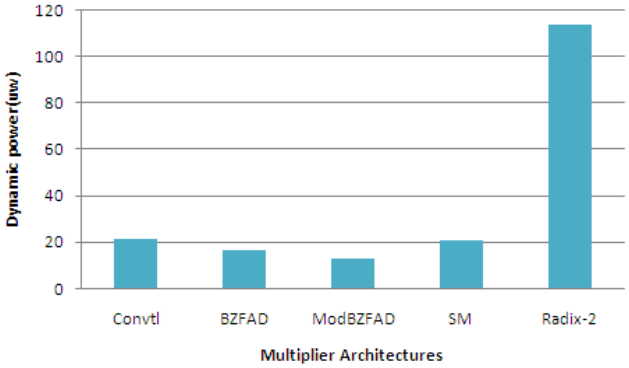

Fig. 5. Power Analysis

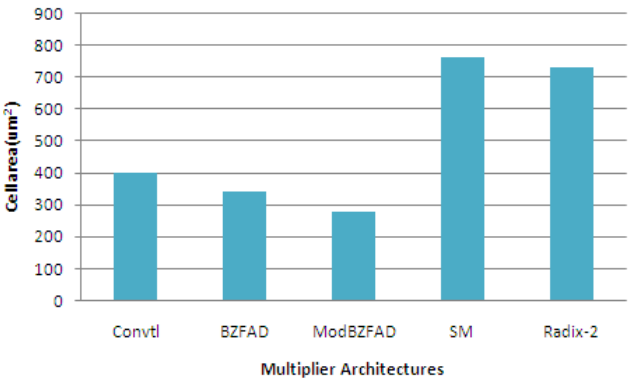

Fig. 6. Area Analysis

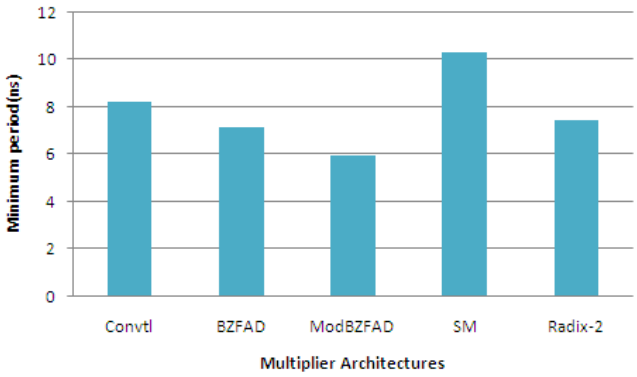

Fig. 7. Timing Analysis

6 Results and Conclusions

In this paper, a modified low-power multiplier based on shift-and-add architecture was proposed. The modifications done to BZFAD multiplier are removal of Bypass register, dflipflop & multiplexers. The synthesis results show that the proposed architecture has 22% lower power than the BZ-FAD architecture. We have compared our architecture with state machine and booth multiplier architecture which shows that the modified BZ-FAD architecture consumes lower power and area amoung the other multiplier architectures.

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