Low Leakage-Power SRAM Cell Design Using CNTFETs at 32nm Technology

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Abstract. Leakage power accounts for an increasingly larger portion of total power consumption in nanometer technologies. Battery powered devices remains idle for most of the time except when in use. However, since the phone remains on, it drains power from the battery. This in-turn reduces battery life. In such a situation, battery power can be saved by shutting down the power supply to the circuit when not in operation. This paper proposes ultra-low power Carbon Nanotube Field-Effect Transistor (CNTFET) based SRAM cell to minimize static power dissipation due to leakage. A Sleep Transistor technique is applied to CNTFET based SRAM cell to reduce leakage power. This method reduces leakage power by dynamically disconnecting supply during inactive state. The 6T SRAM cell circuit using CNTFETs was simulated in HSPICE using Stanford CNFET model at 32nm technology node. The results shows that this method reduces leakage power by 31.5% compared with conventional 6T CNTFET SRAM Cell with minimal area overhead.

Keywords: SRAM Cell, CNTFET, Leakage Power, HSPICE.

1 Introduction

Rapid growth in semiconductor technology has lead to shrinking of feature sizes of transistors using nanometer process. This has allowed for very large circuits with complex functionality to be fabricated on a single chip. As transistor density keeps on increasing so does the power dissipated by the chip. Modern portable battery operated devices such as cellphones, laptops, PDAs are particularly affected by this as high power dissipation reduces battery service life. Thus, power dissipation has now become a vital design metric. Earlier, dynamic or switching power component dominated the total power dissipated by an IC. However, in nanometer regime static or leakage power becomes a dominant proportion of the total power dissipation [1]. Leakage power dissipation arises from the leakage currents flowing through the transistor when there are no input transitions and the transistor has reached steady

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state. The most effective technique for reducing dynamic power dissipation is supply voltage scaling and to maintain performance, transistor threshold voltage also has to be scaled proportionally [2]. This has an adverse effect on leakage power. Thus, in the nanometer regime due to lower supply voltages, leakage power cannot be neglected. To curtail this static power loss, several techniques have been proposed that efficiently minimize leakage power dissipation [3-4].

Since the first CNTFET was reported in 1998, great progress has been made during the past years in all the areas of CNFET science and technology, including materials, devices, and circuits [5]. Carbon Nano Tubes (CNTs) are sheets of graphene rolled into tube. A CNTFET is the analogue of silicon MOSFET in which Single Wall CNTs (SWCNT) replace the silicon channel. Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the SWCNTs can either be metallic or semi-conducting. CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel. Therefore a semiconductor CNT is appropriate for using as channel of FETs. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel [6].

The SRAM leakage power has also become a more significant component of total chip power as a large portion of the total chip transistors directly comes from on-die SRAM. The dominant leakage power component is the subthreshold leakage. Effectively lowering power supply decreases all the leakage components. Since the activity factor of a large on-die SRAM is relatively low, it is much more effective to put in a power reduction mechanism dynamically, which modulates the power supply. But when the SRAMs are required to keep the data retention as the power supply is lowered, the rail-to-rail voltage needs to be carefully controlled to maintain sufficient cell stability, avoiding potential data loss. Especially for modern VLSI processor design, SRAM takes large part of power consumption portion and area overhead. While seeking for solutions with higher integration, performance, stability, and lower power, CNT has been presented for next-generation SRAM design as an alternative material in recent years [7-11]. Hence, this necessitates the need for techniques to reduce this leakage power dissipation in CNTFET based SRAM cell.

2 Leakage Paths in SRAM Cell

Leakage power dissipation arises from the leakage currents flowing through the transistor when there are no input transitions and the transistor has reached steady state. The leakage paths in conventional 6T CNTFET SRAM cell are shown in Fig.1. There are two dominant sub-threshold leakage paths in a 6T SRAM cell: one from V_{DD} to ground paths inside the SRAM cell, called Cell leakage paths and second from the bit-lines 'BL' (or bit-bar line 'BLbar') to ground path through the pass transistor M5 (or M6), called Bitline leakage paths [12].

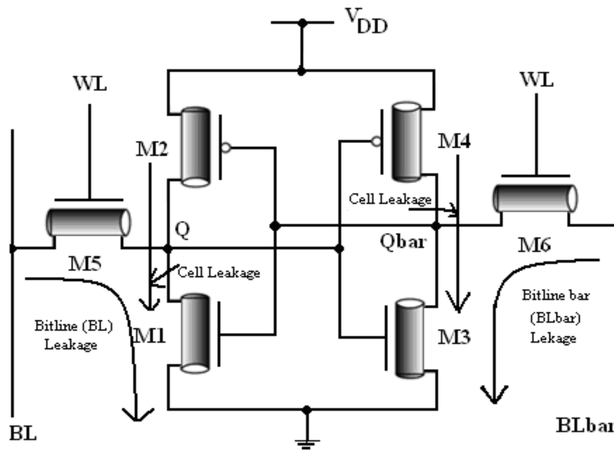

Fig. 1. Leakage paths in 6T CNTFET SRAM Cell

3 Proposed SRAM Cell Design

Subthreshold leakage current and leakage energy dissipation increase exponentially with decreasing threshold voltage. To prevent leakage energy dissipation in a CNTFET SRAM Cell from limiting aggressive threshold-voltage scaling, this paper proposes a Sleep Transistor approach. This sleep transistor technique is applied to SRAM cell based on CNTFETs. Sleep Transistor enables a CNTFET SRAM Cell to "turn off" the supply voltage and eliminate virtually all the leakage energy dissipation in the SRAM's unused sections. The key idea is to introduce an extra transistor in the supply voltage (V_{DD}) or the ground path (GND) of the CNTFET SRAM cells; the extra transistor is turned on in the used sections and turned off in the unused sections. Sleep approach maintains the performance advantages of lower supply and threshold voltages while reducing leakage and leakage energy dissipation. The fundamental reason for the reduction in leakage is the stacking effect of self reverse-biasing series-connected transistors. Extra transistor of the sleep transistor approach produces the stacking effect in conjunction with the CNTFET SRAM cell transistors when the sleep transistor is turned off.

The proposed CNTFET SRAM cell with Sleep transistors is shown in Fig. 2. PMOS sleep transistor MS2 is connected between V_{DD} and the CNTFET SRAM PMOS transistors and NMOS sleep transistor MS1 is connected between GND and the CNTFET SRAM NMOS transistors. These Sleep transistors MS1 and MS2 are turned on for the cell to be in "active" mode and turned off for the cell to be in "standby" mode. These two sleep transistors MS1 and MS2 are controlled by a signal called 'Sleep'. This control signal is '1' in sleep mode and '0' in active mode, so that the sleep transistors are ON in active mode and OFF during inactive or standby mode. This CNTFET based SRAM cell is in active mode when the control signal 'WL' is '1'

and is in inactive or sleep mode when 'WL' is '0'. When a control signal 'WL' is '0', a 'Sleep' is set to '1' and 'SleepBar' to '0' so that sleep transistors MS1 and MS2 are OFF, there by leakage currents are reduced and hence leakage power.

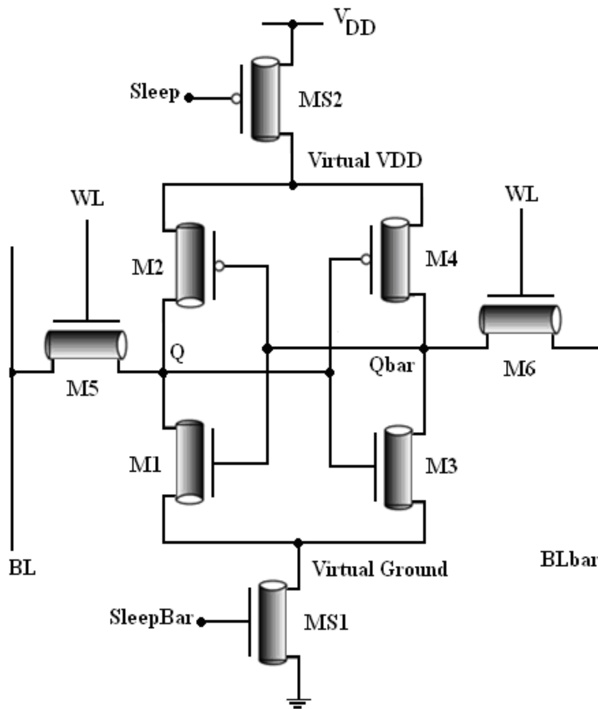

Fig. 2. 6T SRAM cell using CNTFETs with Sleep Transistor

These Sleep Transistors MS1 and MS2 can be shared among multiple SRAM cells to amortize the overhead. To reduce the impact on SRAM cell speed and to ensure stability of the SRAM, the sleep transistors must be carefully sized with respect to the SRAM cell transistors when they are gating. While these sleep transistors must be made large enough to sink the current flowing through the SRAM cells during a read/write operation in the active mode, too large a sleep transistor may reduce the stacking effect, thereby diminishing the energy savings. Moreover, large transistors also increase the area overhead.

4 Results and Discussions

Synopsis HSPICE is used for simulation purpose to estimate delay and power consumption. Simulations performed with Stanford CNTFET model at 32nm feature size with supply voltage V_{DD} of 0.9V [13]. The HSPICE Cscope is used for

displaying simulation waveforms. Simulation waveforms of leakage currents through off transistors M1, M4 and M6 of a 6T CNTFET SRAM Cell for assumed storage bit of Q='1' without and with sleep transistors are shown in Fig. 3 and these leakage current values are tabulated in Table 1. Similarly simulation waveforms of leakage currents through off transistors M2, M3 and M5 of a 6T CNTFET SRAM Cell for assumed storage bit of Q='0' without and with sleep transistors are shown in Fig. 4 and these leakage current values are tabulated in Table 2. From these waveforms it is conformed that the leakage currents through off transistors of 6T CNTFET SRAM Cell with Sleep Transistors are very small compared to 6T CNTFET SRAM cell with out Sleep Transistors. This technique is reducing the leakage power in 6T CNTFET SRAM cell by 31.5% compared with the conventional 6T CNTFET SRAM cell without sleep transistor with the same delay but at the cost of minimal increase of area. Simulated results of CNTFET SRAM cell with and without Sleep Transistors are and summarized in Table 3 for comparison.

Table 1. Lekage Current through OFF transistors if Q=1

Sl. No.	Leakage Currents (A)	6T CNTFET SRAM Cell Without Sleep Transistors	6T CNTFET SRAM Cell With Sleep Transistors
1	I (M1)	1.767e-06	1.130e-08
2	I(M4)	7.133e-07	2.365e-08
3	I(M6)	6.789e-06	3.168e-07
4	Total Leakage	7.843e-06	3.292e-07

Table 2. Lekage Current through OFF transistors if Q=0

Sl. No.	Leakage Currents (A)	6T CNTFET SRAM Cell Without Sleep Transistors	6T CNTFET SRAM Cell With Sleep Transistors
1	I (M2)	1.767e-06	1.117e-08
2	I(M3)	7.133e-07	2.350e-08
3	I(M5)	6.829e-06	2.758e-07
4	Total Leakage	7.883e-06	2.882e-07

Table 3. Simulation Results

Sl. No.	Parameter	6T CNTFET SRAM Cell Without Sleep Transistors	6T CNTFET SRAM Cell With Sleep Transistors
1	Leakage Power (W)	6.95E-9	4.76E-9
2	Read Delay (S)	2.401E-10	2.399E-10
3	SNM (mV)	154	109

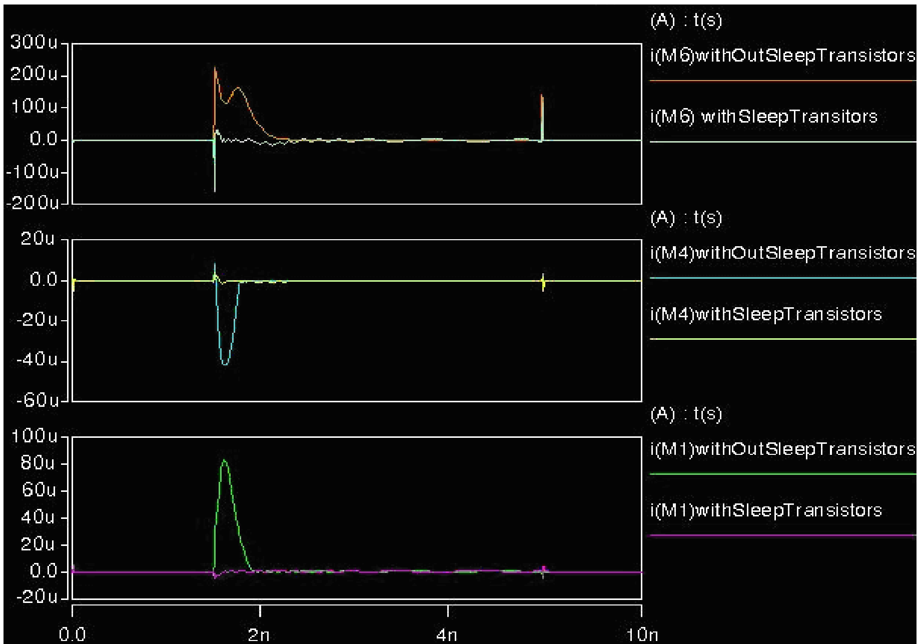

Fig. 3. Leakage currents flowing through the 6T CNTFET SRAM cell with and without Sleep Transistors when Q='1'

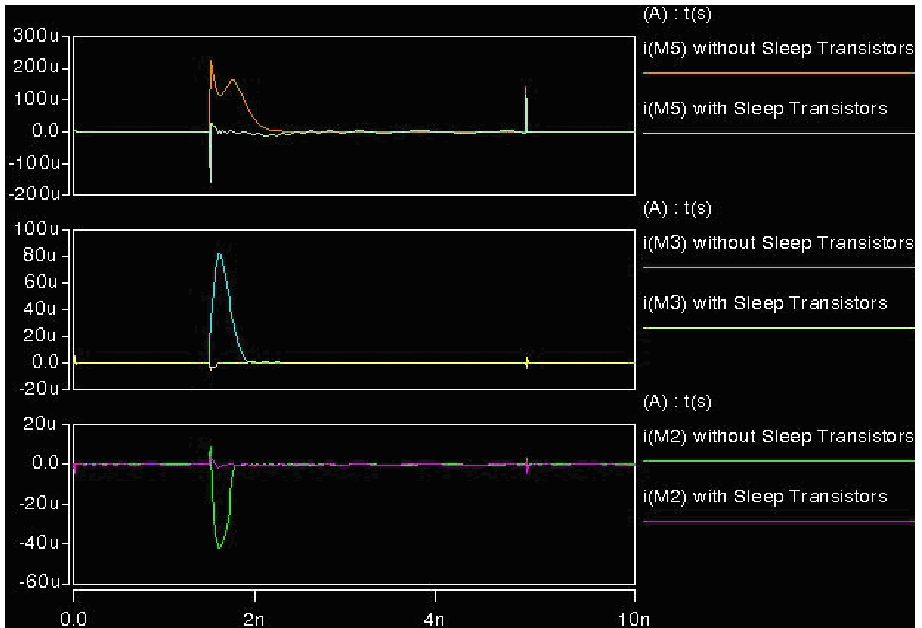

Fig. 4. Leakage currents flowing through the 6T CNTFET SRAM cell with and without Sleep Transistors when Q='0'

5 Conclusion

CMOS technology in nanometer scale faces great challenge due to sub-threshold leakage power Consumption. In this paper a conventional 6T SRAM cell based on CNTFET is designed for leakage power reduction by applying Sleeping Transistors technique. The results show that this design reduces a leakage power to the significant effect by maintaining delay but with minimal increase in area. Proposed cell can be used in design of CNTFET based ultra-low SRAM Memories. This cell can be used for design of low-leakage memory based on CNTFET technology.

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