Implementation of LFSR Counter Using CMOS VLSI Technology

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Abstract. CMOS stands for Complementary Metal Oxide Semiconductor. It is basically a class of integrated circuits, and is used in a range of applications with digital logic circuits, such as microprocessors, microcontrollers, static RAM, etc. It is also used in applications with analogue circuits, such as in data converters, image sensors, etc. There are quite a few advantages that the CMOS technology has to offer. One of the main advantage that CMOS technology, which makes it the most commonly-used technology for digital circuits today, is the fact that it enables chips that are small in size to have features like high operating speeds and efficient usage of energy. Besides, they have very low static power supply drain most of the time. Besides, devices using CMOS technology also have a high degree of noise immunity. This paper presents the implementation of a LFSR (Linear Feedback Shift Register) counter using the recent CMOS sub-micrometer layout tools. Adding to the advantage of CMOS technology, the LFSR counter can be used as a new trend setter in cryptography and can also be beneficial when compared to GRAY & BINARY counter while not forgetting the variety of other applications LFSR counter has.

Keywords: Chip technology, Layout level, LFSR, Pass Transistor.

1 Introduction

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for comparatively lesser price and portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. There are main two sources of power dissipation in digital circuits; these are static (mainly due to leakage current and its contribution to total power dissipation is very small) and dynamic (due to switching i.e. the power consumed due to short circuit current flow and charging of load capacitances) power dissipation. Hence, it is important aspect to optimize power during testing. Power optimization is one of the main challenges.There has been various low power approaches proposed to solve the problem of power dissipation

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i.e. to decrease the power supply voltage, switching frequency and capacitance of transistor during the testing [1]. Here, this paper presents one such approach and that is LFSR counter which has low power architecture. The LFSR is used in variety of applications such as Built-in-self test (BIST) [2], cryptography, error correction code and in field of communication for generating pseudo-noise sequences. Nowadays LFSR's are present in nearly every coding scheme as they produce sequences with good statistical properties, and they can be easily analyzed. Moreover they have a low-cost realization in hardware. Counters like Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks. They produce not only glitches, which increase power consumption but also complexity of design. The propagation delay of results of existing techniques is more which reduces speed & performance of system. LFSR counters overcome these problems which are implemented using different technologies of CMOS.

2 LFSR

LFSR i.e. Linear Feedback Shift Register is a shift register whose input bit is a linear function unlike most everyday devices whose inputs and operations are effectively predefined. LFSR when clocked moves the signal through the register from one flip flop to next. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A LFSR can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip flops as shown in Fig.1.

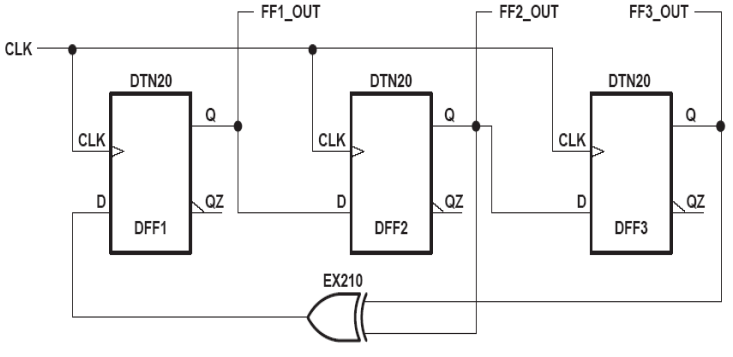

Fig. 1. Linear Feedback Shift Register

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, a LFSR with a well-chosen feedback function can produce a sequence of bits which appears random in nature & which has a very long cycle.

2.1 Working

Pseudorandom Pattern Generation. Linear feedback shift registers make extremely good pseudorandom pattern generators. When the outputs of the flip-flops are loaded with a seed value (anything except all 0s, which would cause the LFSR to produce all 0 patterns) and when the LFSR is clocked, it will generate a pseudorandom pattern of 1s and 0s. Note that the only signal necessary to generate the test patterns is the clock. The list of bits position that affects the next state is called the tap sequence. The outputs that influence the input are called taps.The tap sequence of an LFSR can be represented as a polynomial mod 2. This means that the coefficients of the polynomial must be 1's or 0's. This is called the feedback polynomial or characteristic polynomial. For example: if the taps are at the 3rd, 4th, bits the resulting LFSR polynomial is X4+ x3 +1.The '1' in the polynomial does not correspond to a tap. The powers of the terms represent the tapped bits, counting from the left.

Table 1. Pattern Generation by LFSR Counter

Clock pulse	FF1OUT	FF2OUT	FF3OUT	FF4OUT
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	1	0	0	1
8	1	1	0	0
9	0	1	1	0
10	1	0	1	1
11	0	1	0	1
12	1	0	1	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	1	1	1

FF1OUT –Output of flip flop 1, FF2OUT-output of flip flop 2, FF3OUT-Output of flip flop 3, FF4OUT-Output of flip flop 4.

If (and only if) this polynomial is a primitive, then the LFSR is maximal. The LFSR will only be maximal if the number of taps is even. The tap values in a maximal LFSR will be relatively prime. There can be more than one maximal tap sequence for a given LFSR length. Its output for the various condition of input is expressed in Table 1.

2.2 Design Aspects

A CMOS layout of LFSR Counter is designed.The logic hardware contains a D FlipFlop, a 2-input OR gate, a 2 input XOR gate and inverters. The most important component of our LFSR Counter Design is D Flip Flop. The D-flip flop is designed using following different components: NAND Gates, Transmission gates, inverter and

Pass transistors. Firstly from among the three designs, comparison is done for the power consumption; then the most efficient D-flip flop is selected for the LFSR implementation.The design of D-flip flop and the implementation of LFSR counter are carried out in MICROWIND software.

2.3 Layout Aspects

Layout of D-FlipFlop. Before implementing the whole circuit, a gate-level schematic in DSCH3 is generated. DSCH3 program is a logic editor and simulator used to validate the architecture of logical circuit, before microelectronics started. It provides user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows design and validation of complex logic structures. After successful simulation the above designs of D Flip Flop are implemented with different components using MICROWIND 3.1 CMOS layout tool for its ease of use and availability. The result of the implementation is detailed below.

Design of D-FlipFlop Using NAND Gate. Layout of LFSR counter in which D Flip flop is implemented using NAND gates is as shown Fig.2.

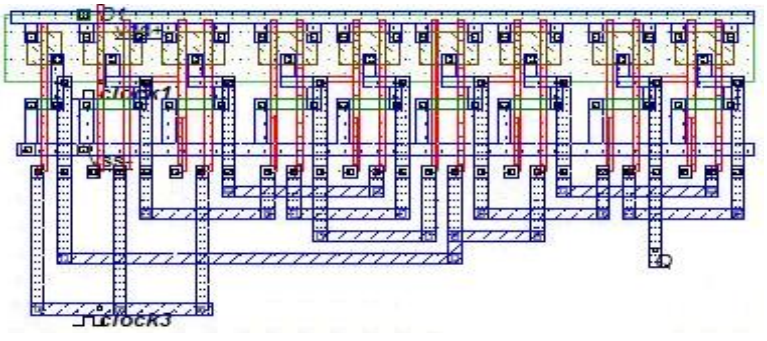

Fig. 2. Layout of D Flip Flop using NAND gate

Design of D-FlipFlop Using Transmission Gate. Layout of LFSR counter in which D Flip flop is implemented using transmission gates is as shown Fig.3.

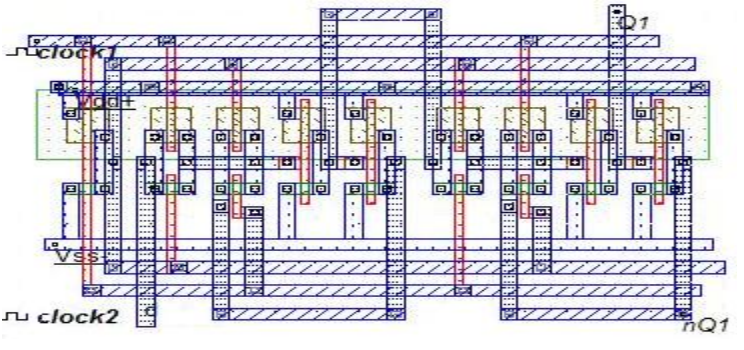

Fig. 3. Layout of D Flip Flop using Transmission gates

Design of D-FlipFlop using Transistor Pass. Layouts of LFSR counter in which D Flip Flop is implemented using transmission gates is as shown Fig.4.

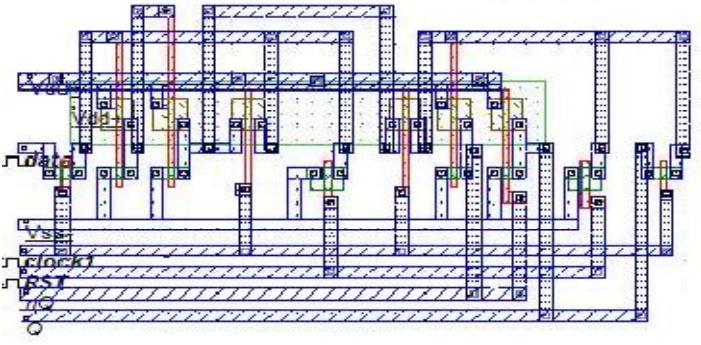

Fig. 4. Layout of D Flip Flop using Transistor Pass

Result of LFSR Layout Implementation. In Table 2 and Table 3the LFSR layouts are compared. The layouts are implemented in 120 nm and 90 nm technology respectively. The various parameters because of different technologies and D Flip Flop design is tabulated for further conclusion and CMOS layout using Pass transistors is as shown in Fig.5.

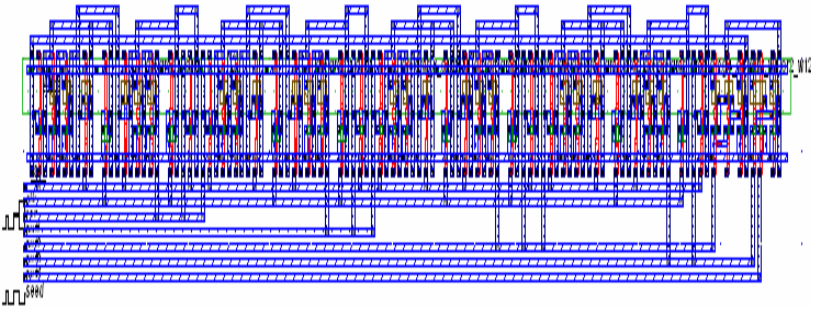

Fig. 5. Layout of LFSR in MICROWIND

Table 2. LFSR in 90 nm Technology

Component	No of Transistors	Power Consumption (Microwatt)	Max Frequency (GHz)	Layout Area (Micro Sq. Meter)
NAND Gates	148	106.0	1.96	295
Transmission Gates	86	99.6	1.7	270
Pass Transistors	68	28.188	1.4	321

Table 3. LFSR in 90 nm Technology

Component	No of Transistors	Power Consumption (Microwatt)	Max Frequency (GHz)	Layout Area (Micro Sq. Meter)
NAND Gates	148	169	1.78	224.8
Transmission Gates	86	155	1.8	390.1
Pass Transistors	68	50.471	1.814	460

3 Comparison of LFSR and GRAY Counter Layout

From Table 2 and Table 3 it is clear that LFSR is optimally implemented layout when compared to the layout of GRAY counter. A layout of both counters is implemented using 120 nm and 90 nm technology. From the layouts various critical parameters are tabulated in Table 4.

Table 4. LFSR in 90 nm Technology

Component	No of Transistors	Power Consumption (Microwatt)	Max Frequency (GHz)	Layout Area (Micro Sq. Meter)
GRAY	188	40.25	0.756	949.6
LFSR	68	28.188	1.4	321

4 Conclusion

The implementation concludes that LFSR counter is best using the pass transistors. In this, the number of transistors required is minimum i.e. 19, power consumption is 28.188 Microwatt, Max operating frequency is 1.4 GHz, layout Size area is 321 Micro Sq meter. Thus it is preferable over Gray counters in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & glitches. Thus LFSR implemented in CMOS chip technology, is the best illustration of VLSI.

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