An Offset-Free 10 MHz Limiting Amplifier Designed for a 5.8 GHz ETC Receiver

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Abstract. Electronic tolling collection (ETC) system will be largely adopted in the next generation of Chinese highway network, and its operating frequency is specified to be 5.8 GHz. A limiting amplifier designed for the 5.8 GHz receiver of the ETC system is presented in this work. AC-coupled gain stage was realized to avoid additional offset cancellation mechanism. The trade-off between the small signal gain, number of stages, gain-bandwidth product, and power dissipation was studied by systematic analysis. Implemented using a standard CMOS 0.18 μm process, the simulation results show that the limiting amplifier achieves overall small signal gain of 81 dB, with 20 MHz bandwidth.

Keywords: Electronic tolling collection (ETC), limiting amplifier, received signal strength indicator (RSSI), offset-free section.

1 Introduction

This Electronic tolling collection (ETC) system adopts radio frequency identification (RFID) technology to facilitate tolling collection in a long range. Because a vehicle is allowed to be charged without slowing down, the ETC is thought to be an effective method to alleviate traffic congestion, and it will be largely adopted in the next generation of the highway network in China. The Standardization Administration of the People's Republic of China (SAC) has already released the Chinese standard of Dedicated Short Range Communications (DSRC), in which the ETC operating frequencies is defined to be 5.8 - 5.9 GHz [1].

The radio frequency (RF) signal processing components are crucial to improve the communication quality in an ETC system. Due to its simple, robust structure and low power consumption, direct conversion architecture is a good fit for an ETC receiver. The architecture of a typical direction conversion receiver is shown in Fig.1. The RF front-end is composed of a low noise amplifier (LNA) and a mixer. The RF input signal is first amplified by the LNA, and is then down-converted to an intermediate-frequency (IF) by

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the mixer, in order to prevent the high DC offset caused by the leakage from the local oscillator to the front-end input. A band-pass filter (BPF) following the mixer extracts the useful information, and a demodulator (Demod) together with the clock and data recovery circuit (CDR) is used to convert the received data into baseband for further processing.

In an ETC system, if multiple vehicles are presented at the tolling gate at the same time, an automatic communication channel selection mechanism should be used to assign a distinct communication channel for each one. This can be realized by inserting a received signal strength indicator (RSSI) into the receiver chain, as shown in Fig.1. The ETC receiver on a vehicle can first scan all the possible communication channels, and analyzes the received signal strength. The bi-directional communication link with the tolling gate will only be established if a vacant channel is found.

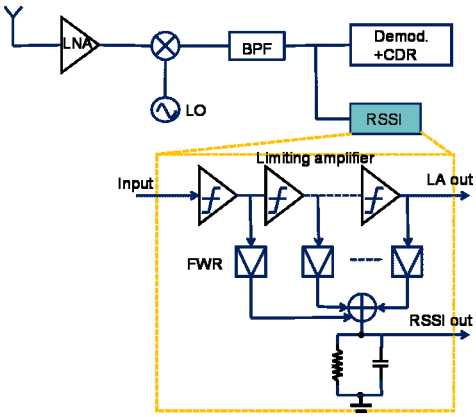


Fig. 1. Architecture of 5.8 GHz RF receiver

The RSSI circuit consists of a limiting amplifier, rectifiers, and a passive current summation network. In order to cover a wide input dynamic range, the limiting amplifier uses multiple cascaded gain stages to achieve a logarithmic character [2]. The output of each amplifying stage is sent to a rectifier, through which the input voltage of each gain stage is converted into an current. These currents are then summed together to indicate the power level of the input signal.

Generally in a RSSI, the random offset voltage appeared at the input of each gain stage will accumulate and deteriorate the overall performance of the limiting amplifier, and therefore additional offset cancellation mechanism is inevitable to ensure the system performance [3]. However, in a direction conversion receiver as shown in Fig.1, if a RSSI is targeted for the down-converted signal at the IF frequency, the gain stages in the limiting amplifier can be AC-coupled, and therefore the offset cancellation mechanism is not necessary.

This paper presents an offset-free limiting amplifier designed for the ETC receiver under developing in Shenzhen University. The paper is organized as follows: In section 2, a systematic level design process is presented to help determine the optimal circuit parameters, such as the number of stages, small signal gain required for each gain stage, and the overall power dissipation. Section 3 discusses the detailed design

of the limiting amplifier. Implemented in a standard 0.18 μm CMOS process, the system is validated under the Zeni IC design environment. The simulation results are given in section 4. Finally, a conclusion is drawn in section 5.

2 Systematic Level Design

In order to prevent the random offset voltage presented at the input of each gain stage to accumulate along the amplifier chain, high pass networks implemented using passive components are added in between each gain stage. The systematic level diagram of an offset-free limiting amplifier is given in Fig.2.

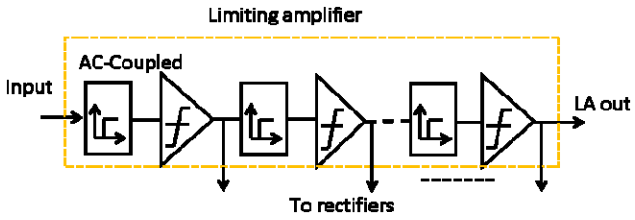


Fig. 2. Systematic level diagram of a limiting amplifier with AC-coupled gain stages

In our design, the required overall small signal gain is specified as 82 dB. In order to have a best compromise among small signal gain of each stage gain, bandwidth, and power dissipation, systematic level analysis is first performed to determine key parameters of each gain stage.

For simplicity, all gain stages are kept identical. For the 1st order approximation, the voltage transfer function of each gain stage can be estimated as

$$\begin{aligned} V_{out} &= AV_{in}, \quad \text{for} \quad V_{in} < V_S \\ V_{out} &= V_L, \quad \text{for} \quad V_{in} \geq V_S \end{aligned} \quad , \tag{1}$$

in which A is the small signal gain of each stage, Vs is the threshold voltage, above which a gain stage is saturated, and VL is the output voltage if the stage is saturated.

All gain stages operate in the linear region when the input signal is small enough. If the number of the stages is N, the output voltage of the limiting amplifier is then A^N x Vin. When the input signal strength increases progressively, the gain stages will be driven into saturation one by one starting from the last stage. Therefore, an approximated logarithmic relationship can be obtained between the input / output voltage of the limiting amplifier.

The linearity (in terms of dB) of the RSSI is determined by the gain of the each stage and the total number of stages consisting of the limiting amplifier. Although increasing the small signal gain and the stage number can improve the linearity, the required bandwidth of each gain stage, and the total power dissipation on the other hand will be deteriorated. The relationship among the stage gain, the overall bandwidth, and the power dissipation is studied by the normalization method presented in [2]. If the overall small signal gain and bandwidth of the limiting

amplifier are noted as A_V and f_V, the normalized gain and bandwidth (A_C and f_C) for the identical single stage are given in the following:

$$A_C = A_V^{(1/N)-1} \tag{2}$$

$$f_C = \frac{f_V}{\sqrt{2^{1/N}-1}} \tag{3}$$

From (2), although the voltage gain for each gain stage can be reduced when the cascading number of stages increases, but a large bandwidth is required in such condition, which is indicated by (3). Thus, the gain-bandwidth product (GBW) is used in the design procedure. Specifying the overall gain of 82 dB, the normalized gain, bandwidth, and the GBW values are calculated as the function of the stage number, and the results are plotted as shown in Fig.3.

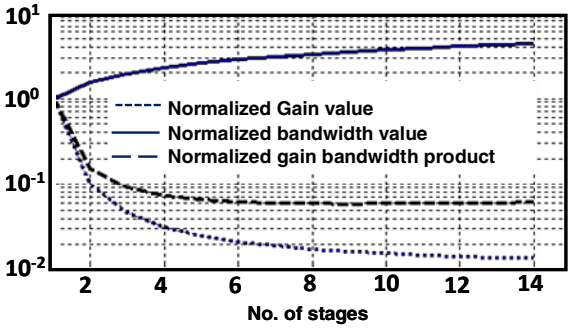


Fig. 3. Normalized gain, bandwidth and GBW of single gain stage for a limiting amplifier with 82 dB small signal gain

As shown in Fig.3, the bandwidth requirement tends to be stabilized when the stage number is larger than 10. However, a large number of gain stages will result in more power dissipation. If the power of the each stage gain is defined as P_C, the overall power consumption of the limiting amplifier P_V can be estimated by (4) [4]:

$$P_V = N \times P_C \propto N \times (GBW)^2 \tag{4}$$

In (5), the GBW is proportional to square root of the power consumption for each gain stage P_C, which is given in (5) :

$$GBW = \frac{g_m}{C} = \frac{\sqrt{2\mu C_{ox}(W/L)I_d}}{kWL} \propto \sqrt{\frac{I_d}{WL^3}} = \sqrt{\frac{P_C}{V_{DD}WL^3}} \tag{5}$$

, where I_d is the bias current of the identical gain stage, W and L are the width and length of the MOS transistor that provides the trans-conductance.

For 82 dB overall small signal gain, the normalized power consumption of the limiting amplifier is calculated for different stage numbers, as plotted in Fig.4. The total power consumption decreases as the number of stages becomes larger and

remains stable when the stage number is larger than 4. Considering the requirements of logarithmic approximation [5], totally 9 stages are included in this design and the corresponding gain of each stage should be about 9 dB. In this case, the maximum error [5], defined as the maximum deviation of the implemented output-input voltage response from the ideal logarithmic function, is about 0.14 dB.

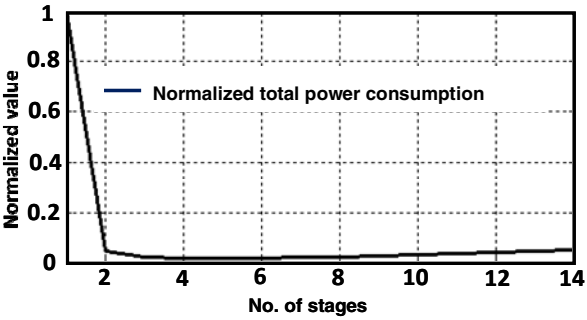


Fig. 4. Normalized total power consumption of a limiting amplifier with 82dB small signal gain

3 Circuit Implementation

The single gain stage employs a simple differential amplifier with NMOS input pair, and resistive load R_D. A source degeneration resistor *R3* is added to improve the amplifier linearity. The AC-coupling between consecutive gain stages is realized by adding series capacitors *C1* and *C2* to the input, and therefore a passive high pass network is formed with the help of resistors *R1* and *R2*. The input pair is also self-biased through *R1* and *R2*, and therefore only a single bias voltage V_b is required to sustain the circuit operation. The detailed schematic of the gain stage is given in Fig.5.

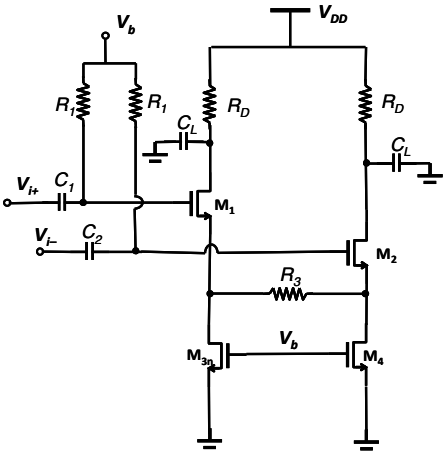


Fig. 5. Schematic of a single AC-coupled gain stage

Neglecting the gate-bulk capacitance of the input NMOS pair, the overall voltage gain of the identical gain stage can be written as:

$$A_V = \frac{G_m \times R_D \| C_L}{1 + sR_1C_1} = \frac{sG_mR_DR_1C_1}{(1+sR_1C_1)(1+sR_DC_L)} \tag{6}$$

, where C_L is the load capacitance at the amplifier output.

Form (6), it is noted that the gain stage has a band-pass characteristic, and the passing band is determined by the two amplifier poles: $1/(R_1C_1)$ and $1/(R_DC_L)$.

The common mode rejection ration of the stage is given in (7),

$$CMRR = \frac{A_{vd}}{A_{cm}} = \frac{(g_m r + 1)(sR_DC_L + 1)}{g_m R_D(sC_L r_{1,2} + 1) + r_{1,2}}, \tag{7}$$

where $r_{1,2}$ is the channel resistances of M_1 / M_2, and r equals to $R_3/2$.

4 Design Validation

The 9-stage limiting amplifier was implemented using a standard 0.18 μm CMOS process. In this design, C_1, C_L, R_1 and R_D are selected as 950 fF, 400 fF, 71.5 KΩ and 3.76 KΩ, respectively. The finished layout of the limiting amplifier is shown in Fig.6. The complete design occupies 810 x 290 μm^2 of silicon area.

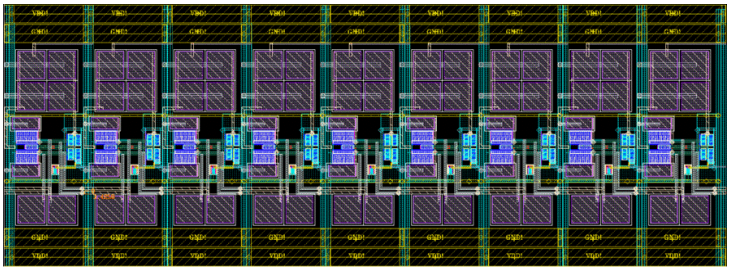
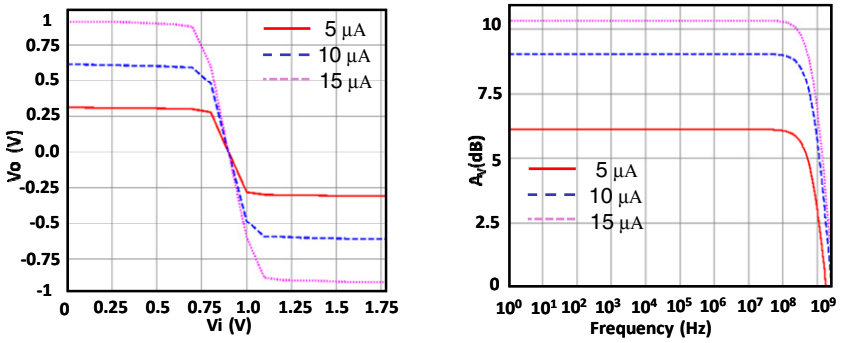


Fig. 6. Layout of the 9-stage offset-free limiting amplifier

Under Zeni IC design environment, the system performance is characterized. The performance of the identical gain stage is first studied under three different bias current I_{SS}, which were 5 μA, 10 μA, and 15 μA. The simulation results of the gain stage without the AC-coupled block are given in Fig.7. From Fig.7 (b), the 3 dB cutoff frequencies of the three cases are around 100 MHz, while the gains are 6.5 dB, 8.8 dB and 11 dB, respectively. The required DC bias voltage Vb can be obtained by the voltage transfer characteristics, which is around 0.9V as given in Fig.7 (a).

The AC performance of the single gain stage with the AC-coupled block is also simulated for the three bias currents, and the results are given in Fig.8. When the bias current is 15 μA, the block achieves a gain 8.8 dB, which is close to the optimization result discussed in section 2.



(a) (b)

Fig. 7. Single gain stage performance under different bias currents: (a) voltage transfer characteristics; (b) gain and bandwidth

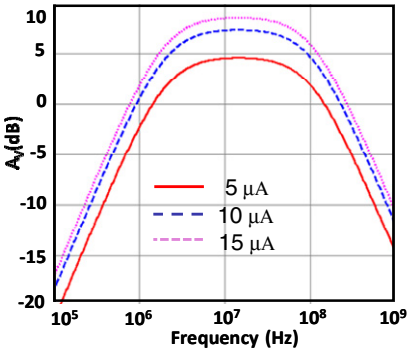


Fig. 8. Frequency response of the AC-coupled gain stage

The performance of the 9-stage limiting amplifier is studied through AC simulation, and the results are given in Fig.9. An overall small signal gain around 81 dB is achieved. The limitting amplifier presents a band-pass characteristcs with the center frequency at around 10 MHz, and the 3dB bandwidth is about 20 MHz (3.8 MHz - 23.55 MHz), approximately 1/5 of the bandwidth of an identical gain stage.

Varying the input signal strength from -100 dBm to 0 dBm (at 10 MHz carrier frequency), the -3 dB input sensitivity of the limiting amplifier is studied under different DC offset voltage, which vary from -50 mV to +50 mV. The results (as shown in Fig. 10) perfectly overlap, indicating the offset voltages at the input of each gain stage do not have noticeable impact on the system performance. The -3 dB input sensitivity of the finished limiting amplifier is about -50 dBm.

The power consumption of the completed limiting amplifier is around 250 µW with a 1.8 V DC supply voltage.

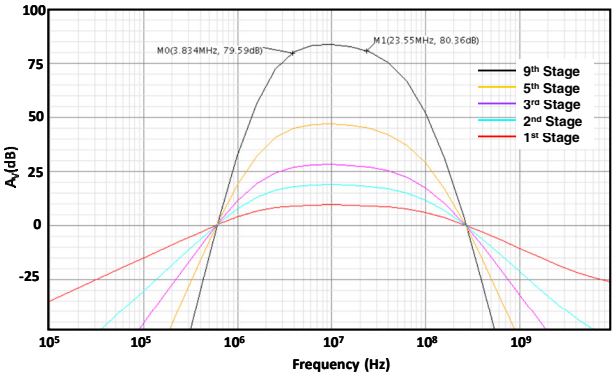


Fig. 9. Simulated gain at the outputs of various gain stages

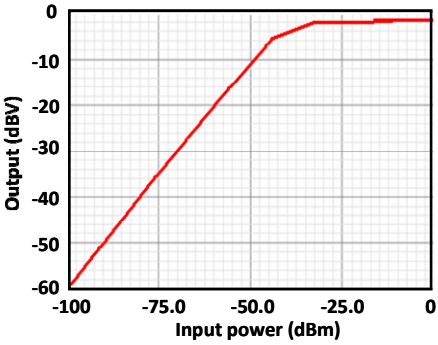


Fig. 10. The input-output transfer response of the limiting amplifier (with input DCoffset voltage ranging from -50 mV to 50mV)

5 Conclusion

A 9-stage limiting amplifier designed for the RSSI of a 5.8 GHz ETC receiver is presented in this work. Because the system is targeted for the down-converted signal at 10 MHz IF frequency, the offset cancellation mechanism generally included in the limiting amplifier designs is not required. Instead, the cascaded gain stages are AC coupled. The designed limiting amplifier consists of 9 identical gain stages in total, and the small signal gain is set to 9 dB for each stage. The optimized design is implemented in a standard 0.18 μm CMOS process, and validated under the Zeni IC design environment. Simulation results show that the limiting amplifier achieves the overall small signal gain of 81 dB at the center frequency of 10 MHz, and consumes about 250 μW from a single 1.8V power supply.

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